

Figure 1: layout of DP130 chip between the FPPCIE-098-02-F-D-EMS2GA and the output processor

Inter-connect connector: Samtec P/N PCIE-098-02-F-D-EMS2 – rated up to 7 GHz / 14 Gb/s

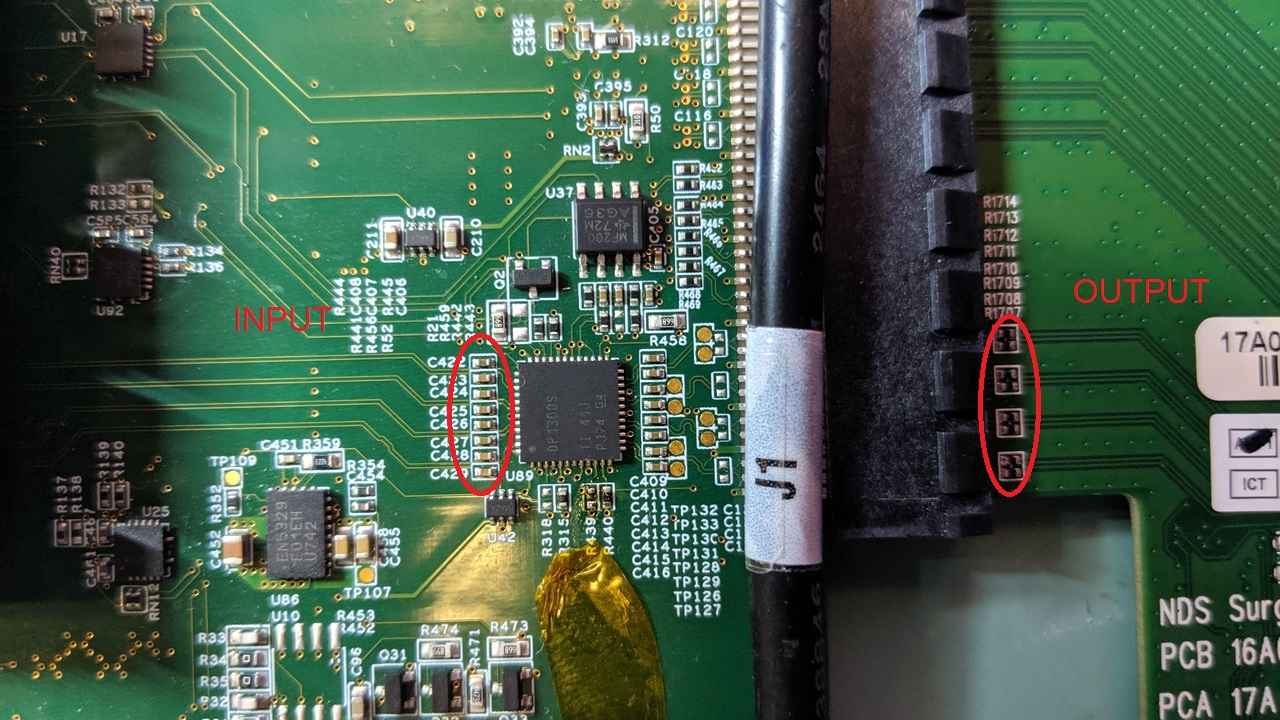


Figure 2: location where differential input signals and output signals are measured

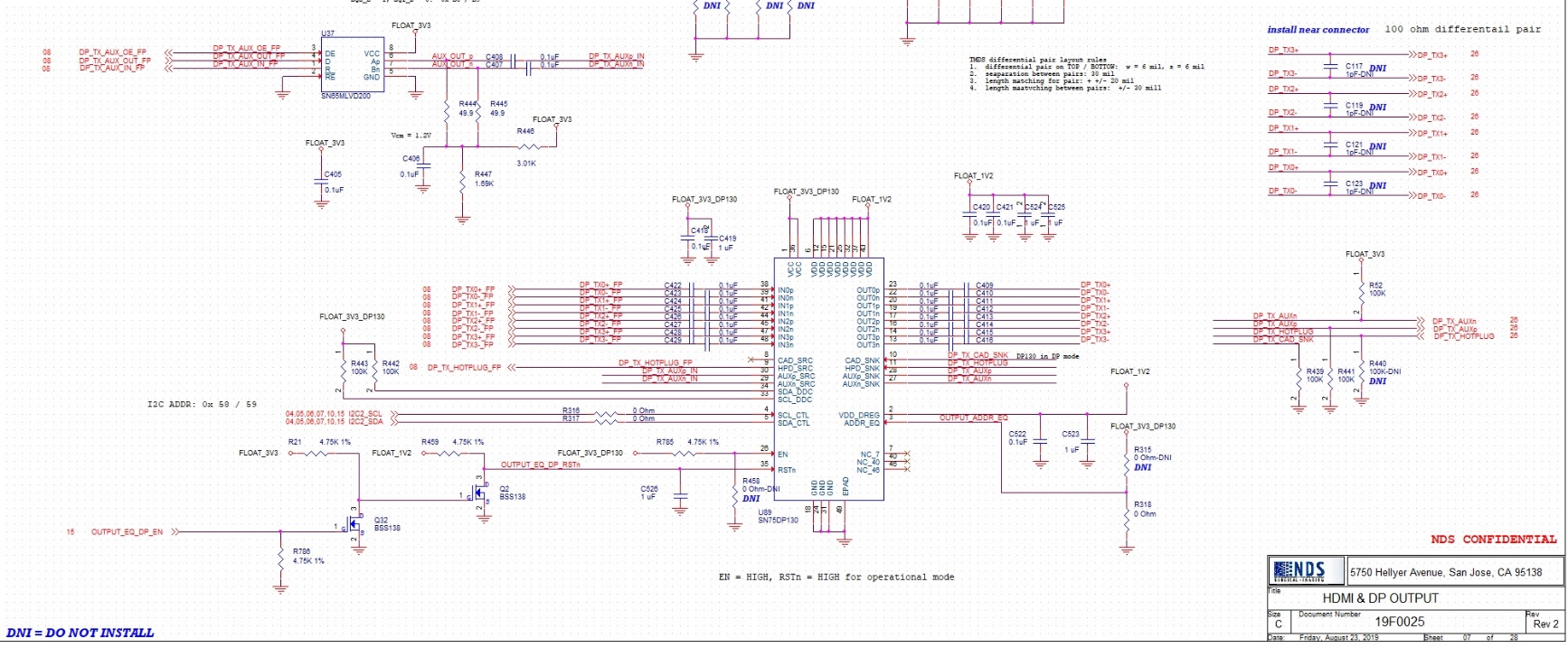


Figure 3: schematic of DP130 section – follow close to specs and application notes - Chip programming = default values

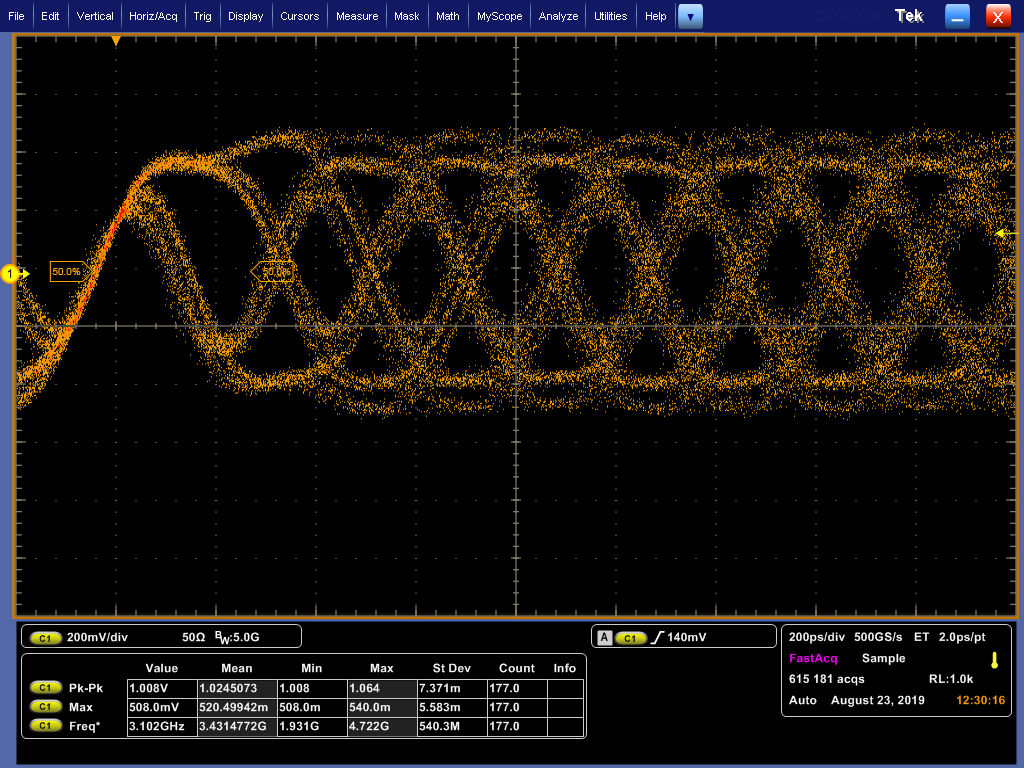


Figure 4: 5.4 Gb/s signal captured at input

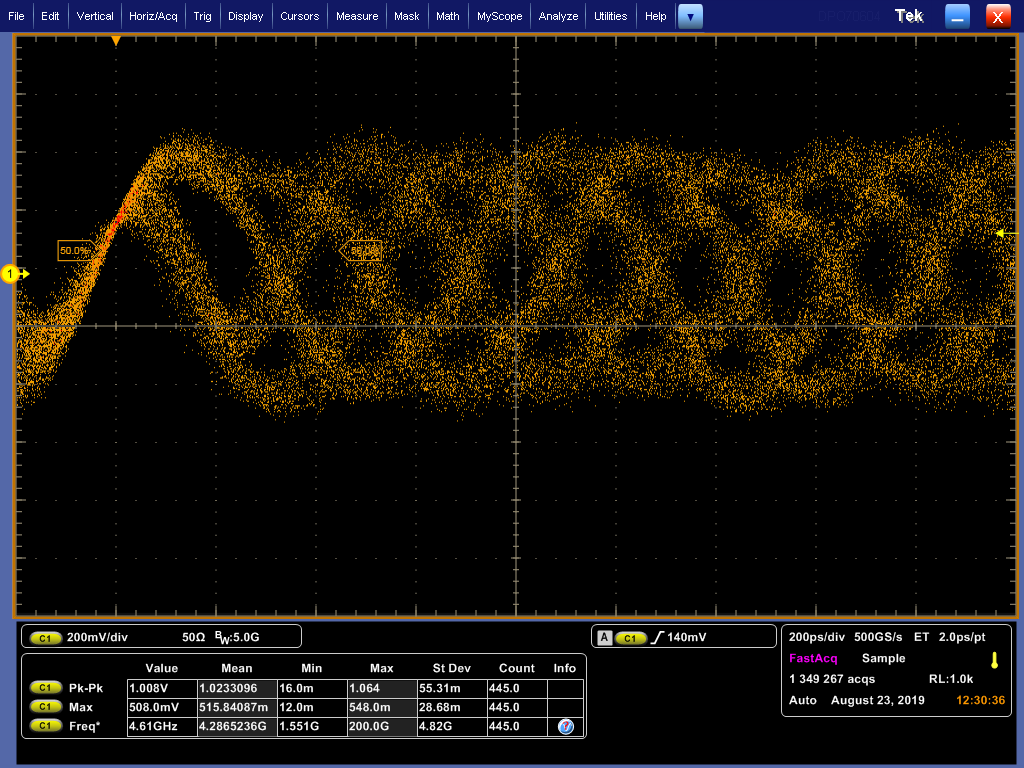


Figure 5: 5.4 Gb/s signal capture at output.

Question: why the output signal looks worse than the input signal? Anything we did wrong or we can improve the signal quality?