Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer L1	Copper	2.80mil		
4	Dielectric 1	FR-4 High Tg	6.00mil	4.6	
5	GND Plane L2	Copper	2.80mil		
6	Dielectric 2	FR-4 High Tg	6.00mil	4.6	
7	GND Plane L3	Copper	2.80mil		
8	Dielectric 3	FR-4 High Tg	5.00mil	4.6	
9	GND/Signal L4	Copper	2.80mil		
10	Dielectric 4	FR-4 High Tg	5.00mil	4.6	
11	GND Plane L5	Copper	2.80mil		
12	Dielectric 5	FR-4 High Tg	5.00mil	4.6	
13	GND Plane L6	Copper	2.80mil		
14	Dielectric 6	FR-4 High Tg	6.00mil	4.6	
15	GND Plane L7	Copper	2.80mil		
16	Dielectric 7	FR-4 High Tg	6.00mil	4.6	
17	Bottom Layer L8	Copper	2.80mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				

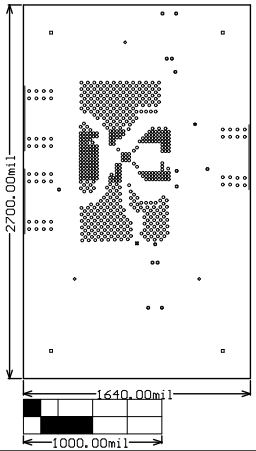
DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
○	594	7.87mil (0.200mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
⌖	14	10.00mil (0.254mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
☼	1	38.50mil (0.978mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
⊠	1	40.00mil (1.016mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
□	4	125.00mil (3.175mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
◇	3	270.00mil (6.858mm)	PTH	Round	Top Layer L1 - Bottom Layer L8	
	617 Total					

7.87mil (0.200mm) Holes L1 to L8 to be to be plugged with thermal/electrical conductive epoxy of manufacturers choice. Plugged vias to be plated after plugging to present flat surface to device U1 on L1 and H9 on L8, no potholes.

7.87mil (0.200mm) Holes L5 to L8 to be to be plugged with thermal/electrical conductive epoxy of manufacturers choice. Plugged vias to be plated after plugging to present flat surface to device H9, no potholes.

TEXAS INSTRUMENTS

PROJECT TITLE: OPA SINGLE (RGT) EVM
DESIGNED FOR: Public Release
FILE NAME: HSP006A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: HSP006	REV: A	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 7/24/2017 10:58:55 AM	TEXAS INSTRUMENTS	

ENGINEER:	LAYOUT BY:
Rohit Bhat	Bob Holtz
SCALE: 0.72	ALTIUM DESIGNER VERSION: 17.1.5.472