PWM Frequency Voltage Noise Cancellation in Three-Phase VSI Using the Novel SVPWM Strategy

Yingliang Huang, Yongxiang Xu, *Member, IEEE*, Yong Li, Guijie Yang, Jibin Zou, *Senior Member, IEEE*

***Abstract*—This paper has focused on the novel SVPWM strategy for the two-level three-phase inverter, which could eliminate the harmonics nearby PWM frequency. Ear-piercing high frequency electromagnetic noise from motor is common due to PWM technique. The proposed SVPWM is able to remove the high frequency harmonics located nearby the PWM frequency and other odd multiples by changing the original switching states. The unpleasant acoustic noise could be removed with the novel strategy whose PWM frequency is selected near 10 kHz. By comparison, it is near 20 kHz for conventional SVPWM to achieve the similar performance. Therefore, the switching losses are significantly reduced using the novel method. Furthermore, the proposed technique neither changes the characteristics of the fundamental wave nor employs the additional circuits in the drive. At last, the effectiveness of proposed strategy is verified by simulation and experiment.**

***Index Terms*—SVPWM, acoustic noise, harmonic suppression, motor drives, LC filter.**

I. INTRODUCTION

Space vector pulse-width modulation (SVPWM) is the most important PWM technique in motor drives because of excellent steady-state and dynamic performances [1]. However, the SVPWM sequence of pulses contains a useful base frequency and abundant high frequency harmonics. The set of high frequency harmonics are located nearby the carrier frequency and its multiples [2]. Nowadays, 2-20 kHz switching frequencies are common [3]. The range of human hearing generally from 20 Hz to 20 kHz overlaps with switching frequency. Ear-piercing high frequency electromagnetic vibration and noise could be produced by sideband harmonics whose frequency is less than 20 kHz [4]. In certain domestic and commercial areas, such as electric vehicles and elevators, the acceptability of drive system is tied strongly to the perceived sound levels resulting from their operation [4]. Acoustic comfort has become an increasingly important feature, as well as a way to comply with the IEC 60034-9 norm [5]. Thus, such unpleasant acoustic and electromagnetic vibration and noise caused by PWM is quite a common issue and should be addressed properly [4]-[14].

Generally, motor acoustic noise can be classified in two types. One type includes the aerodynamic and mechanical noise produced by the fan and bearings, respectively [6]. The other type of noise emitted by motors involves electro-magnetic acoustical noise [5]. This type of noise is produced by vibration force density wave according to

$$v(\alpha,t) = b^2(\alpha,t)/(2\mu_0)$$

where $b(\alpha,t)$ is the air-gap flux density harmonic components, and α is the angular position. t and μ_0 mean time and vacuum permeability, $4\pi\cdot10^{-7}$ H/m , respectively. This type of noise depends on the space harmonics and the time harmonics [6], [25]. Space harmonics are produced due to the nonlinearities that the flux density generates in the air gap, even with a sinusoidal power supply. Time harmonics appear when the motor is fed by a power inverter due to voltage harmonics with the fundamental voltage [5]. The stator magnetomotive force (MMF) harmonics due to PWM harmonics in stator currents have magnitudes and frequencies which vary depending on the PWM strategy used. The PWM technique has a direct impact on torque ripple, heating in coils, vibrations, and mechanical noise [6].

Many researchers have attempted to reduce electromagnetically induced acoustic noise due to time harmonics [2]-[14]. A well-researched approach to spread the acoustic noise spectrum is to employ random pulse width modulation (RPWM) [8], [10], [11]. The carrier frequency is modulated by a pseudorandom code [8]. This technique spreads power of noise over a wide range of frequency domain compared with the conventional SVPWM with fixed switching frequency [10]. The effects on reducing electromagnetic noise

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of the triangular periodic carrier frequency modulation (PCFM) [14] are similar to RPWM. However, the human hearing acoustic noise still exits and the level of noise maybe not acceptable in some applications. In addition, this method may excite the system resonant frequencies, which increases the acoustic noise and vibration [11]. The greatest amount of magnetic noise in the motor occurs at frequencies close to the natural mechanical frequencies of the stator system. [5], [6] optimize the inverter behavior in order to reduce the total harmonic distortion (THD) and acoustic noise by using the HIPWM-FMTC strategy or SLPWM strategy.

Using LC output filters between VSI and motor is another particularly effective approach to reduce the amplitude of the switching ripple, make the voltage on the motor terminals sinusoidal [15] and reduce the acoustic noise without requiring modification of the carrier frequency [5]. For the design of LC output filter, the resonance frequency of filter is considered of the output voltage waveform [16]. In order to achieve an almost sinusoidal motor voltage, the resonance frequency of the filter has to be well below the lowest harmonic frequency of the inverter voltage resulting from pulse width modulation. To avoid additional resonance suppressing control, the resonance frequency has also to be well above the fundamental frequency of the inverter voltage [17-19]. A rule of thumb in control theory is that the frequencies of such a configuration have to have at least a factor of 10 between them to decouple the effects. According to this rule, for 60 Hz fundamental frequency, resonance frequency has to be at least 600 Hz, and switching frequency of the inverter output has to be at least 6000 Hz [17]. In other words, the resonance frequency of filter is influenced by switching frequency of VSI. Therefore, the performance, size and cost of LC filter strongly depend on the switching frequency [17-21]. However, due to its large inductance and capacitance values, the filter will be large in size, which limits the applications of LC filter [18].

These publications do much work in filters and make important contribution to power electronics and electrical noise. If the inverter can operate with near 20 kHz switching frequency, the effects of the time harmonics will be minimal because the current harmonics are attenuated by the inductive circuit of the motor [5]. However, the switching frequency of VSI is severely restricted to mitigate switching losses. In this paper, a new SVPWM method has been proposed to shift the first switching harmonic to the twice original switching frequency for a two-level three-phase VSI with only increasing 33% switching losses. By using this strategy, the actual switching frequency can be selected near 13 kHz, and the frequency of voltage harmonic is near 20 kHz, which is beyond the human hearing range. The annoying whine that the motor produces can be removed by eliminating distinct tones in the applied voltage. Moreover, for the applications with LC output filters, the smaller filter components could be used because of the increase of actual switching harmonics.

The rest of this paper is organized as follows. The conventional SVPWM and PCFM are listed in Section II in order to compare with the proposed strategy. Then, the proposed SVPWM technique is discussed in Section III, which includes the implementation of the proposed strategy using program, the influences of modulation ratio and carrier-modulating frequency ratio. The noise investigation in SVPWM, PCFM and the proposed SVPWM are shown in Section IV. Experiments are carried out on a 0.75 kW PMSM using digital signal processor (DSP) control board in Section V. Finally, concluding remarks are presented in Section VI.

II. Review Of The Conventional SVPWM and PCFM

A. The conventional SVPWM

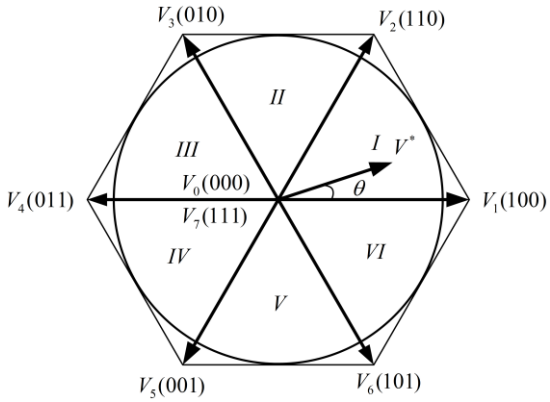

Fig. 1. Space vector diagram.

As shown in Fig. 1, the vector space is divided into eight possible voltage vectors which consist of two zero vectors (V_0 and V_7) and six active vectors ($V_1 - V_6$). With respect to V^* position, which is located in sector I, two active vectors V_1 and V_2 are applied to the two-level three-phase VSI.

The adjacent clockwise and counter-clockwise vectors of V^* and the zero vectors are applied for the percentage time of T_1, T_2, and $T_{0,7}$, which are given in (1)-(3), over the switching period T_s, respectively

$$T_1 = mT_s \sin(\frac{\pi}{3} - \theta) \tag{1}$$

$$T_2 = mT_s \sin\theta \tag{2}$$

$$T_{0,7} = T_s - T_1 - T_2 \tag{3}$$

where m is modulation ratio of SVPWM and $m = \frac{\sqrt{3}}{v_{dc}}\left|V^*\right|$. θ is the rotating angle of V^* with respect to its adjacent clockwise vector, and v_{dc} is the voltage of DC-link [22-24].

Generally, the duration of zero vectors T_0 and T_7 are equal, and both V_0 and V_7 are used in each switching cycle for SVPWM. Fig. 2(a) shows the switching pulse pattern in the SVPWM technique when V^* is located in Sector I. The power switches are considered as ideal switches. The minimum pulse width and dead-time are ignored. s_a, s_b, s_c are the switching states. High voltage level indicates the upper switch is on and lower switch in the same arm is off. Low voltage level indicates

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the lower switch is on and upper switch in the same arm is off. The active vectors V_1 and V_2 are symmetric about V_7, which is shown more clearly in Fig. 2(b). As shown in Fig. 2(c), the three-phase voltages are also symmetric about V_7 due to the symmetry of switching states for SVPWM technique.

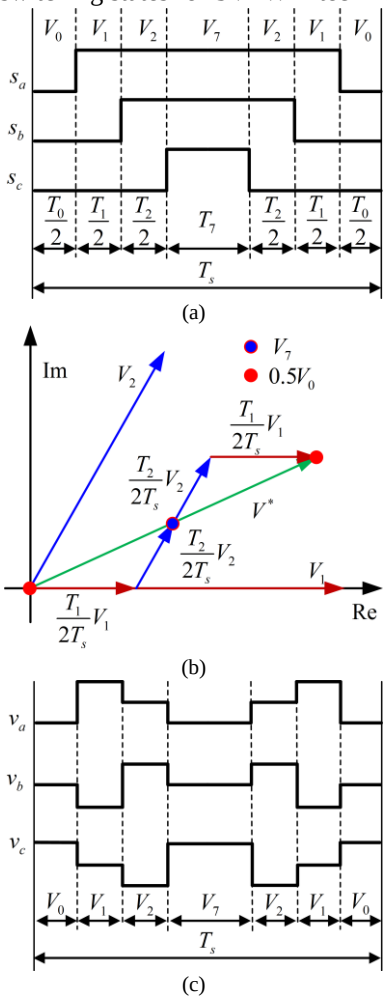

Fig. 2. Conventional SVPWM (a) Switching states, (b) Composition of vector V^*, (c) Three-phase voltages when V^* located at sector I.

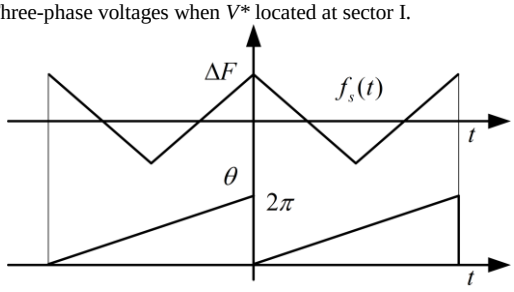

Fig. 3. The schematic of triangular PCMF.

B. *The review of PCFM*

The PWM frequency of conventional SVPWM is constant, whereas that of PCFM is variable [1], [14]. The instantaneous PWM frequency of PCFM is defined as

$$f_a(t) = f_s + f_s(t) \tag{4}$$

where f_s is the nominal PWM frequency of conventional SVPWM, and $f_s(t)$ is the periodic carrier function, such as triangular function, sawtooth function or random function (RPWM).

Fig. 3 shows the $f_s(t)$ of triangular PCFM. In general, the period of periodic carrier function $f_s(t)$ is equal to the period of fundamental wave T_0. ΔF, the amplitude of $f_s(t)$, is defined as

$$f_s(t) = \begin{cases} \Delta F + \dfrac{4\Delta F t}{T_0} & (-\dfrac{T_0}{2} \le t \le 0) \\ \Delta F - \dfrac{4\Delta F t}{T_0} & (0 \le t \le \dfrac{T_0}{2}) \end{cases} \tag{5}$$

If PWM frequency is from 4 kHz to 6 kHz, fundamental frequency is 50 Hz and the nominal PWM frequency is 5 kHz, the instantaneous PWM frequency of triangular PCFM is $f_a(t) = \begin{cases} 2000(3+100t) & (-0.01 \le t \le 0) \\ 2000(3-100t) & (0 \le t \le 0.01) \end{cases}$.

III. The Proposed SVPWM

SVPWM has several advantages over the other PWM techniques, such as low THD and implementation simplicity. The last advantage is very important when the performance of micro controller unit (MCU) was low. Nowadays, the development of field programmable gate array (FPGA) and MCU make it possible to achieve more excellent and complex SVPWM technique.

A. *Introduction of the novel SVPWM*

As mentioned in the Section II, the switching states of SVPWM are symmetric about zero vectors. The switching functions, composition of vector and three-phase voltages of the novel SVPWM are shown in Fig. 4. As shown in Fig. 4(a), the sequence of V_1 and V_2 are exchanged. Compared with the conventional SVPWM technique, the components of V^* are asymmetric about V_7. Therefore, in each switching cycle, V_1 and V_2 are applied twice in order, which is illustrated clearly in Fig. 4(b). Fig. 4(c) shows the waveforms of three phase voltages, where the waveform 1 is the same as waveform 2. Thus, the phase voltage meets

$$v(t + 0.5T_s) = v(t) \tag{6}$$

where T_s is the PWM cycle. The minimum period of $v(t)$ is $0.5T_s$. The harmonics frequency of $v(t)$ is

$$n\frac{1}{0.5T_s} = \frac{2n}{T_s} = 2nf_s \tag{7}$$

where $n = 1, 2, 3...$, f_s is the PWM frequency. For the proposed SVPWM, the high frequency voltage harmonics are located nearby $2f_s, 4f_s, 6f_s, \ldots$

As seen in Fig. 4(a), in a PWM cycle, the phase-B arm is operated twice and phase-A and phase-C arm are operated once. For the proposed strategy, switching operations is 4 times, whereas 3 times for conventional SVPWM technique in a PWM cycle. In other words, the price of reducing odd multiples

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harmonics is increasing 33% switching losses.

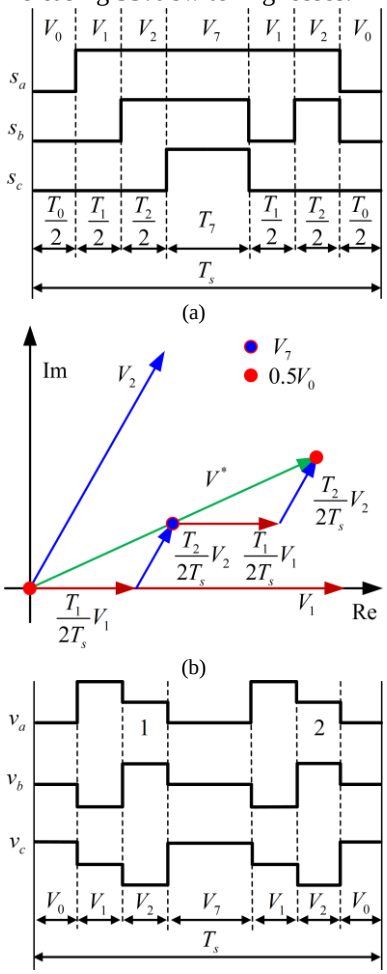

Fig. 4. (a) The proposed SVPWM (a) Switching states, (b) Composition of vector *V**, (c) Three-phase voltages when *V** located at sector I.

B. Implementation of the novel SVPWM

TABLE I The comparison of SVPWM and the proposed SVPWM

Sector	MS State	SVPWM	Proposed SVPWM
I	s_b	$V_1\ V_2\ V_7\ V_2\ V_1$	$V_1\ V_2\ V_7\ V_1\ V_2$
II	s_a	$V_2\ V_3\ V_7\ V_3\ V_2$	$V_2\ V_3\ V_7\ V_2\ V_3$
III	s_c	$V_3\ V_4\ V_7\ V_4\ V_3$	$V_3\ V_4\ V_7\ V_3\ V_4$
IV	s_b	$V_4\ V_5\ V_7\ V_5\ V_4$	$V_4\ V_5\ V_7\ V_4\ V_5$
V	s_a	$V_5\ V_6\ V_7\ V_6\ V_5$	$V_5\ V_6\ V_7\ V_5\ V_6$
VI	s_c	$V_6\ V_1\ V_7\ V_1\ V_6$	$V_6\ V_1\ V_7\ V_6\ V_1$

In this paper, the switching state function different from conventional SVPWM, as s_b shown in Fig. 4(a), is called modified switching state function (MS State). In each cycle of the proposed SVPWM, there are two conventional switching state functions and one modified switching state function. The comparison of the proposed SVPWM is shown in TABLE I. For instance, if V^* is located in sector III, the switching state functions s_a and s_b are the same as conventional SVPWM. The modified switching state function s_c is $V_3\ V_4\ V_7\ V_3\ V_4$, which is different from $V_3\ V_4\ V_7\ V_4\ V_3$ in SVPWM. The proposed strategy could be achieved easily with MCU, or FPGA according to the logic in TABLE I.

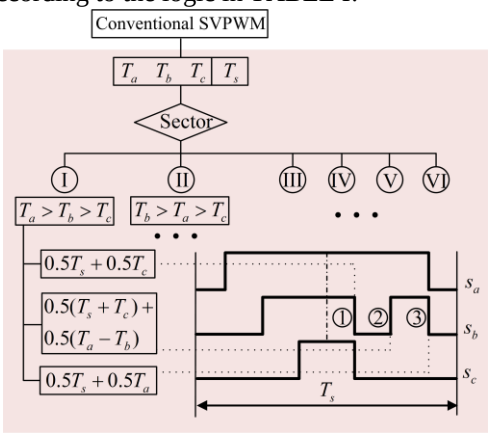

Fig. 5. The implementation of the proposed SVPWM with program.

The implementation of the proposed SVPWM with program in MCU or DSP is shown in Fig. 5. In order to implement the conventional SVPWM technique, the PWM period T_s and the durations of three phases on-time T_a, T_b and T_c should be calculated. The sector could be obtained by comparing the values of T_a, T_b and T_c. If $T_a > T_b > T_c$, V^* is located in sector I. The 3 special points marked as ①, ② and ③ in Fig. 5 are calculated by $0.5(T_s + T_c)$, $0.5(T_s + T_c) + 0.5(T_a - T_b)$ and $0.5(T_s + T_a)$ respectively. The switching functions s_a and s_c are the same as conventional SVPWM. The modified switching state function s_b changes to low level at point ① with s_c, then high level at point ②, at last low level with s_a. When V^* is located in anyone of other 5 sectors, the special 3 points could be calculated in the same way, which are listed in TABLE II. The proposed strategy could be achieved easily with switch-case function and the computational burden is light for present MCU or DSP.

TABLE II
Implementation of the proposed SVPWM

Sector	Condition	Point ①	Point ②	Point ③
I	$T_a > T_b > T_c$	$0.5(T_s + T_c)$	$0.5(T_s + T_a + T_c - T_b)$	$0.5(T_s + T_a)$
II	$T_b > T_a > T_c$	$0.5(T_s + T_c)$	$0.5(T_s + T_b + T_c - T_a)$	$0.5(T_s + T_b)$
III	$T_b > T_c > T_a$	$0.5(T_s + T_a)$	$0.5(T_s + T_a + T_b - T_c)$	$0.5(T_s + T_b)$
IV	$T_c > T_b > T_a$	$0.5(T_s + T_a)$	$0.5(T_s + T_a + T_c - T_b)$	$0.5(T_s + T_c)$
V	$T_c > T_a > T_b$	$0.5(T_s + T_b)$	$0.5(T_s + T_b + T_c - T_a)$	$0.5(T_s + T_c)$
VI	$T_a > T_c > T_b$	$0.5(T_s + T_b)$	$0.5(T_s + T_a + T_b - T_c)$	$0.5(T_s + T_a)$

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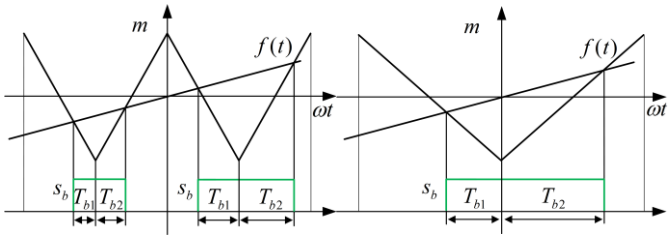

Fig. 6. Asymmetrical regular sampled SVPWM (a) c_f is large, (b) c_f is small.

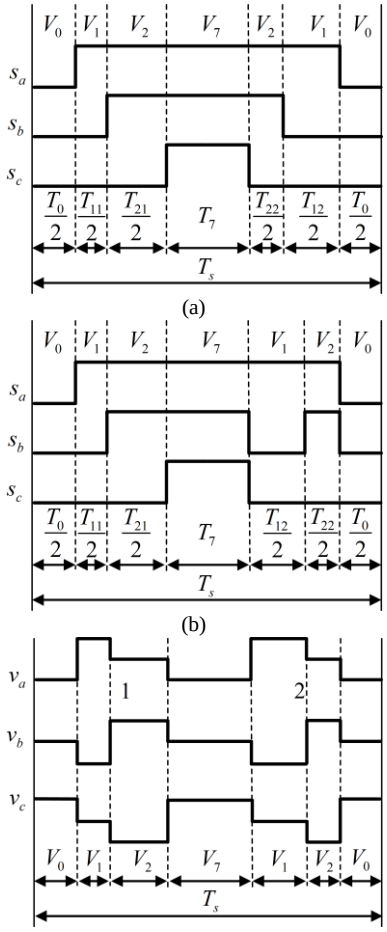

Fig. 7. (a) Switching states of conventional SVPWM, (b) Switching states of the proposed SVPWM, (c) Waveforms of three-phase voltages using the proposed SVPWM.

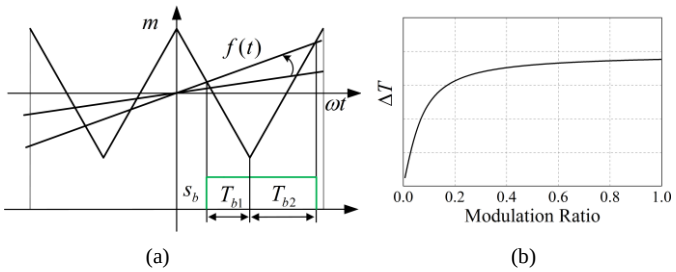

Fig. 8. (a) Asymmetrical regular sampled SVPWM with changing c_f, (b) The relationship between ΔT and modulation ratio.

C. The influence of carrier-modulating frequency ratio on the proposed SVPWM

The modulation model of asymmetrical regular sampled SVPWM is shown in Fig. 6, where $f(t)$ is the modulation wave of phase-B. The switching state s_b depends on the value of $f(t)$ at the midpoint of each PWM cycle. If carrier-modulating frequency ratio c_f is large enough, the duration of switching state before each midpoint marked as T_{b1} will be almost equal to the duration of behind midpoint marked as T_{b2}, as shown in Fig. 6(a). However, Fig. 6(b) shows that if the motor speed is relatively high or the PWM frequency is rather low, which means that c_f is small enough, the difference of durations between T_{b1} and T_{b2} will be obvious. The difference is defined by $\Delta T = T_{b1} - T_{b2}$. ΔT will influence the effect of PWM frequency voltage harmonic cancellation for the proposed SVPWM. The reasons are analyzed as follows.

When c_f is small enough, the switching states of conventional SVPWM are shown in Fig. 7(a). The duration of V_1 and V_2 is T_{11}, T_{12} and T_{21}, T_{22} respectively, and $T_{11} < T_{12}$, $T_{21} > T_{22}$. The corresponding switching states of the proposed SVPWM are shown in Fig. 7 (b). Fig. 7(c) shows the waveforms of phase voltages with the proposed SVPWM and demonstrates the waveform 1 and waveform 2 are not congruous compared with them in figure 4c. Thus, the PWM frequency harmonics exist in phase voltage sequence based on Fourier series analysis. The larger the difference ΔT is, the higher PWM frequency harmonics content in phase voltage becomes. It is clear that the harmonic content located nearby the PWM frequency will increase with the decrease of carrier-modulating frequency ratio.

D. The influence of modulation ratio on the proposed SVPWM

The influence of modulation ratio on the proposed SVPWM is similar to the cases of carrier-modulating frequency ratio. As shown in Fig. 8(a), the slope of modulation wave $f(t)$ increases with the increase of modulation ratio. The difference of durations ΔT will vary with the slot of $f(t)$. The relationship between ΔT and modulation ratio is shown in Fig. 8(b). As seen in the figure, the increase trend of ΔT becomes slow with the modulation ratio. Thus, the PWM frequency harmonic will increase with the increase of modulation ratio for the proposed SVPWM when modulation ratio is less than 0.6. When modulation ratio is larger than 0.6, the PWM frequency harmonic content basically remains unchanged.

IV. The Noise Investigation in SVPWM, PCFM and the Proposed SVPWM

As mentioned in the Section II, the switching states of conventional SVPWM are symmetric about zero vectors. Consequently, SVPWM has low THD. PCFM reduces the noise by changing the PWM frequency as a particular function, and could be easily implemented compared with RPWM. This section mainly evaluates the capability of noise reduction near

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PWM frequency for SVPWM, triangular PCFM and the proposed SVPWM. The sampling frequency of phase voltage is 125 kHz, and the FFT resolution is 10 Hz.

Fig. 9 shows power spectral density (PSD) of phase voltage using the conventional SVPWM, PCFM and the proposed method respectively. The PWM frequency is 3 kHz for SVPWM. For the proposed SVPWM, the actual switching frequency is equal to 4 kHz. 2.5 kHz to 3.5 kHz has been selected for triangular PCFM, so the average of switching frequency is equal to 3 kHz. The fundament component, carrier-modulating frequency ratio and modulation ratio for the three methods is equal to 50Hz, 60 and 0.8 respectively.

As seen in Fig. 9(a), for the conventional SVPWM, the set of high frequency harmonics are located nearby the PWM frequency and its multiples. The PSD of PWM frequency harmonic is rather high in 3 kHz. The results of PCFM are shown in Fig. 9(b), the PSD of PWM frequency is distributed relatively equally throughout 2.5 kHz to 3.5 kHz. Compared with the results of conventional SVPWM marked by solid line, the lower level of harmonics near PWM frequency based on PCFM-based methods indicates that they have better effects on noise elimination. However, the noise near PWM frequency is still obvious and unacceptable in some applications.

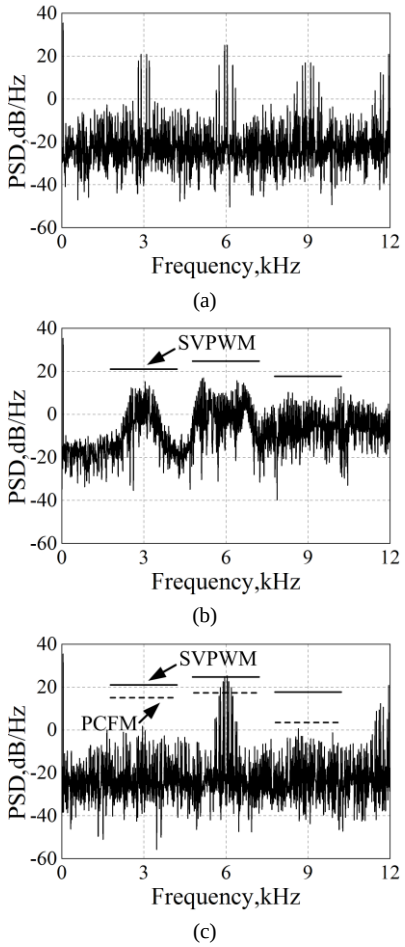


Fig. 9. (a) PSD of phase voltage with (a) SVPWM, (b) PCFM, (c) proposed SVPWM when carrier-modulating frequency ratio is 60 and modulation ratio is 0.8.

Fig. 9(c) shows the PSD of the proposed method and marks the PSD levels of SVPWM and PCFM near PWM frequency. Compared with the results of conventional SVPWM and PCFM, the PWM frequency voltage noise cancellation of the proposed SVPWM is very remarkable.

The FFT results of three methods when carrier-modulating frequency ratio is equal to 60 and modulation ratio is equal to 0.8 are discussed above. In fact, the components of PWM frequency harmonics are relevant to the carrier-modulating frequency ratio and modulation ratio, which is discussed in Section III. In order to compare the effects of the proposed SVPWM on PWM frequency voltage noise elimination with PCFM comprehensively, the amplitudes of PWM frequency harmonic varying with different modulation ratios and carrier-modulating frequency ratio respectively are simulated in the following.

Fig. 10(a) shows the amplitudes of PWM frequency(3 kHz) phase voltage noise for SVPWM, PCFM and the proposed SVPWM when modulation ratio varies from 0.3 to 0.9. The fundamental frequency is equal to 50Hz and carrier-modulating frequency ratio is equal to 60. The amplitudes of PWM frequency noise using SVPWM or PCFM increase with the increase of modulation ratio. For the proposed SVPWM, the amplitude increases with modulation ratio when modulation ratio is less than 0.6. By contrast, when modulation ratio is larger than 0.6, the amplitude basically remains unchanged. For the three methods, the amplitude of PWM frequency noise using PCFM is lower than SVPWM and that using the proposed SVPWM is the lowest in different modulation ratios.

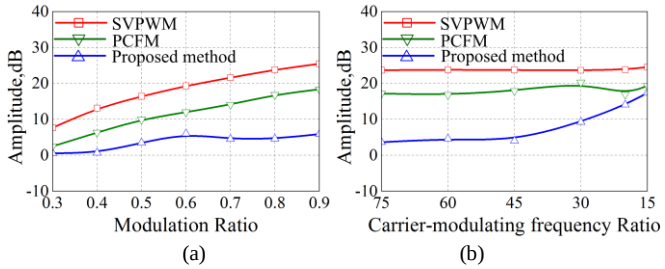


Fig. 10. The PWM frequency harmonics amplitude of phase voltage varies with (a) different modulation ratios when carrier-modulating frequency ratio is 60, (b) different carrier-modulating frequency ratios when modulation ratio is 0.8.

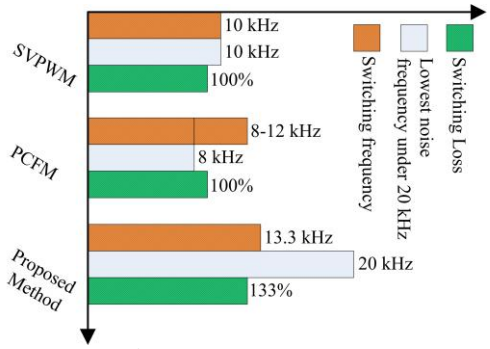


Fig. 11. The comparison of SVPWM, PCFM and the proposed SVPWM.

Fig. 10(b) shows the amplitude of PWM frequency phase voltage noise using these three techniques when carrier-modulating frequency ratio varies from 75 to 15. The fundamental frequency is equal to 50Hz and modulation ratio is equal to 0.8. The amplitude of PWM frequency noise using the

proposed SVPWM is still the lowest of these techniques. For the proposed SVPWM, the noise amplitude keeps in rather low level when carrier-modulating frequency ratio is more than 45. If the carrier-modulating frequency ratio is less than 45, the amplitude will increase. The noise amplitude using the proposed SVPWM is close to that using PCFM when carrier-modulating frequency ratio is equal to 15. For better effects on PWM frequency noise elimination, it is recommended that the carrier-modulating frequency ratio is more than 30.

The results in PWM frequency voltage noise cancellation using these three methods with different carrier-modulating frequency ratios and modulation ratios are shown above. Fig. 11 involves the comparison of the switching loss for SVPWM, PCFM and the proposed SVPWM. When PWM frequency is equal to 10 kHz, the switching loss of SVPWM is defined 100%. For SVPWM in 10 kHz PWM frequency, the frequency of the lowest PWM harmonics is near 10 kHz which is in the range of human hearing and whose amplitude is high. For triangular PCFM, the switching frequency varies from 8 kHz to 12 kHz, the average of which is equal to 10 kHz. The frequency of the lowest PWM harmonics is near 8 kHz and its amplitude is lower than SVPWM. However, the level of ear-piercing noises in 8 kHz to 12 kHz is rather high and still unacceptable in some applications. The PWM frequency is equal to 10 kHz for the proposed SVPWM, and the actual switching frequency is 13.3 kHz due to the additional switching action in each PWM cycle. For this method, the voltage harmonics near PWM frequency are basically removed. Thus, the frequency of the lowest PWM harmonics is near 20 kHz, which is beyond the range of human hearing, and the amplitude of noise is very low. Moreover, because the actual switching frequency is equal to 13.3 kHz, the switching losses are 133%. As a consequence, the proposed method has the global optimum performance in PWM frequency voltage cancellation and switching losses reduction in these three methods.

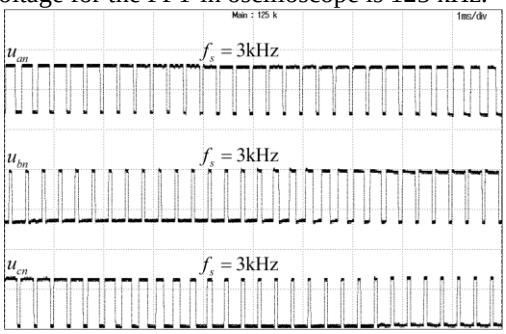
V. Experimental Verification

TABLE III
Specification and Parameter of System

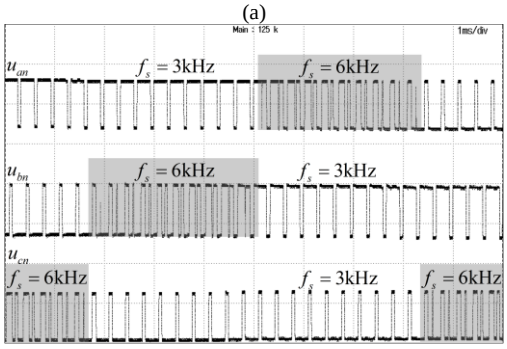
Specification and Parameter	Value
Phase Resistance	0.7464 Ω
Phase Inductance	3.98 mH
Back-EMF Coefficient	55.80 V/krpm
Pole Pairs	5
Rated Load	2.5 N.m
PWM frequency	3000 Hz
Load	2.0 N.m

In this section, a three-phase VSI has been implemented to verify the effectiveness of proposed SVPWM strategy in removing voltage noise located nearby the PWM frequency practically. For showing the advantages of the proposed strategy, the experimental results of SVPWM technique and PCFM are shown as well. The specification and parameters of drive system are shown in TABLE III. As seen in this table, PWM frequency of VSI is 3 kHz which is rather low compared with common VSI, because lower switching frequency could reduce the demands of measuring instrument (High voltage differential probe and oscilloscope).

In the following results, the fundamental frequency is equal to 50Hz, carrier-modulating frequency ratio is equal to 60 and modulation ratio is equal to 0.65. The sampling frequency of phase voltage for the FFT in oscilloscope is 125 kHz.

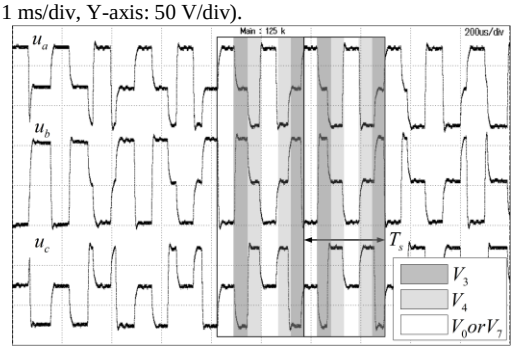


(a)

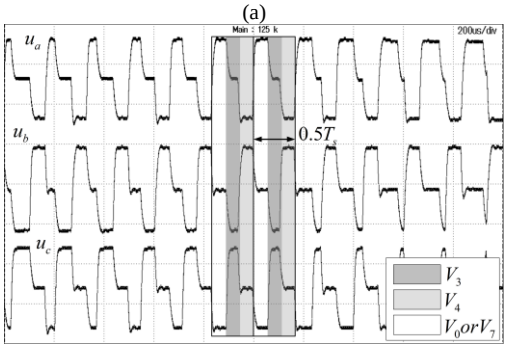


(b)

Fig. 12. The pole voltages using (a) SVPWM, (b) the proposed SVPWM (X-axis: 1 ms/div, Y-axis: 50 V/div).



(a)



(b)

Fig. 13. Three phase voltages using (a) SVPWM, (b) the proposed SVPWM (X-axis: 200μs/div, Y-axis: 20 V/div).

Fig. 12 shows the switching loss comparison of three phase pole voltages using SVPWM and the proposed method. For conventional SVPWM shown in Fig. 12(a), the switching frequency of all switches is always 3 kHz. Fig. 12(b) illustrates

pole voltages using the proposed SVPWM. At any time, the switching frequency of one phase pole voltage is 6 kHz and that of other two phase pole voltages is 3 kHz. In other words, one arm is operated at 6 kHz and other two arms are operated at 3 kHz. The actual switching frequency is

$$\frac{1\times 6\text{kHz}+2\times 3\text{kHz}}{3}=4\text{kHz}\ .$$

Thus, at the same PWM frequency, the switching loss of the proposed method is 133% of conventional SVPWM.

In the following section, three phase voltage and their harmonics spectra using SVPWM and the proposed method are shown respectively. Three phase voltages using SVPWM is shown in Fig. 13(a). In a switching cycle the sequence of applied vectors is $V_0V_3V_4V_0V_4V_3$. The period of each waveform is one switching cycle T_s. Fig. 13(b) shows three phase voltages using the proposed method. Compared with SVPWM, the sequence of applied vectors is $V_0V_3V_4-V_0V_3V_4$ and the period of each waveform is 0.5 switching cycle. Therefore, the PWM harmonics frequencies of phase voltage using the proposed method are twice as that using SVPWM.

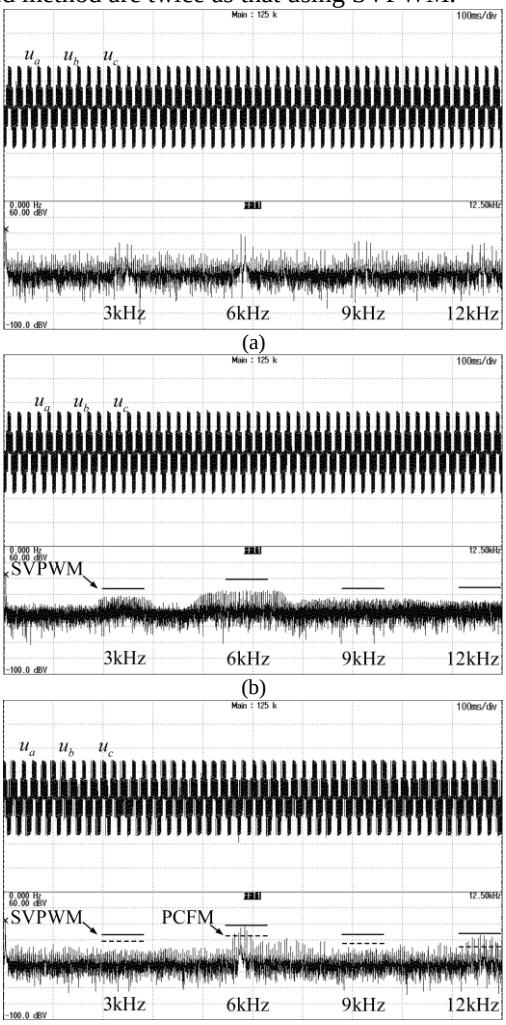


Fig. 14. The harmonics spectrum of phase voltage using (a) SVPWM, (b) PCFM, (c) the proposed SVPWM (X-axis: 1.25 kHz/div, Y-axis: 20 dBV/div).

Fig. 14(a) illustrates the harmonics spectrum of phase voltage using SVPWM. As aforementioned, PWM frequency is equal to 3 kHz, and harmonics concentrates on 3 kHz and its multiples. The results of triangular PCFM whose switching frequency ranges from 2.5 kHz to 3.5 kHz are shown in Fig. 14(b). The average switching frequency is equal to 3 kHz. As seen in this figure, the amplitudes of PWM frequency harmonics are almost flat and lower than that using SVPWM. Fig. 14(c) demonstrates the amplitudes of the harmonics spectrum of phase voltage using the proposed method. The PWM frequency is equal to 3 kHz and actual switching frequency is equal to 4 kHz. In order to compare the amplitudes of PWM frequency harmonics using these three methods, the harmonics levels of SVPWM and PCFM are marked in Fig. 14(c). The amplitudes of PWM frequency harmonics are much lower than that of other two methods. There are no obvious voltage noises less than the double PWM frequency (6 kHz). The experiment results confirm that the proposed method could eliminate the PWM frequency voltage noise, as the results obtained from analysis and simulation.

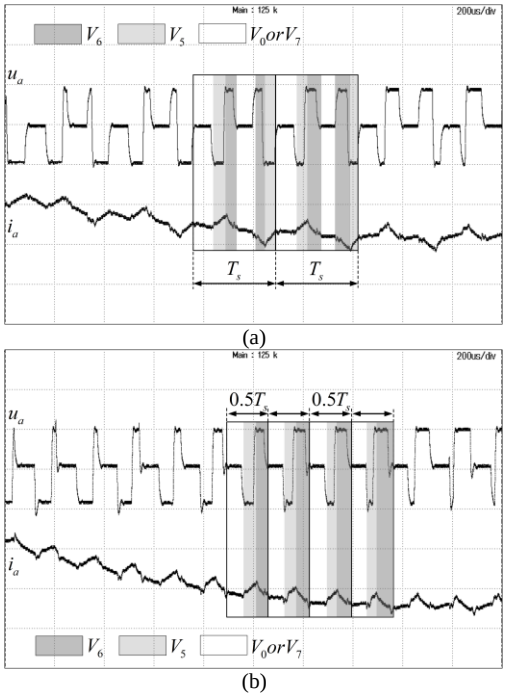


Fig. 15. Phase-A voltage and phase-A current using (a) SVPWM, (b) the proposed SVPWM (X-axis: 200μs/div, Y-axis: 20 V/div).

In power electronics and their loads, current components cause acoustic noise. In terms of acoustic noise, the current amplitude in each frequency component is important [11]. Therefore, the phase current harmonics cancellation are analyzed and shown in the following part to further illustrate the proposed strategy. The corresponding relation of phase current and phase voltage using SVPWM is shown in Fig. 15(a), and the case using the proposed strategy is shown in Fig. 15(b). Similar to the phase voltage above, the sequence of applied vectors is $V_0V_5V_6V_0V_6V_5$ in a switching cycle. The period of phase voltage and phase current waveforms is one switching cycle T_s. Compared with SVPWM, the sequence of applied

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vectors is $V_0V_5V_6 - V_0V_5V_6$ and the period of each waveform is 0.5 switching cycle. Thus, the PWM harmonics frequencies of phase current using the proposed method are twice as that using SVPWM. The harmonics spectrum of phase current using SVPWM and the proposed method is shown in Fig. 16(a) and Fig. 16(b) respectively. The amplitudes of PWM frequency harmonics using SVPWM and PCFM are marked in Fig. 16(b). In comparison with these two methods, the levels of PWM frequency harmonics using the proposed method are much lower. The PWM frequency harmonics of phase current are reduced significantly by the proposed method.

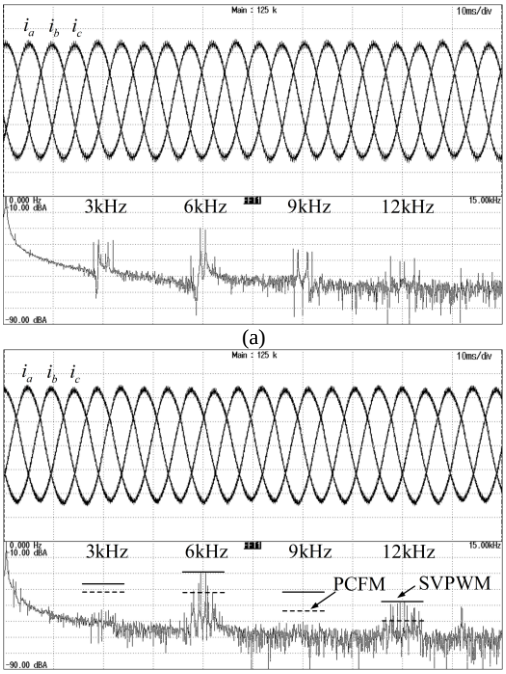

Fig. 16. The harmonics spectrum of phase current using (a) SVPWM, (b) the proposed SVPWM (X-axis: 1.50 kHz/div, Y-axis: 10 dBV/div).

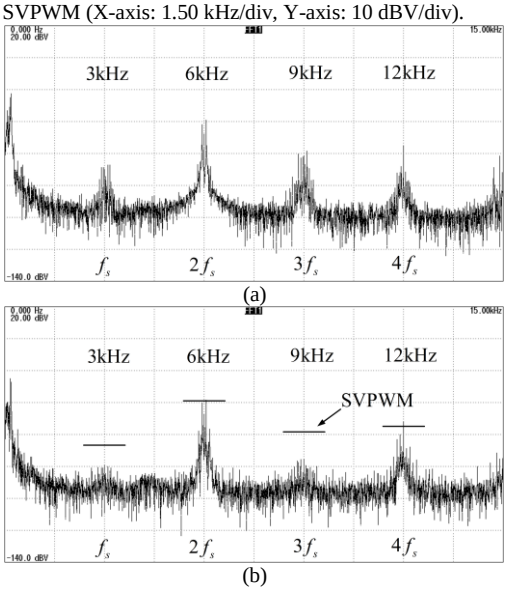

Fig. 17. The noise spectrum using (a) SVPWM, (b) the proposed SVPWM (X-axis: 1.50 kHz/div, Y-axis: 20 dBV/div).

The PWM technique has a direct impact on vibrations and mechanical noise [6]. When the PWM frequency noise are cancelled from phase voltages and phase currents, this frequency acoustic noise could almost be removed. The acoustic noise of motor is measured by a MEMS microphone and the frequency spectrum using SVPWM and the proposed method is shown in Fig. 17(a) and Fig. 17(b) respectively. Compared with the results using SVPWM, the PWM frequency acoustic noises are almost be removed by the proposed method, which verifies the effectiveness of proposed strategy in removing the PWM frequency noise.

VI. Conclusion

This paper has proposed a novel SVPWM strategy for two-level three-phase VSI. The proposed strategy is designed by changing the original switching state functions of conventional SVPWM to cancel the PWM frequency voltage noise and current noise at the expense of increase 33% switching frequency only. Consequently, the proposed method plays an important role in decreasing ear-piercing vibration and unpleasant acoustic noise, improving the performance of LC filters and reducing their cost and size. In this paper, the influence of modulation ratio and carrier-modulating ratio on the proposed method is studied and the implementation of the method by program on MCU or DSP is shown. In addition, the effects on PWM frequency voltage noise elimination using SVPWM, PCFM and the proposed method are compared. The proposed method could significantly reduce PWM frequency voltage noise with the minimum switching loss. Moreover, the recommended carrier-modulating ratio is more than 30 to take full advantage of the method. Simulations and experimental results verify the effectiveness of the proposed method. In fact, the proposed method can be used not only in motor drive applications, but also in grid-connected inverter system to reduce the size of output filter inductors.

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