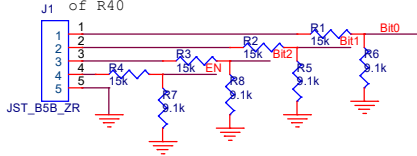
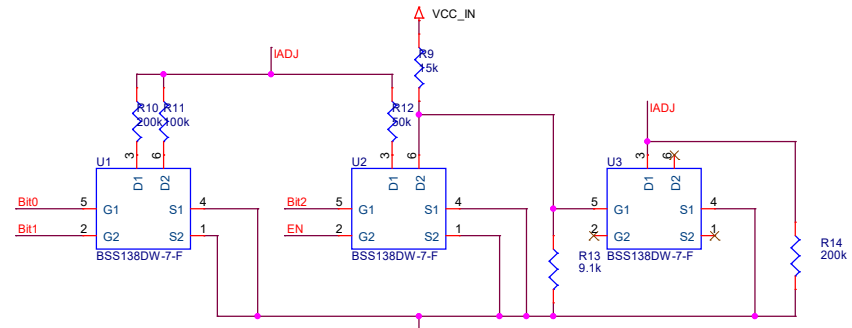


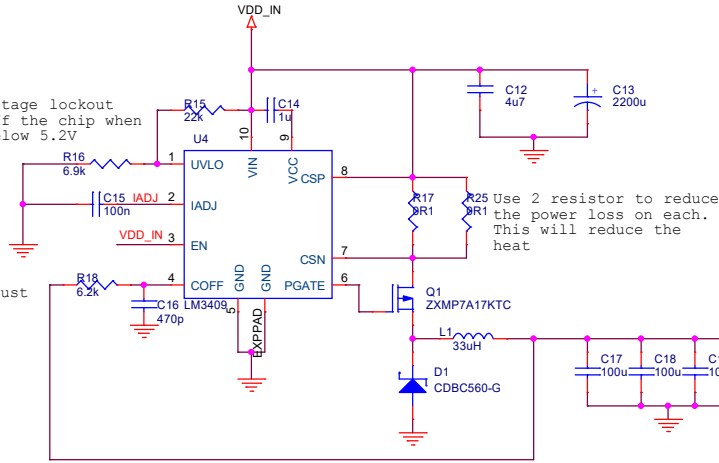
DN: This JST connector will be connect to a connector which is located at the housing of R40



These vottage divider are used to generate a max. voltage of 9V between Gate and Source. Because the max. Gate to Source Voltage is +/- 20V

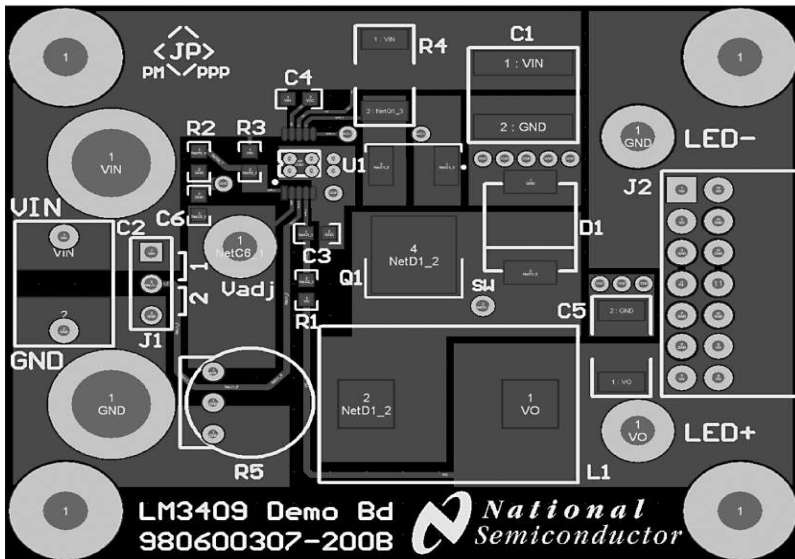


The undervoltage lockout will turn off the chip when VDD\_IN is below 5.2V



DN: R18 and C16 adjust 1.38us Offtim

LN: A 100uF capacitor has to be placed direct on the LED



D

C

B

A

|      |           |
|------|-----------|
| otis |           |
| 1    | Rev       |
| 2    | <RevCode> |

