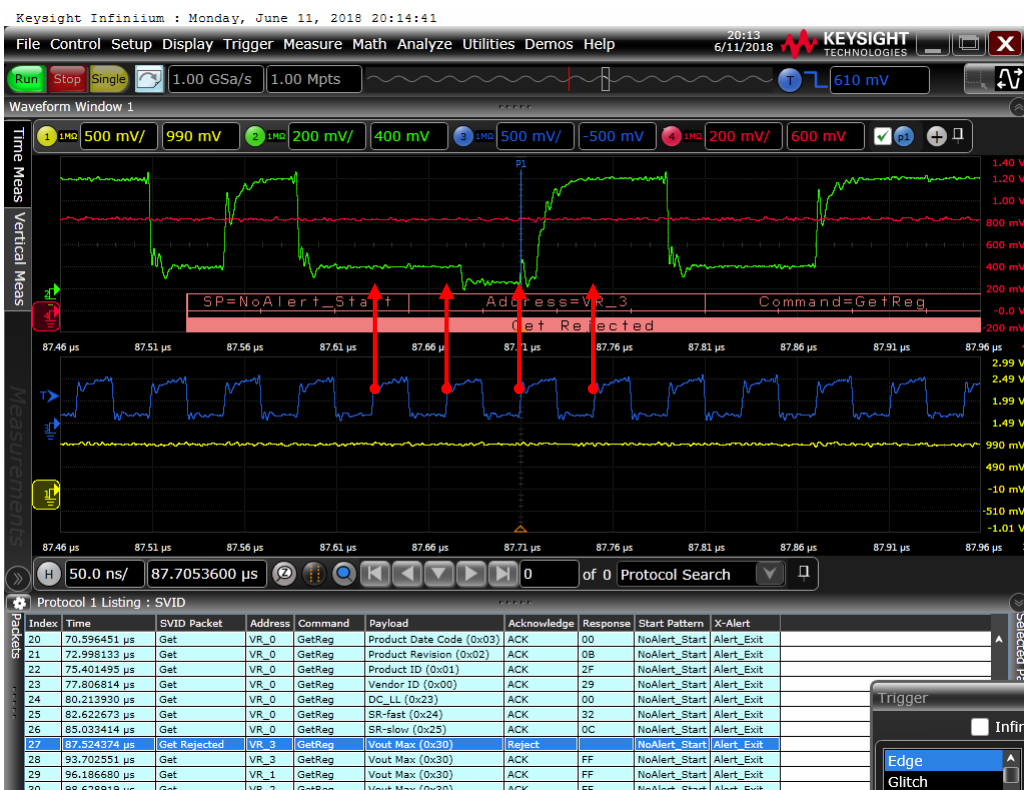


OK:
The SVID master(Xeon) is driving the VDIO data on the pos edge of clock.



NG:
It seems that the VDIO edge is not matched with the pos clock edge, and the address field has two low-voltage-level.
It might be collision between the SVID master output and the phantom pulse.
If so, there is a possibility that the SVID transaction will be unintended garbled data. (the address data will be garbled, and so on.)