

**Preliminary****ISX017-0AWR-C****STARVIS****Description**

The ISX017 is a System on Chip that consists a diagonal 5.678 mm (Type 1/3.2) CMOS active pixel type image sensor with approx. 1.27 active pixel array and a high performance image processing engine. This chip operates with analog 2.9 V and digital 1.8 (or 3.3) V / 1.1 V triple power supply voltage, and has low current consumption. This chip supports YCbCr format from Parallel I/F or MIPI CSI-2 I/F, RAW format from MIPI CSI-2 I/F, and Analog output. In addition, the control software is coded in on-chip ROM, which is suitable for small form-factor camera module application with this one chip device for surveillance.

(Application: surveillance)

**Features**

- ◆ CMOS active pixel type dots
- ◆ 12-bit A/D converter on chip
- ◆ PLL on chip
- ◆ High sensitivity, low dark current, no smear
- ◆ High frame rate (Quad-VGA 60 frame/s, HD720p 60 frame/s SMPTE296M)
- ◆ Control interface (I<sup>2</sup>C, SPI, UART)
- ◆ Digital output interface (Parallel output, MIPI CSI-2: 2 / 4-Lane)
  - YCbCr format
  - RAW format (Only MIPI CSI-2 output, Bayer format)
- ◆ Analog output interface (Composite video-out)
  - 11bit D/A converter output
- ◆ Wide dynamic range (WDR) function
  - Digital overlap WDR
- ◆ DEFOG function
- ◆ Vertical flip and horizontal mirror function (Dynamic transition supported)
- ◆ Mechanical-less Day & Night function
- ◆ AE, AWB control function
- ◆ AF detection function
- ◆ Mechanical IRIS control function
- ◆ IR-Optimizer function
- ◆ OSD menu function
- ◆ Serial-Flash control function

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## Device Structure

- ◆ CMOS image sensor
- ◆ Image size : Diagonal 5.678 mm (Type 1/3.2)
- ◆ Number of active pixels : 1297(H) × 977(V) = approx. 1.27M pixels
- ◆ Number of recommended recording pixels : 1280(H) × 960(V) = approx. 1.23M pixels
- ◆ Unit cell size : 3.5µm(H) × 3.5µm(V)
- ◆ Substrate material : Silicon

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## Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (I/O 1.8 / 3.3 V)	V <sub>DDMIO</sub>	- 0.3	+ 4.6	V	-
	V <sub>DDMMD</sub>	- 0.3	T.B.D.	V	-
Supply voltage (Analog 2.9 V)	V <sub>DDH</sub>	- 0.3	+ 4.1	V	-
Supply voltage (Digital 1.1 V)	V <sub>DDL</sub>	- 0.3	+ 1.5	V	-
Input voltage (I/O)	VI18 / VI33	VSS - 0.3	V <sub>DDM</sub> + 0.3	V	Not exceed 4.6 V
	VI29	VSS - 0.3	V <sub>DDH</sub> + 0.3	V	Not exceed 4.1 V
Output voltage (I/O)	VO18 / VO33	VSS - 0.3	V <sub>DDM</sub> + 0.3	V	Not exceed 4.6 V
	VO29	VSS - 0.3	V <sub>DDH</sub> + 0.3	V	Not exceed 4.1 V
Operating temperature	Topr	- 30	+ 85	°C	-
Storage temperature	Tstg	- 40	+ 85	°C	-

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## Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (I/O 1.8 / 3.3 V) <sup>*1</sup>	V <sub>DDM</sub>	1.70	1.80	1.90	V
		3.15	3.30	3.45	
Supply voltage (Analog 2.9 V)	V <sub>DDH</sub>	2.80	2.90	3.00	V
Supply voltage (Digital 1.1 V)	V <sub>DDL</sub>	1.00	1.10	1.20	V

\*1: For supply voltage of each I/O, refer to the Table 3-2 and Section 3-3.

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## 1. Feature

The ISX017 has characteristics shown below.

Table 1-1. Main characteristics

Function		Description
Image sensor	Sensor type	1/3.2 type CMOS image sensor
	Active pixel	1297 (H) × 977 (V) approx. 1.27Mpixels
	Recording pixel	1280 (H) × 960 (V) approx. 1.23Mpixels
ISP block	Adjustment function	Pattern generator function
	Auto control function	Auto exposure (AE) control, Auto white balance (AWB) control
	Image tuning function	Edge enhance, Noise reduction, Color control, Gamma correction, Brightness function, Contrast function, Effect function
	Output image format	YCbCr RAW (Only MIPI CSI-2)
Input / Output I/F	Image output	Digital Output • Parallel 16bit • MIPI CSI-2: 2/4Lane Analog Output(NTSC/PAL) • Composite video-out
	Control signal	I <sup>2</sup> C fast mode (@400 kHz), SPI, UART
Input clock frequency		27MHz
Maximum output frequency		Digital Output • 94.5MHz@YCbCr(Quad-VGA 60fps) • 74.25MHz@YCbCr(HD720p 60fps): SMPTE 296M
External interfaces		Serial-Flash I/F, GPIO 16ch, PWM 3ch
Number of PIN		76pins

## 2. ISP Features

ISP (Image Signal Processor)は以下の特徴を有しています。

Table 2-1. ISP Characteristics

Function		Description
Image conversion	Resize	Bi-linear subsampling (up to VGA size)
	Electrical zoom	Trimming data output (Resize at Host CPU mandatory)
	Image flip	Vertical, Horizontal
Camera control	Scene selection	Scene-dependent parameter (up to 255 parameters)
	Exposure control mode	Auto, Manual, Shutter priority, Gain priority, Preset, Mask
	Photometry	Center weight, Average, Spot, Histogram
	Exposure compensation	-2 EV to +2 EV, 1/3 EV step On typical setting
	Shutter speed range	1/60s to 1/67500s (Quad-VGA, Normal mode, 60fps)
	White balance	Auto : T.B.D. to T.B.D. (Typical setting) Preset : T.B.D.
	Back light compensation	Make dark area visible under backlit condition
Image processing	Wide dynamic range compensation	Synthesis 2 or 3 multiple exposure images
	Shading correction	RGB channel. Asymmetric shading correction
	Pixel compensation	Dynamic correction
	Noise reduction	Adaptive noise reduction
	Black level subtraction	Auto subtraction
	Adaptive Tone Reproduction	Luminance compression according to local block histograms
	Remosaicing	Convert from RGBW color filter array to Bayer color filter array while decomposing IR (Infra-red) signal component
	Gamma curve	Programmable
	Aperture compensation	Edge enhancement (sharpness)
	Suppress	Adaptive color suppression
	Color reproduction	Linear matrix, Hue gain control, Multi-color channel compensation
	Defog	Remove fog
	Highlight compensation	Make bright luminance area visible
	Flicker correction	50/60Hz auto detection, corrected by shutter speed control
	Image effect	Negative
	Lens distortion correction	Horizontal correction only

Other	Privacy Masking	Area masking by monotone overlay or mosaicking (up to 16 area)
	On Screen Display	455 fonts on ROM (for English, French, Germany, Spanish, Russian, Portuguese, Chinese, numerical and some symbols) and user specific fonts (up to 40 fonts)
	Synchronization	Internal/External
	Control signal format	I <sup>2</sup> C fast mode, UART, SPI
	Digital data rate	Quad-VGA 60fps YCbCr output
	Analog data rate	NTSC 59.94fps YCbCr output PAL 50fps YCbCr output

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### 3. Hardware Specification

#### 3-1. Block Diagram

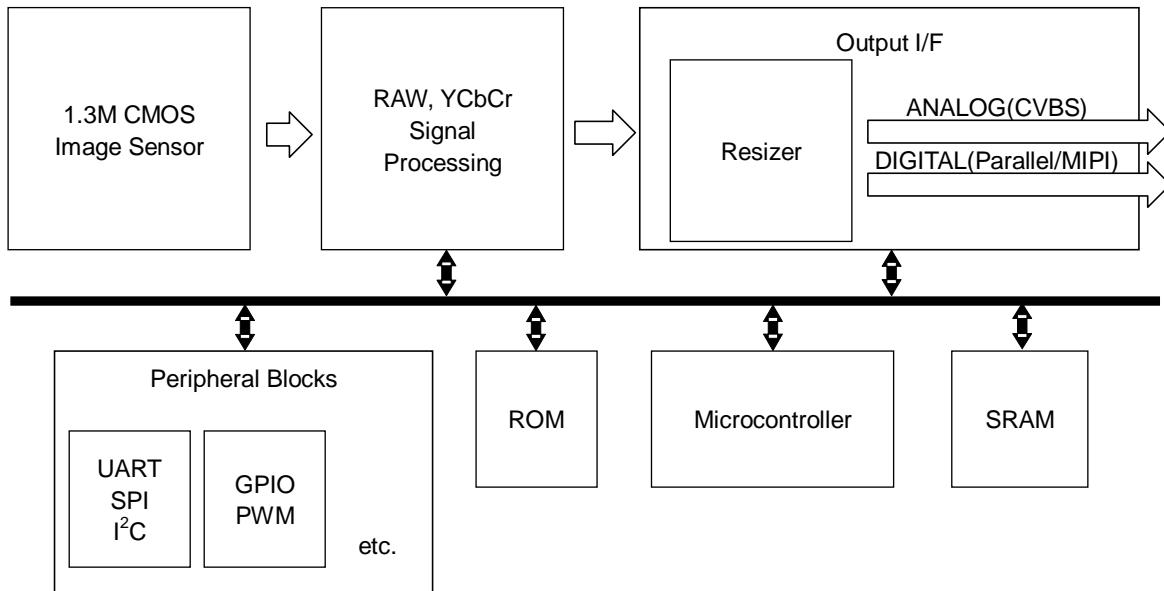


Fig. 3-1. Block structure

### 3-2. Pin Description

Table 3-1. Pin Description-1

Item	Pin No	Symbol	I/O	Pin description	Power
System	K4	OSCI	I	Clock Input	VDDMIO
	J4	OSCO	O	Clock Output	
	J8	XCLR	I	System reset (Active Low)	
	H6	FSYNC	I/O	External sync / PWM0 (IR Control) / GPIO12	
	F10	EXBUSY	I/O	Busy signal / GPIO15	
	J5	WDTINT	I/O	Watch dog timer interrupt / GPIO11	
OUTPUT I/F	B4	VSYNC	I/O	Parallel vertical sync / PWM1(M-IRIS/CONTBAL) / GPIO13	VDDMIO
	A4	HSYNC	I/O	Parallel horizontal sync / PWM2(M-IRIS/DRVLEVEL) / GPIO14	
	C1	DCK	I/O	Parallel data output clock	
	B3	DO00	I/O	Parallel image data bit0	
	A3	DO01	I/O	Parallel image data bit1	
	A2	DO02	I/O	Parallel image data bit2	
	B2	DO03	I/O	Parallel image data bit3	
	B1	DO04	I/O	Parallel image data bit4	
	C2	DO05	I/O	Parallel image data bit5	
	D1	D3P	O	Parallel image data bit6 / MIPI DMO3P (4lane mode)	VDDMIO VDDMMMD
GPIO	D2	D3N	O	Parallel image data bit7 / MIPI DMO3N (4lane mode)	
	E1	D1P	O	Parallel image data bit8 / MIPI DMO1P (2lane/4lane mode)	
	E2	D1N	O	Parallel image data bit9 / MIPI DMO1N (2lane/4lane mode)	
	F1	CKP	O	Parallel image data bit10 / MIPI DCKP (2lane/4lane mode)	
	F2	CKN	O	Parallel image data bit11 / MIPI DCKN (2lane/4lane mode)	
	G1	D2P	O	Parallel image data bit12 / MIPI DMO2P (2lane/4lane mode)	
	G2	D2N	O	Parallel image data bit13 / MIPI DMO2N (2lane/4lane mode)	
	H1	D4P	O	Parallel image data bit14 / MIPI DMO4P (4lane mode)	
	H2	D4N	O	Parallel image data bit15 / MIPI DMO4N (4lane mode)	
	J6	GPIO0	I/O	GPIO / Parallel data enable	VDDMIO
SPI	K6	GPIO1	I/O	GPIO / AF detect vertical sync	
	K5	GPIO2	I/O	GPIO	
	J10	GPIO3	I/O	GPIO / SPI Slave SCK	
	K9	GPIO4	I/O	GPIO / SPI Slave SDI	
	H9	GPIO5	I/O	GPIO / SPI Slave SDO	
	J9	GPIO6	I/O	GPIO / SPI Slave XCE	
	F9	GPIO7	I/O	GPIO / I <sup>2</sup> C SDA (Slave, Master) / UART TXD	
	G10	GPIO8	I/O	GPIO / I <sup>2</sup> C SCL (Slave, Master) / UART RXD	
	G9	GPIO9	I/O	GPIO	
	H10	GPIO10	I/O	GPIO	
CVBS OUT	D10	SCKM	I/O	SPI Master(Serial-Flash I/F)	VDDMIO9
	E9	SDIM	I/O		
	E10	SDOM	I/O		
	D9	XCEM	I/O		
CVBS OUT	A8	VDAOUTP	O	Analog data output	VDDHAVD

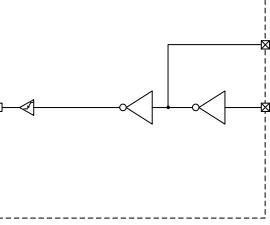
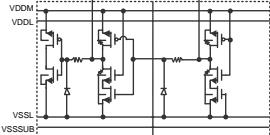
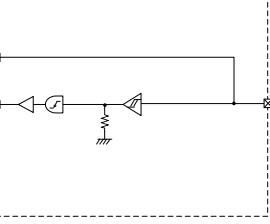
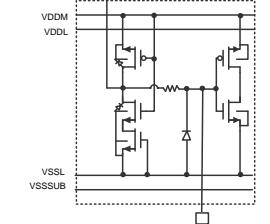
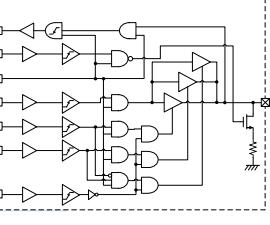
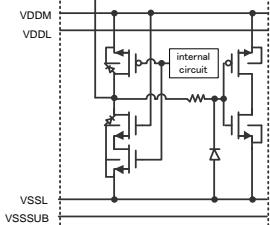
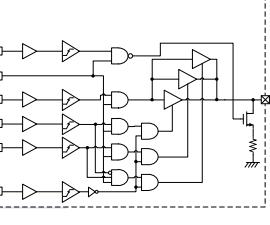
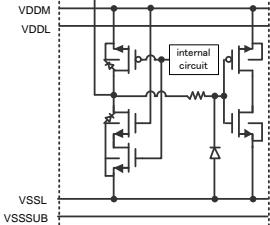
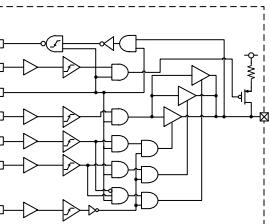
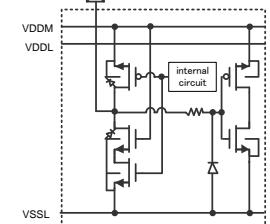
Table 3-2. Pin Description-2

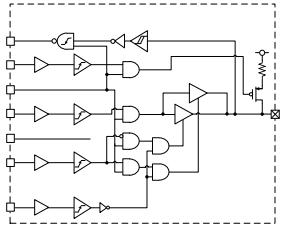
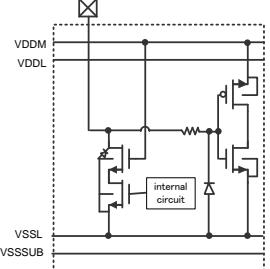
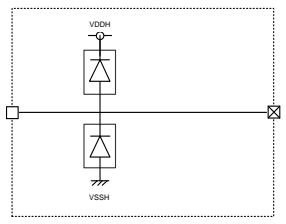
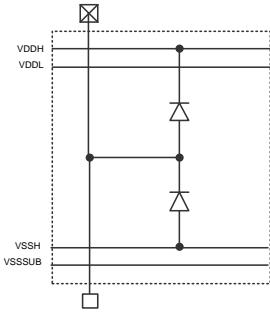
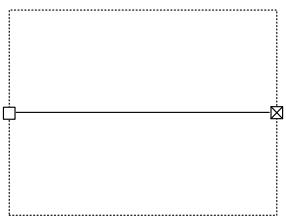
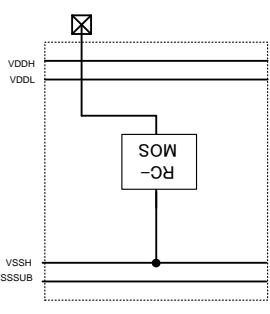
Item	Pin No	Pin name	I/O	Description (Parallel)	Description (MIPI)
Power	B10, C3, H3, H8, K8	VDDL	P	Core digital power (1.1V)	
	J1, K2	VDDLPL	P	PLL analog power (1.1V)	
	H4	VDDMMMD	P	I/O (Parallel) power (1.8 / 3.3V) *1	I/O (MIPI) power (1.8V)
	C10, H5	VDDMIO	P	I/O digital power (1.8 / 3.3 V) *1	I/O digital power (1.8 / 3.3V)
	A9	VDDMIO9	P	I/O (SPI Master (Serial-Flash IF)) digital power (1.8 / 3.3V)	
	A6, A7, B6	VDDH	P	Analog power (2.9V)	
GND	B9, C4, C8, C9, H7, J2, J3, J7, K3, K7	VSSL	G	Core digital GND	
	B7, C5, C6	VSSH	G	Sensor analog GND	
Sensor Internal Signal	B8	VCAP1	O	Reference pin	
	A5	VCAP2	O	Reference pin	
	B5	VCAP3	O	Reference pin	

\*1 It is necessary to make power supply voltage the same.

### 3-3. Equivalent Circuit

Table 3-3. Equivalent circuit

Name	Symbol	etc.	Drive capability	I/F voltage	Logic Symbol	ESD Image
IO-OSC	OSCI OSCO	—	—	1.8 V 3.3 V		
IO-I1	XCLR	Schmitt	—	1.8 V 3.3 V		
IO-O1	CKP CKN D1P D1N D2P D2N D3P D3N D4P D4N	Pull-down	[1.8V] 0.5mA 1mA 2mA 4mA / [3.3V] 1mA 2mA 4mA 8mA	1.8 V 3.3 V		
IO-BPD1	DCK DO00 DO01 DO02 DO03 DO04 DO05 GPIO0 GPIO1 GPIO2 GPIO4 GPIO5 GPIO10 FSYNC VSYNC HSYNC SDIM SDOM	Pull-down	[1.8V] 0.5mA 1mA 2mA 4mA / [3.3V] 1mA 2mA 4mA 8mA	1.8 V 3.3 V		
IO-BPU1	GPIO3 GPIO6 GPIO9 EXBUSY SCKM XCEM WDTINT	Pull-up	[1.8V] 0.5mA 1mA 2mA 4mA / [3.3V] 1mA 2mA	1.8 V 3.3 V		

Name	Symbol	etc.	Drive capability	I/F voltage	Logic Symbol	ESD Image
			4mA 8mA			
IO-BPU2	GPIO7 GPIO8	Pull-up	[1.8V] 1mA 2mA / [3.3V] 2mA 4mA	1.8 V 3.3 V		
IO-A1	VDAOUTP VCAP1	—	—	2.9 V		
IO-A2	VCAP2 VCAP3	—	—	—		

VDDL: Core digital power (1.1 V)

VDDM: I/O digital power (1.8 / 3.3 V)

VDDH: Analog power(2.9 V)

VSSL: Core digital GND

VSSH: Analog GND

VSSSUB: Substrate GND

### 3-4. Pin Status

Pin status during operation is shown below.

Table 3-4. Pin Status

Symbol	I/O	Reset	After Reset	Normal Operating
OSCI	I	IN		IN
OSCO	O	OUT		OUT
XCLR	I	IN		IN
EXBUSY	I/O	Hi-z(pull-up)	OUT H(pull-up)	OUT
SCKM	I/O	Hi-z(pull-up)	OUT H(pull-up)	OUT
SDIM	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	IN
SDOM	I/O	Hi-z(pull-down)	OUT L(pull-down)	OUT
XCEM	I/O	Hi-z(pull-up)	OUT H(pull-up)	OUT
WDTINT	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O (*1 GPIO)
GPIO0	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
GPIO1	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
GPIO2	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
GPIO3	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O
GPIO4	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
GPIO5	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
GPIO6	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O
GPIO7	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O
GPIO8	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O
GPIO9	I/O	Hi-z(pull-up)	IN(Hi-z pull-up)	I/O
GPIO10	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
DCK	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
FSYNC	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
HSYNC	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
VSYNC	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	I/O
DO00	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
DO01	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
DO02	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
DO03	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
DO04	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
DO05	I/O	Hi-z(pull-down)	IN(Hi-z pull-down)	OUT
D3P	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D3N	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D1P	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D1N	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
CKP	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
CKN	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D2P	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D2N	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D4P	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT
D4N	O	Hi-z(pull-down)	Hi-z(pull-down)	OUT

\*1 WDTINT pin is shared with GPIO. Default status is WDTINT. The status will be the OUT (Low output) only when the interrupt is occurred by Watch-dog-timer.

### 3-5. Chip Center, Optical Center and Pin Configuration

The package center and optical center are same.

### 3-6. Pin Configuration

	A	B	C	D	E	F	G	H	J	K
10	TEST	VDDL	VDDMIO	SCKM	SDOM	EXBUSY	GPIO8	GPIO10	GPIO3	NC
9	VDDMIO9	VSSL	VSSL	XCEM	SDIM	GPIO7	GPIO9	GPIO5	GPIO6	GPIO4
8	VDAOUTP	VCAP1	VSSL	TOPVIEW					VDDL	XCLR
7	VDDH	VSSH	TVMON						VSSL	VSSL
6	VDDH	VDDH	VSSH						FSYNC	GPIO0
5	VCAP2	VCAP3	VSSH						VDDMIO	WDTINT
4	HSYNC	VSYNC	VSSL						VDDMMMD	OSCO
3	DO01	DO00	VDDL						VDDL	VSSL
2	DO02	DO03	DO05	D3N	D1N	CKN	D2N	D4N	VSSL	VDDLPL
1	NC	DO04	DCK	D3P	D1P	CKP	D2P	D4P	VDDLPL	NC

## 4. Sensor Specification

### 4-1. Pixel Array Physical Image

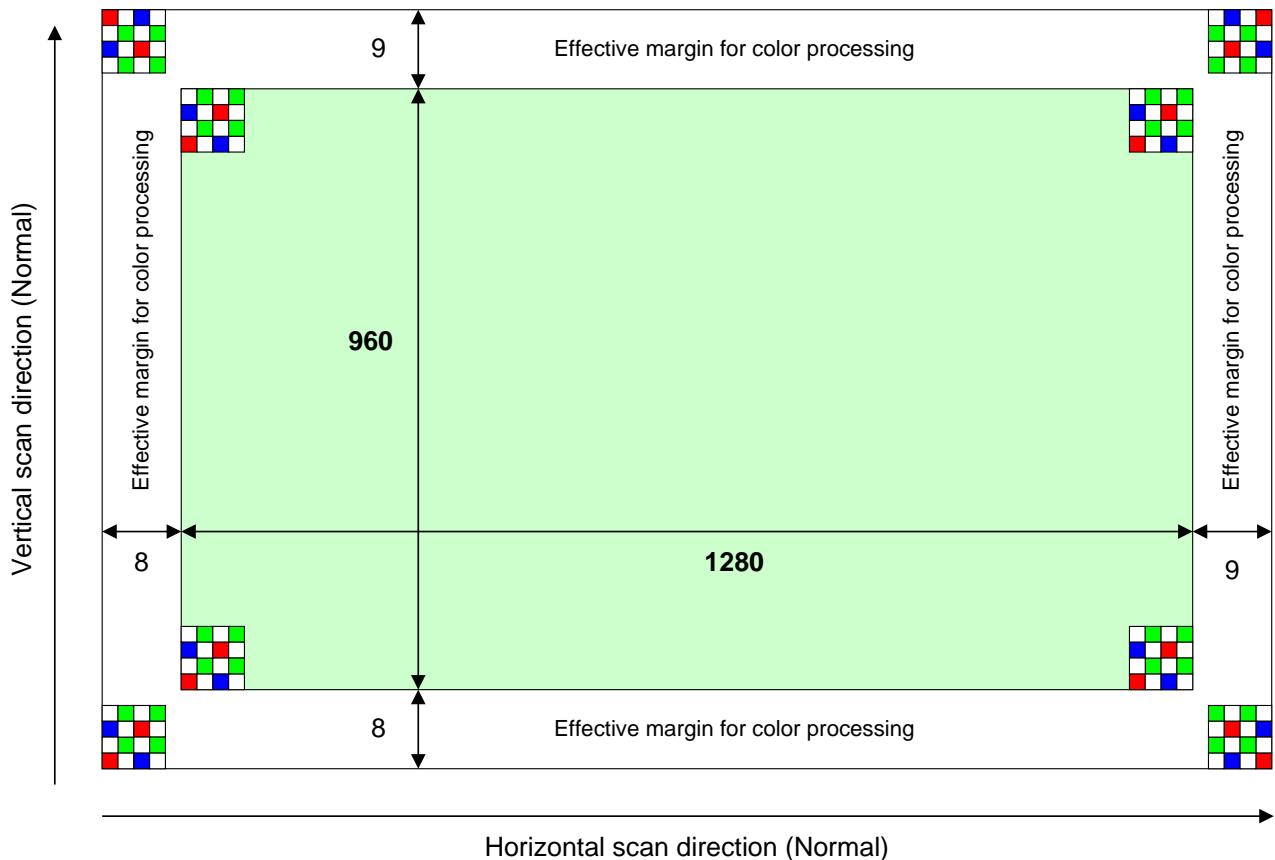


Fig. 4-1. Pixel Array Diagram

#### 4-2. Readout Position

Read-out in the default condition of the ISX017 starts from the lower left corner when Pin No.1 is located in the upper right corner. The image is flipped vertically and horizontally through the lens, so placing Pin No.1 in the upper right corner is correct for proper image output.

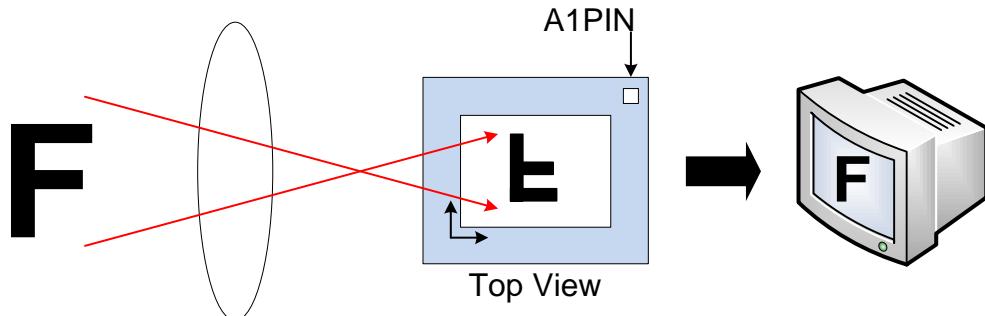


Fig. 4-2. Readout Position

In addition, this system supports up/down and/or right/left flipping, and is capable of the following outputs. When using the inversion function, the pixel array read from the sensor changes, but this is processed adaptively within the ISP, so there is no need for users to be aware of it. However, care must be taken in RAW output mode since the sensor data is output as is.

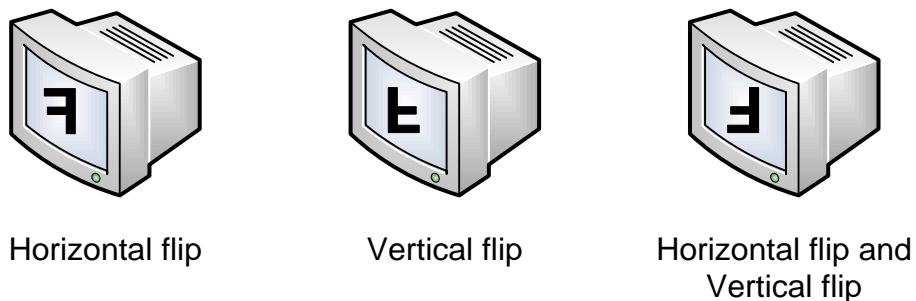


Fig. 4-3. Output Image for Vertical Flip and Horizontal Mirror

## 5. Electrical Characteristics

### 5-1. DC Characteristics

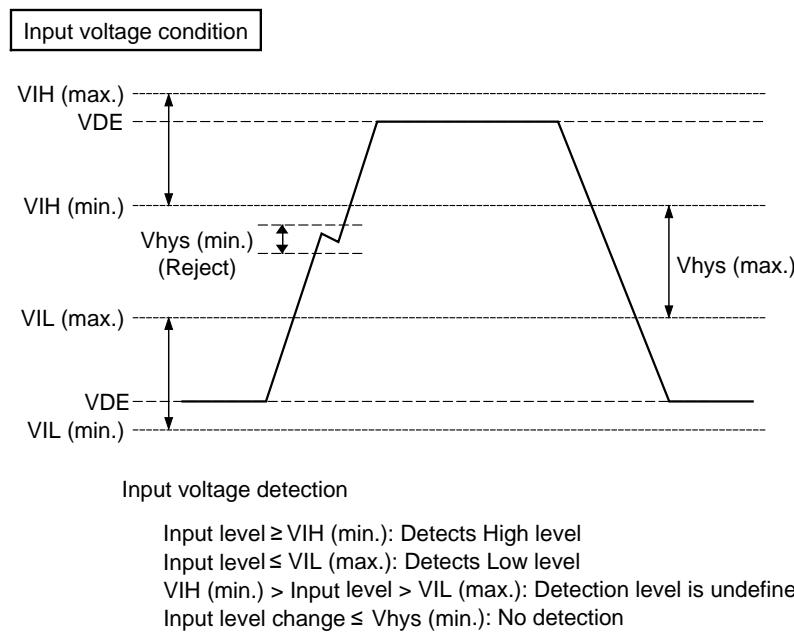


Fig. 5-1. Definition of Input Voltage Condition

#### 5-1-1. IO-OSC DC Characteristics

Table 5-1. IO-OSC DC Characteristics (In case of external clock input)

Name	Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
IO-OSC	H level schmitt input voltage	VIH	$V_{DDM} \times 0.65$	—	—	V	
	L level schmitt input voltage	VIL	—	—	$V_{DDM} \times 0.35$	V	
	Input leakage current	IL	-10	—	+10	$\mu A$	

#### 5-1-2. IO-I1 DC Characteristics

Table 5-2. IO-I1 DC Characteristics

Name	Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
IO-I1	H level schmitt input voltage	VIH	$V_{DDM} \times 0.65$	—	—	V	
	L level schmitt input voltage	VIL	—	—	$V_{DDM} \times 0.35$	V	
	Input leakage current	IL	-10	—	+10	$\mu A$	
	Hysteresis width	Vhys	—	0.2	—	V	

**5-1-3. IO-O1**

Table 5-3. IO-O1 DC Characteristics

Name	Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
IO-O1	H level output voltage ( $V_{DDM} = 1.8 \text{ V}$ )	VOH1	$V_{DDM} - 0.2$	—	—	V	$IOH = -0.5 \text{ mA}$
	L level output voltage ( $V_{DDM} = 1.8 \text{ V}$ )	VOL1	—	—	0.2	V	$IOL = 0.5 \text{ mA}$
	H level output voltage ( $V_{DDM} = 3.3 \text{ V}$ )	VOH2	$V_{DDM} - 0.2$	—	—	V	$IOH = -1 \text{ mA}$
	L level output voltage ( $V_{DDM} = 3.3 \text{ V}$ )	VOL2	—	—	0.2	V	$IOL = 1 \text{ mA}$
	Output leakage current	IOZ	$V_{DDM} - 0.2$	—	+35 +55	$\mu\text{A}$	1.8V 3.3V
	Pull-down resistance	Rpd	80	100	120	k $\Omega$	

**5-1-4. IO-BPD1, IO-BPU1, IO-BPU2 DC Characteristics**

Table 5-4. IO-BPD1, IO-BPU1, IO-BPU2 DC Characteristics

Name	Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
IO-BPD1 IO-BPU1 IO-BPU2	H level input voltage	VIH	$V_{DDM} \times 0.65$	—	—	V	
	L level input voltage	VIL	—	—	$V_{DDM} \times 0.35$	V	
	Input leakage current	IL	-35 -55	—	+35 +55	$\mu\text{A}$	1.8V 3.3V
	H level output voltage ( $V_{DDM} = 1.8 \text{ V}$ )	VOH1	$V_{DDM} - 0.2$	—	—	V	$IOH = -0.5 \text{ mA}$
	L level output voltage ( $V_{DDM} = 1.8 \text{ V}$ )	VOL1	—	—	0.2	V	$IOL = 0.5 \text{ mA}$
	H level output voltage ( $V_{DDM} = 3.3 \text{ V}$ )	VOH2	$V_{DDM} - 0.2$	—	—	V	$IOH = -1 \text{ mA}$
	L level output voltage ( $V_{DDM} = 3.3 \text{ V}$ )	VOL2	—	—	0.2	V	$IOL = 1 \text{ mA}$
	Output leakage current	IOZ	-35 -55	—	+35 +55	$\mu\text{A}$	1.8V 3.3V
	Pull-down resistance Pull-up resistance	Rpd Rpu	80	100	120	k $\Omega$	

## 5-2. AC Characteristics

### 5-2-1. Input Clock

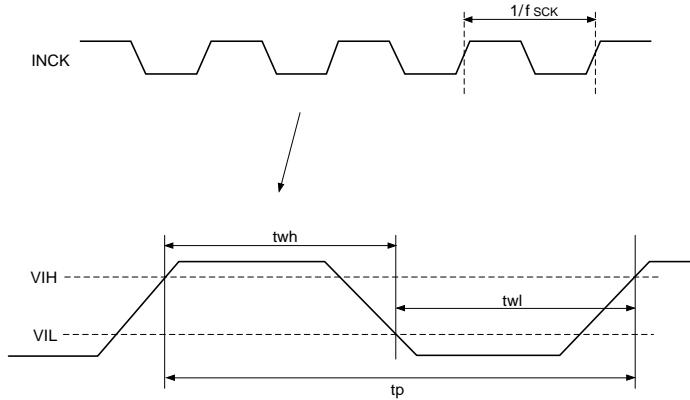


Fig. 5-2. Input clock timing

Table 5-5. Input clock specific characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	$f_{SCK}$	-	27	-	MHz
INCK Low level width	twl	0.45 tp		0.55 tp	ns
INCK High level width	twh	0.45 tp		0.55 tp	ns

### 5-2-2. I<sup>2</sup>C I/F

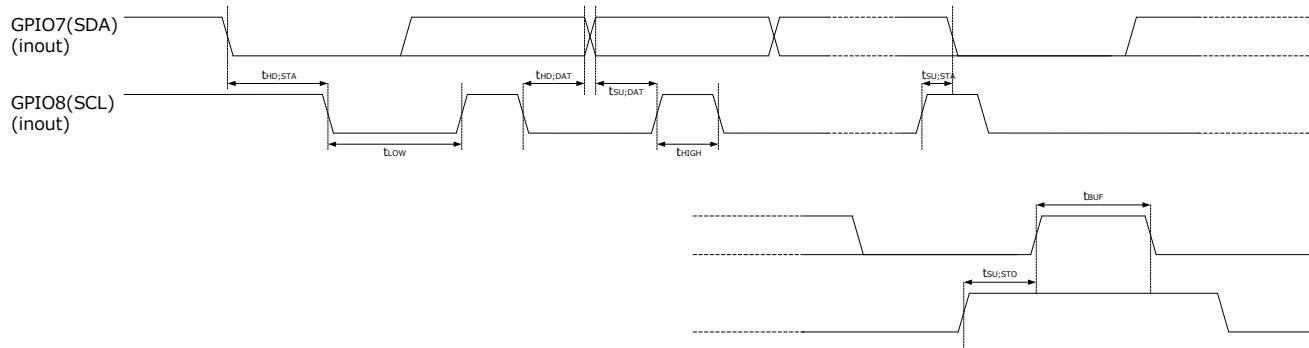


Fig. 5-3. I<sup>2</sup>C Communication Timing

Table 5-6. I<sup>2</sup>C specific characteristics

Item	Symbol	Typical mode		High speed mode		Unit
		Min.	Max.	Min.	Max.	
SCL frequency	$f_{SCL}$		100		400	kHz
Hold time (iterated) "START" condition	$t_{HD;STA}$	4.0		0.6		μs
SCL Low period	$t_{LOW}$	4.7		1.3		μs
SCL High period	$t_{HIGH}$	4.0		0.6		μs
Iterated "START" condition setup	$t_{SU;STA}$	4.7		0.6		μs
Data hold	$t_{HD;DAT}$	0	—	0	—	μs
Data setup	$t_{SU;DAT}$	250		100		ns
"STOP" condition setup	$t_{SU;STO}$	4.0		0.6		μs
Bus free time between "STOP" condition and "START" condition	$t_{BUF}$	4.7		1.3		μs
Load capacity of bus line	$C_b$		20		20	pF

### 5-2-3. External CPU I/F

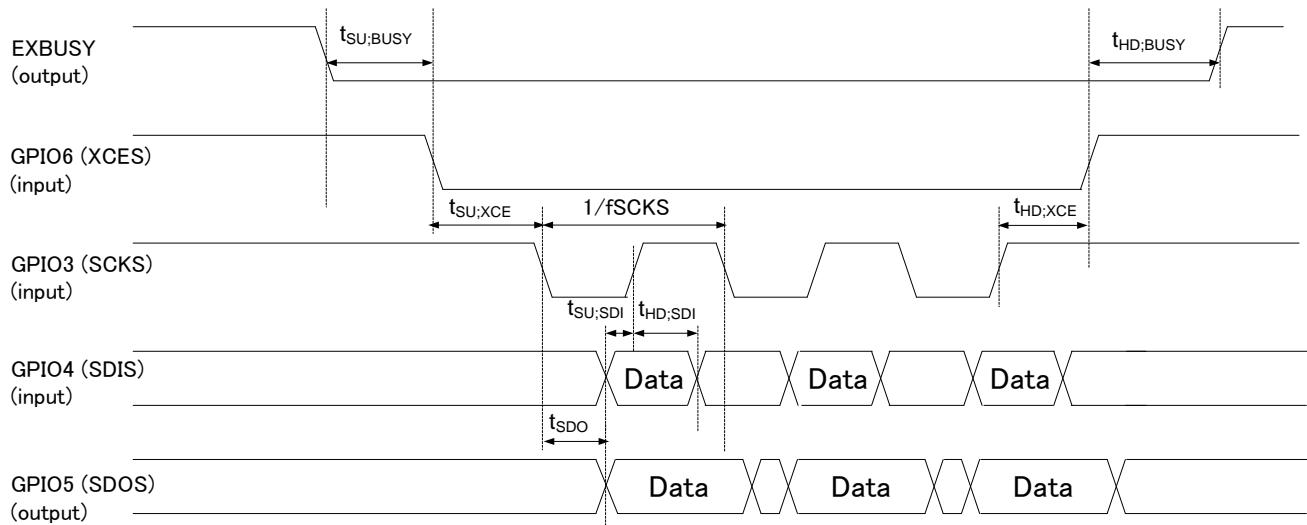


Fig. 5-4. External CPU I/F

Table 5-7. External CPU I/F specific characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCKS clock frequency	$f_{SCKS}$	-	-	580	KHz
EXBUSY setup time	$t_{SU;BUSY}$	10	-	-	ns
EXBUSY hold time	$t_{HD;BUSY}$	-	-	200	ns
XCES setup time	$t_{SU;XCE}$	600	-	-	ns
XCES hold time	$t_{HD;XCE}$	500	-	-	ns
SDIS setup time	$t_{SU;SDI}$	10	-	-	ns
SDIS hold time	$t_{HD;SDI}$	125	-	-	ns
SDOS output delay	$t_{SDO}$	5	-	160	ns

(Max. Capacitance: 20pF)

### 5-2-4. Serial-Flash I/F

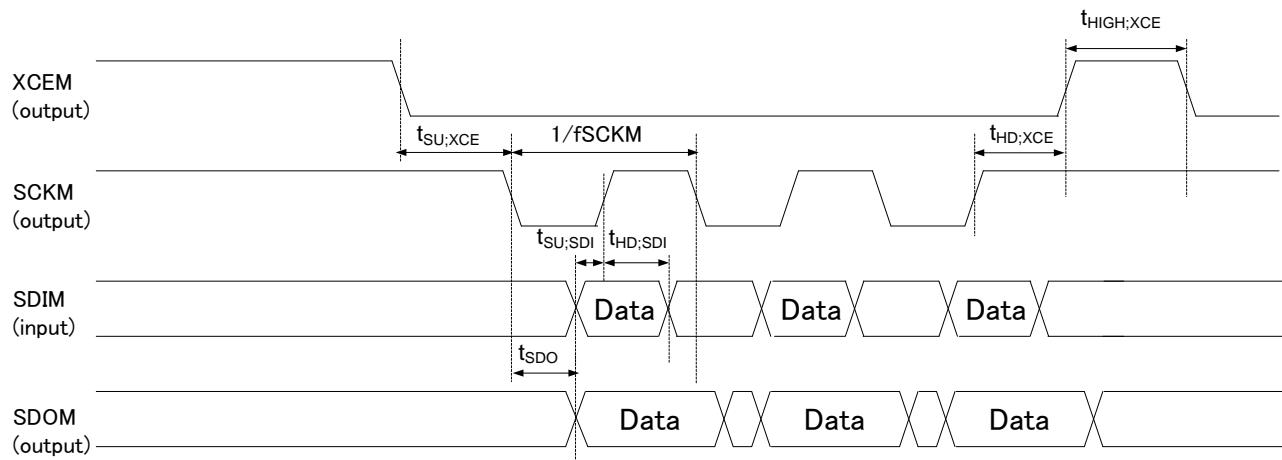


Fig. 5-5. Serial-Flash I/F

Table 5-8. Serial-Flash I/F specific characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCKM clock frequency	$f_{SCKM}$	-	-	13.5	MHz
XCEM High time	$t_{HIGH:XCE}$	100	-	-	ns
XCEM setup time	$t_{SU:XCE}$	100	-	-	ns
XCEM hold time	$t_{HD:XCE}$	100	-	-	ns
SDIM setup time	$t_{SU;SDI}$	20	-	-	ns
SDIM hold time	$t_{HD; SDI}$	0	-	-	ns
SDOM output delay	$t_{SDO}$	-20	-	20	ns

(Max Capacitance : 20pF)

### 5-2-5. Parallel Output

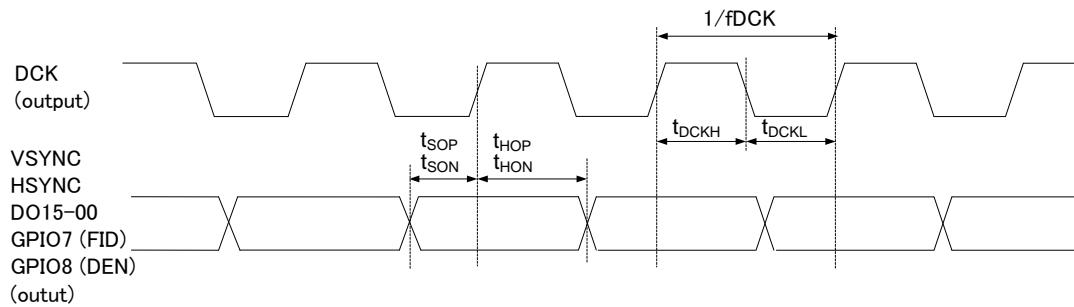


Fig. 5-6. Parallel Output

Table 5-9. Parallel Output specific characteristics (DCK normal output)

Item	Symbol	Min.	Typ.	Max.	Unit
DCK frequency	f <sub>DCK</sub>			108	MHz
DCK Low pulse width	t <sub>DCKL</sub>	(1/f <sub>DCK</sub> )×0.4		(1/f <sub>DCK</sub> )×0.6	ns
DCK High pulse width	t <sub>DCKH</sub>	(1/f <sub>DCK</sub> )×0.4		(1/f <sub>DCK</sub> )×0.6	ns
SYNC/Data setup	t <sub>SOP</sub>	0			ns
SYNC/Data hold	t <sub>HON</sub>	3.0			ns

Table 5-10. Parallel Output specific characteristics (DCK inverted output)

Item	Symbol	Min.	Typ.	Max.	Unit
DCK frequency	f <sub>DCK</sub>			108	MHz
DCK Low pulse width	t <sub>DCKL</sub>	(1/f <sub>DCK</sub> )×0.4		(1/f <sub>DCK</sub> )×0.6	ns
DCK High pulse width	t <sub>DCKH</sub>	(1/f <sub>DCK</sub> )×0.4		(1/f <sub>DCK</sub> )×0.6	ns
SYNC/Data setup	t <sub>SON</sub>	2.5			ns
SYNC/Data hold	t <sub>HON</sub>	2.0			ns

Table 5-11. Maximum External Load Capacitance

Voltage	External load capacitance	Drive capability
1.8 / 3.3V	10pF	2.0mA
	15pF	4.0mA

### 5-3. Current Consumption

#### 5-3-1. Operating Current (Quad-VGA, 60fps, Digital overlap 2frame mode, Parallel output)

Table 5-12. Operating current (Quad-VGA, 60fps, Digital overlap 2frame mode, Parallel output)

Item	Symbol	Min.	Typ.	Max.	Unit	Description
I/O		—	T.B.D.	T.B.D.	mA	
Analog		—	T.B.D.	T.B.D.	mA	
Digital		—	T.B.D.	T.B.D.	mA	

Typ.  $V_{DDM}$ : 1.8V,  $V_{DHD}$ : 2.9V,  $V_{DDL}$ : 1.1V,  $T_j = 25^\circ\text{C}$

Max.  $V_{DDM}$ : 1.9V,  $V_{DHD}$ : 3.0V,  $V_{DDL}$ : 1.2V,  $T_j = 60^\circ\text{C}$

#### 5-3-2. Operating Current (Quad-VGA, 60fps, Digital overlap 2frame mode, MIPI 2Lane output)

Table 5-13. Operating current (Quad-VGA, 60fps, Digital overlap 2frame mode, MIPI 2Lane output)

Item	Symbol	Min.	Typ.	Max.	Unit	Description
I/O		—	T.B.D.	T.B.D.	mA	
Analog		—	T.B.D.	T.B.D.	mA	
Digital		—	T.B.D.	T.B.D.	mA	

Typ.  $V_{DDM}$ : 1.8V,  $V_{DHD}$ : 2.9V,  $V_{DDL}$ : 1.1V,  $T_j = 25^\circ\text{C}$

Max.  $V_{DDM}$ : 1.9V,  $V_{DHD}$ : 3.0V,  $V_{DDL}$ : 1.2V,  $T_j = 60^\circ\text{C}$

#### 5-3-3. Operating Current (NTSC-1280H, Digital overlap 2frame mode, Analog output)

Table 5-14. Operating current (NTSC-1280H, Digital overlap 2frame mode, Analog output)

Item	Symbol	Min.	Typ.	Max.	Unit	Description
I/O		—	T.B.D.	T.B.D.	mA	
Analog		—	T.B.D.	T.B.D.	mA	
Digital		—	T.B.D.	T.B.D.	mA	

Typ.  $V_{DDM}$ : 1.8V,  $V_{DHD}$ : 2.9V,  $V_{DDL}$ : 1.1V,  $T_j = 25^\circ\text{C}$

Max.  $V_{DDM}$ : 1.9V,  $V_{DHD}$ : 3.0V,  $V_{DDL}$ : 1.2V,  $T_j = 60^\circ\text{C}$

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## 6. Image Sensor Characteristics

### 6-1. Spectral Sensitivity Characteristics

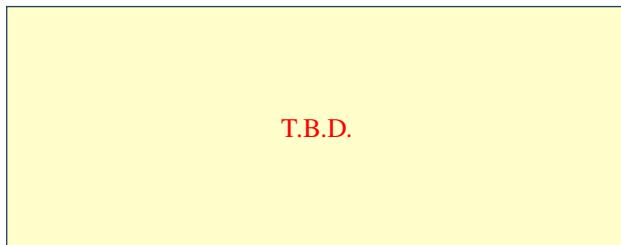


Fig. 6-1. Spectral Sensitivity Characteristics

**6-2. Image Sensor Characteristics**

Table 6-1. List of Image Sensor Characteristics

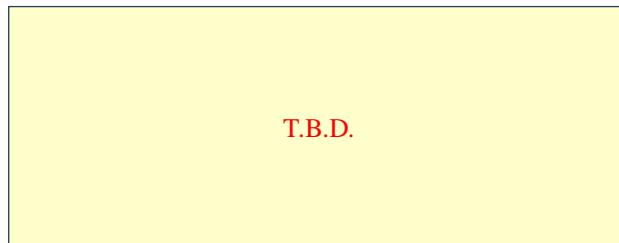
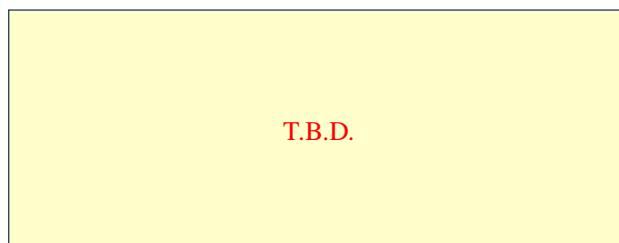
**Video Shading Zone Definition**

Fig. 6-2. Video Shading Zone Definition

### 6-3. Image Sensor Characteristics Measurement Method

#### Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the W, Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

#### Color Coding of Physical Pixel Array

The color filter filters of this image sensor are arranged in the layout shown below.

W	G	W	G	W	G	W	G
B	W	R	W	B	W	R	W
W	G	W	G	W	G	W	G
R	W	B	W	R	W	B	W
W	G	W	G	W	G	W	G
B	W	R	W	B	W	R	W
W	G	W	G	W	G	W	G
R	W	B	W	R	W	B	W

Fig. 6-3. Color Coding Diagram

### 6-4. Definition of standard imaging conditions

#### Standard imaging condition I:

Use a pattern box (luminance: 706 cd/m<sup>2</sup>, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S ( $t = 1.0$  mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

#### Standard imaging condition II:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S ( $t = 1.0$  mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

#### Standard image condition III:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -30 mm) with CM500S ( $t = 1.0$  mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

## 6-5. Measurement Method

### 1. Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the G signal outputs ( $V_G$ ) and Wg and Wrb signal outputs ( $V_{WG}$ ,  $V_{Wrb}$ ) at the center of the screen, and substitute the values into the following formula.

$$S = V_G \times 100/30 \text{ [mV]}$$
$$S = (V_{WG} + V_{Wrb}) / 2 \times (100 / 30) \text{ [mV]}$$

### 2. Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting the average value of the G signal outputs to **T.B.D.** mV, measure the R signal output ( $V_R$  [mV]), the G signal output ( $V_G$  [mV]), the B signal output ( $V_B$  [mV]) and Wg and Wrb signal outputs ( $V_{WG}$ ,  $V_{Wrb}$  [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

$$RG = (V_R / V_G)$$
$$RB = (V_B / V_G)$$
$$WG = \{(V_{WG} + V_{Wrb}) / 2\} / V_G$$

### 3. Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the G signal output, **T.B.D.** mV, measure the minimum values of the Wg, Wrb, G, R and B signal outputs.

### 4. Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Wg and Wrb signal outputs is **T.B.D.** mV. Then measure the maximum value ( $W_{max}$  [mV]) and the minimum value ( $W_{min}$  [mV]) of the Wg and Wrb signal outputs, and substitute the values into the following formula.

$$SH = (W_{max} - W_{min}) / **T.B.D.** \times 100 [\%].$$

### 5. Dark signal

With the device junction temperature of 60 °C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output ( $V_{dt}$  [mV]).

### 6. Dark signal shading

After the measurement item 5, measure the maximum value ( $V_{dmax}$  [mV]) and the minimum value ( $V_{dmin}$  [mV]) of the dark signal output, and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} \text{ [mV]}$$

## 7. I/O Interface

### 7-1. UART Interface

This section describes the communication interface of UART from the HOST.

#### 7-1-1. Connection Diagram

The connection example of UART in half duplex connection is shown below.

\* Full duplex connection is also available.

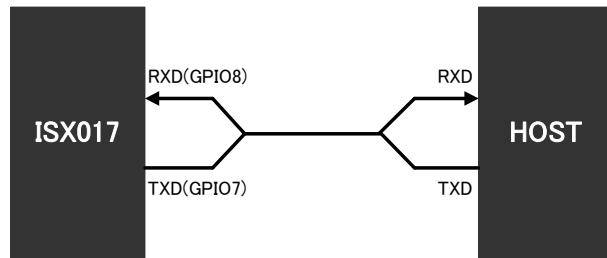


Fig. 7-1. UART Connection Schema

#### 7-1-2. Communication Setting

The baud rate can be changed from the HOST, but all other settings are fixed. The baud rate can be changed by register settings in start up or PreActive state. When using Reset Config, the baud rate of start-up is depend on selection of Reset Config. The maximum size for transmission and reception data is 137 bytes each.

Table 7-1. UART Communication Setting

Supported baud rate[bps]	9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400
Data length	8bit
Parity bit	Not available
Stop bit	1bit
Flow control	Not available
Amount of transmission data in one packet	Max. 137byte
Amount of reception data in one packet	Max. 137byte

## 7-2. I<sup>2</sup>C Interface

This section describes the communication interface of I<sup>2</sup>C from the HOST

### 7-2-1. Connection Diagram

The Host is the master, and the ISX017 is the slave.

Note that multi-master function is not supported, so do not connect multiple master devices.

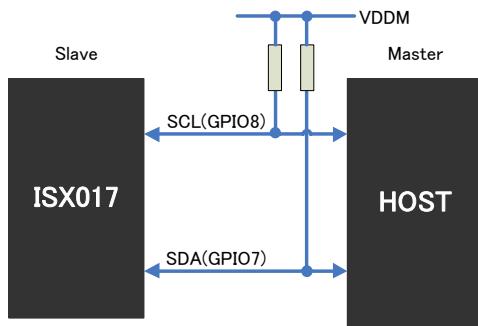


Fig. 7-2. I<sup>2</sup>C Connection Schema

### 7-2-2. Communication Specification

The maximum size of transmission data and reception data is 138 bytes (includes slave address). The slave address is 7-bits long, and the communication direction bit will be added to LSB when transmitted.

Table 7-2. I<sup>2</sup>C Communication Setting

Slave address *1	Possible to set arbitrary value to 7-bit by register
SCL clock frequency	100KHz, 400KHz
Amount of transmission data in one packet	Max. 138 byte ( include slave address )
Amount of reception data in one packet	Max. 138 byte ( include slave address )

\*1 Default value of slave address is 0x18. It is possible to set by Reset Config.

### 7-3. SPI Interface

This section describes the communication interface of SPI from the HOST.

#### 7-3-1. Connection Diagram

Connect 4-wire communication signals and BUSY signal. The HOST is the master, and the ISX017 is slave.

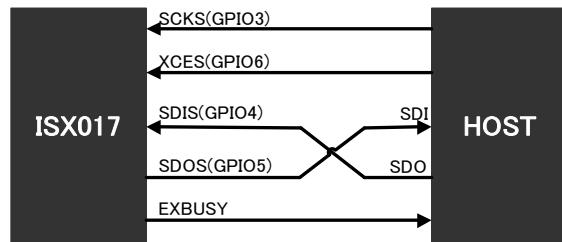


Fig. 7-3. SPI Connection Schema

#### 7-3-2. Communication Specification

The maximum size of transmission data and reception data is 137 bytes each. Do not transmit or receive data of more than 138 bytes.

Table 7-3. SPI Communication Setting

SCK frequency *1	Max 580KHz
SCL polarity	Low active
CS polarity	Low active
BUSY signal	High : Communication prohibited Low: Communication enable
Amount of transmission data in one packet	Max. 137 Byte
Amount of reception data in one packet	Max. 137 Byte

\*1 w/o Interval

#### 7-4. Port Driver

Port Driver is a function that changes the parameter values via GPIO input pins and outputs parameter values to GPIO output pins. The control method can be selected from among Volume, Toggle, Data output, and General-purpose input and output. It is possible to set each channel separately.

Table 7-4. List of Port Driver Function

Function name	GPIO I/O direction	Description
Volume	Input	Parameters can be incremented or decremented by input-signal time-period to GPIO input pin. Also step value and speed to increment or decrement parameters can be set via the GPIO.
Toggle	Input	Parameters can be switched by input-signal On/Off to GPIO input pin.
Data output	Output	Bit value (High or Low) of any parameters can be output to GPIO output pin.
General purpose data	Input	Input value to GPIO pins can be monitored at a register.
	Output	Values requested can be output to GPIO output pins.

---

## 8. Image Output

### 8-1. Description

The ISX017 supports three kind of interface; the parallel output from YCbCr format, MIPI CSI-2 output from YCbCr format, MIPI CSI-2 output from RAW format, and composite video-out from analog format (NTSC/PAL).

\* Simultaneous output from each interface is not supported.

### 8-2. Output Mode

The summary of output modes in ISX017 are shown in

Table 8-1. The summary of output modes in ISX017 are shown on Table 8-1. The details of each output interface are described in following chapter.

Table 8-1. List of Output mode

I/F	Parallel	MIPI		Analog
		2Lane	4Lane	
Output Rate	108MHz(MAX)	756Mbps/Lane(MAX)	432Mbps/Lane(MAX)	NTSC:SMPTE170M PAL:BT1700
Picture Size	YCbCr 1280x960(MAX) RAW 1296x976(MAX)	YCbCr 1280x960(MAX) RAW 1296x976(MAX)	YCbCr 1280x960(MAX) RAW 1296x976(MAX)	
Specification	YCbCr 16bit	YCbCr 16bit RAW 12bit	YCbCr 16bit RAW 12bit	

### 8-3. Parallel Interface

#### 8-3-1. Description

The ISX017 outputs signals which shown in the table 8-2 as parallel interface. Image data consists of an 8-bit luminance signal (Y) and an 8-bit chrominance signal (CbCr). A 16-bit parallel where luminance and chrominance signals is output. HSYNC / VSYNC / DEN are output as sync signals. In addition, the TRC (SAV/EAV) signals can be output within the output data. Note that the parallel interface is corresponding to progressive output only.

Table 8-2. Parallel Interface Signal Output

Pin Name	I/O	Bit width	Description
DCK	O	1	Data output clock
VSYNC	O	1	Vertical sync
HSYNC	O	1	Horizontal sync
GPIO0 (DEN)	O	1	Data enable
D1N~D4N, D1P~D4P, CKN, CKP, DO05~DO00	O	16	Digital data

\*DEN pin is also used as GPIO0 pin.

### 8-3-2. Data Output Pin

The data output pins are shown in the Table 8-3.

Table 8-3. Data Output Pin

Pin Name	YCbCr 16bit Parallel
D4N(DO15)	Cb[7] / Cr[7]
D4P(DO14)	Cb[6] / Cr[6]
D2N(DO13)	Cb[5] / Cr[5]
D2P(DO12)	Cb[4] / Cr[4]
CKN(DO11)	Cb[3] / Cr[3]
CKP(DO10)	Cb[2] / Cr[2]
D1N(DO09)	Cb[1] / Cr[1]
D1P(DO08)	Cb[0] / Cr[0]
D3N(DO07)	Y[7]
D3P(DO06)	Y[6]
DO05	Y[5]
DO04	Y[4]
DO03	Y[3]
DO02	Y[2]
DO01	Y[1]
DO00	Y[0]

### 8-3-3. H/V SYNC Output Outline

The ISX017 has two ways to output HSYNC / VSYNC: Level output and Pulse output. In Level output, the HSYNC signal is active during the effective period of each line, and the VSYNC signal is active during periods other than V-blanking. In Pulse output, the VSYNC / HSYNC pulses are output for synchronous timing of the frame and line. The polarities of HSYNC / VSYNC can be changed depending on the setting. The output diagram of Pulse output and Level output are shown in Fig. 8-1. The output diagram of Level output of H/VSYNC is shown in Fig. 8-2.

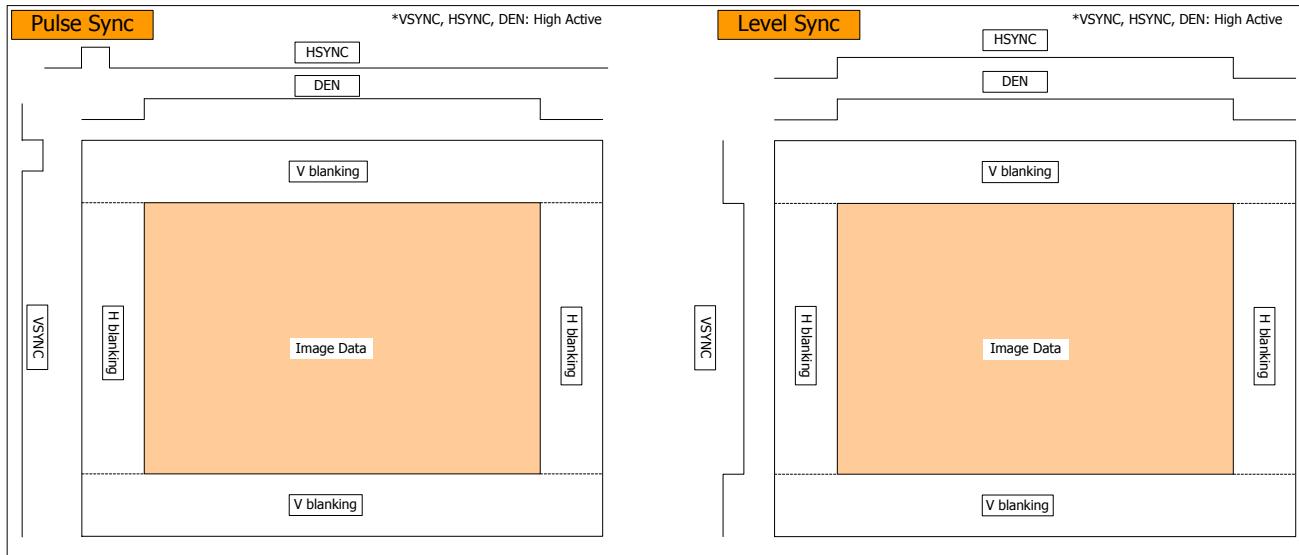


Fig. 8-1. Synchronous Signal Output Image Drawing

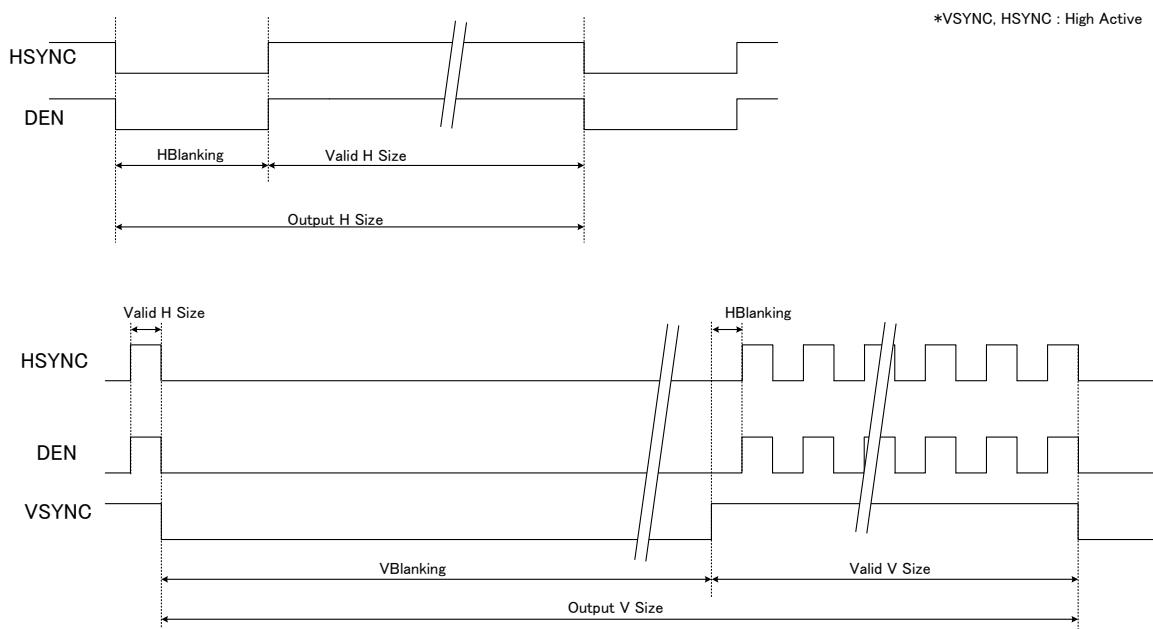


Fig. 8-2. Synchronous Timing of H / V Sync in Level Output

For the Pulse output timing of H / VSYNC, described to each output mode in chapter 8-4.

### 8-3-4. TRC Output

The TRC (Timing Reference Code) is a synchronous code that is inserted in the output data at the beginning and end of the blanking period. The EAV (End of Active Video) is inserted at the beginning of blanking, and the SAV (Start of Active Video) is inserted at the end of blanking. SAV and EAV are 4-byte continuous data, each with 0xFF, 0x00, 0x00, and 0xXY. Fig. 8-3. shows the positions of the inserted SAV, and Table 8-4 shows the bit assignment for the 4th byte.

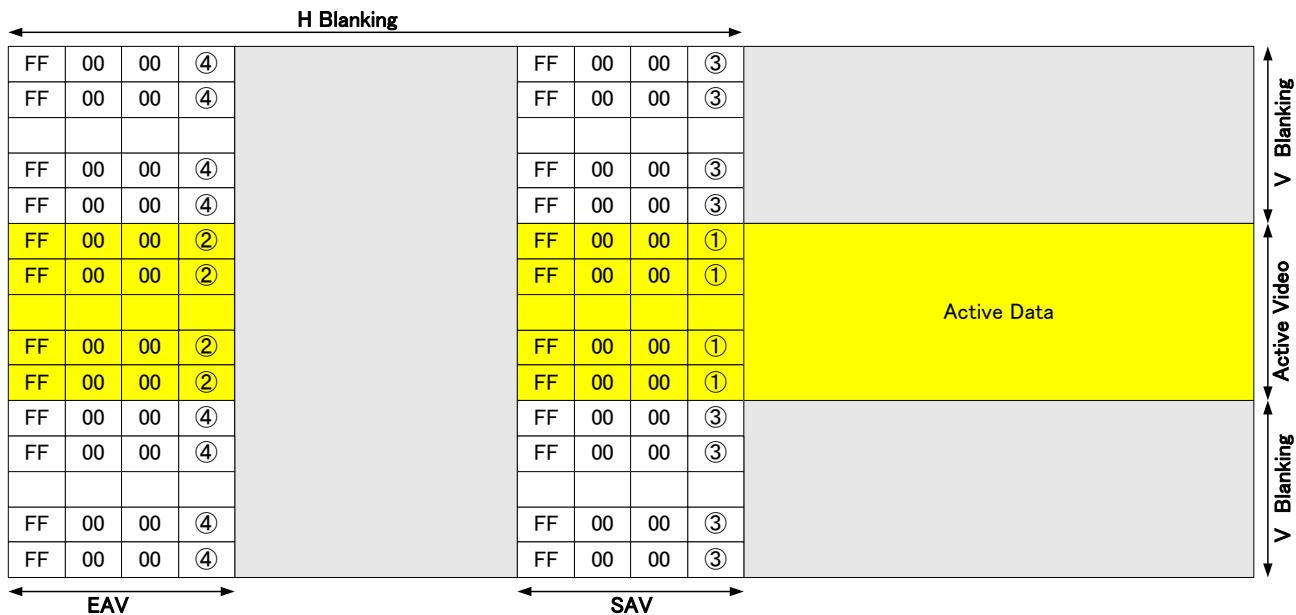


Fig. 8-3. Image Drawing of Inserted SAV/EAV Position

Table 8-4. TRC 4th Code

	7(MSB) (Fixed)	6 (F)	5 (V)	4 (H)	3 (P3)	2 (P2)	1 (P1)	0(LSB) (P0)	Hex
①	1	0	0	0	0	0	0	0	80
②	1	0	0	1	1	1	0	1	9D
③	1	0	1	0	1	0	1	1	AB
④	1	0	1	1	0	1	1	0	B6

F=0 during field 1

F=1 during field 2

V=0 during visible data

V=1 during field blanking

H=0 SAV

H=1 EAV

### 8-3-5. YCbCr Output Outline

The output sequence of YCbCr data is possible to change by register setting.

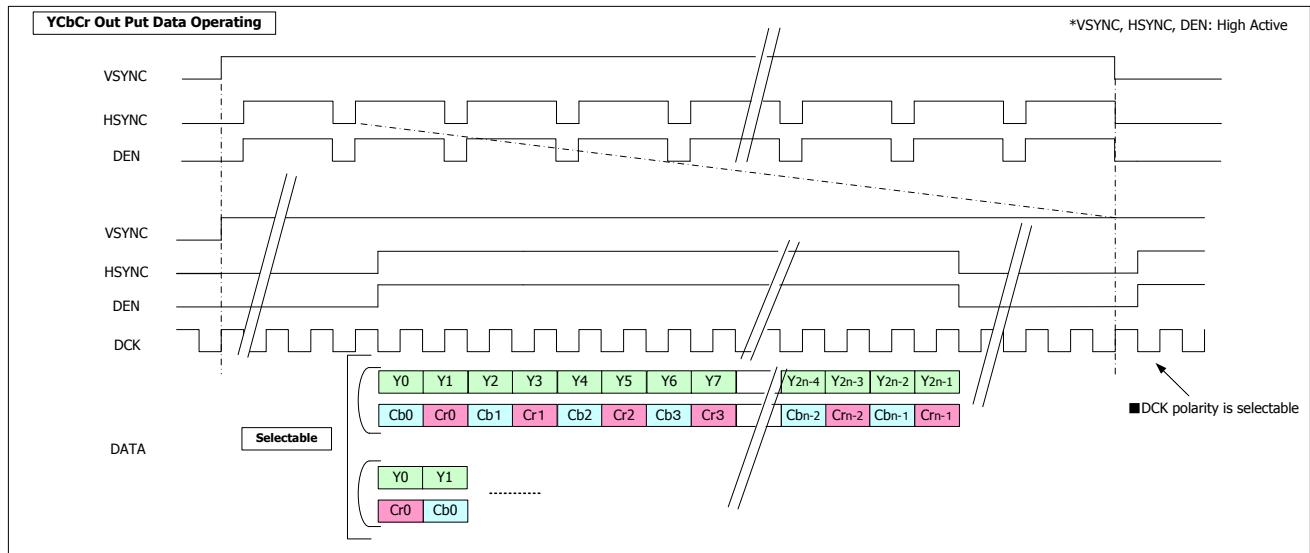


Fig. 8-4. YCbCr Output Specification

#### 8-4. Detailed Specification of Parallel Output Mode

The H / VSYNC pulse output timing and TRC timing for each output mode are shown below.

##### 8-4-1. Quad-VGA All-pixel Scan Mode (YCbCr)

The drive mode of Quad-VGA All-pixel scan mode in parallel output is shown in Table 8-5. For the detailed timing of each output mode, refer the Fig. number which is described on the table.

Table 8-5. Quad-VGA All-pixel Scan Output Mode

Output Mode		fps	I/P*1	Valid Size		Output Size		DCK [MHz]	Pulse	TRC
Picture Size	Mode			H	V	H	V			
Quad-VGA	Normal / Digital Overlap 2Frame	25	P	1280	960	1680	1125	47.25	Fig. 8-5	Fig. 8-7
		30	P			1400			Fig. 8-6	
		50	P			1680		94.5	Fig. 8-5	
		60	P			1400			Fig. 8-6	
	Digital Overlap 3Frame	25	P	1920	1500	1920	72	Fig. 8-8	Fig. 8-10	
		30	P			1600		Fig. 8-9		

\*1 I: Interlace, P: Progressive

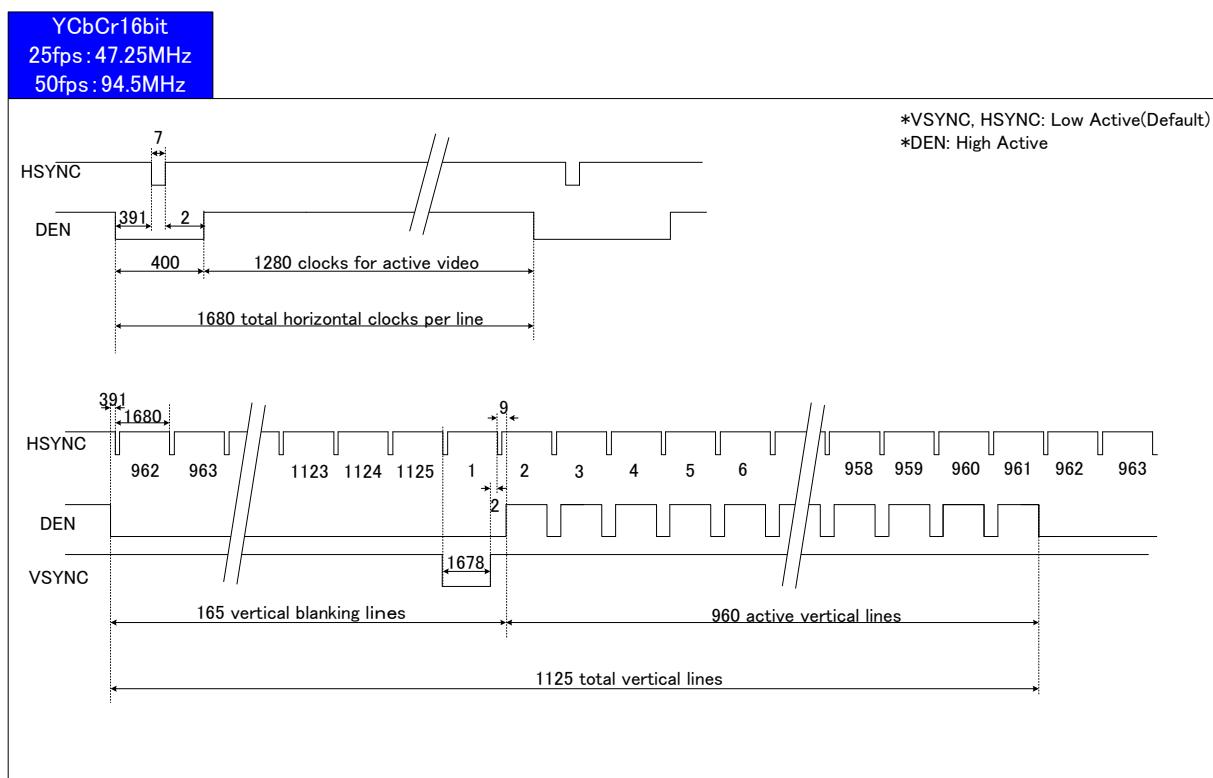


Fig. 8-5. Pulse Output Synchronous Signal Timing  
in Quad-VGA All-pixel Scan Output Mode, Normal / DOL2, 25/50fps

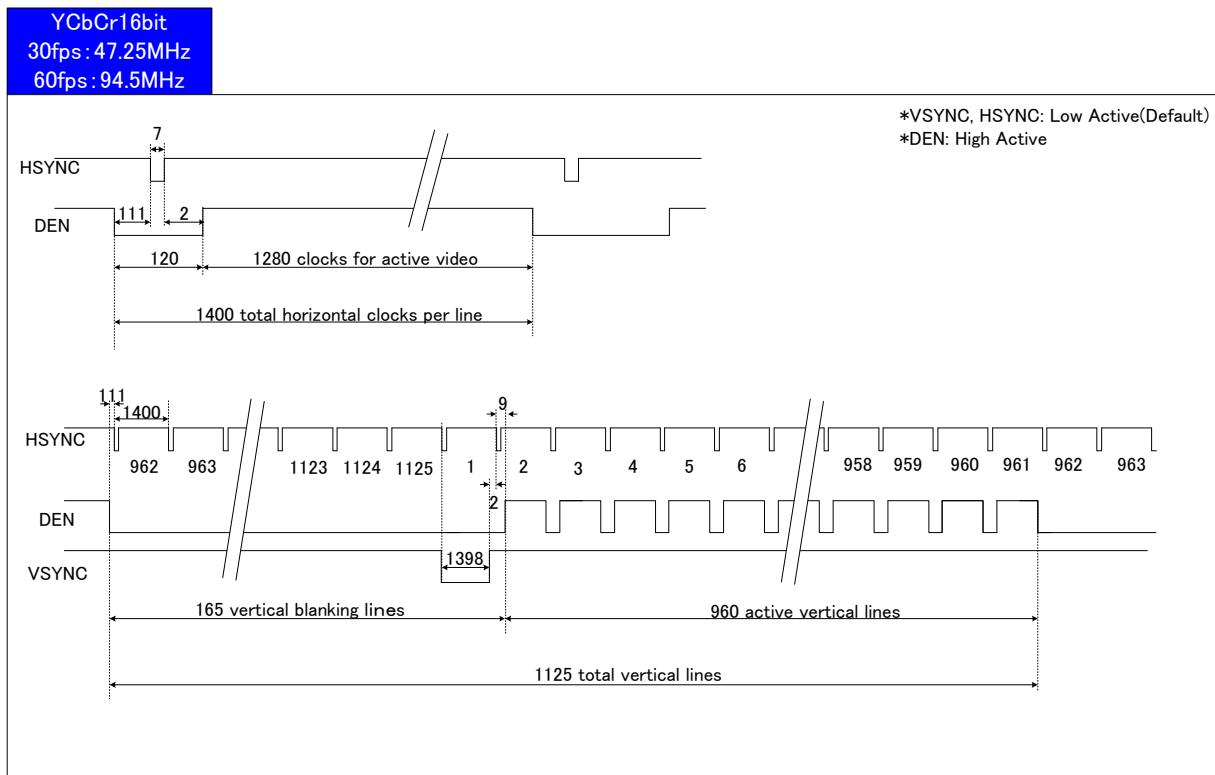


Fig. 8-6. Pulse Output Synchronous Signal Timing in Quad-VGA All-pixel Scan Output Mode, Normal / DOL2, 30/60fps

Fig. 8-7. TRC Timing in Quad-VGA All-pixel Scan Mode, Normal / DOL2

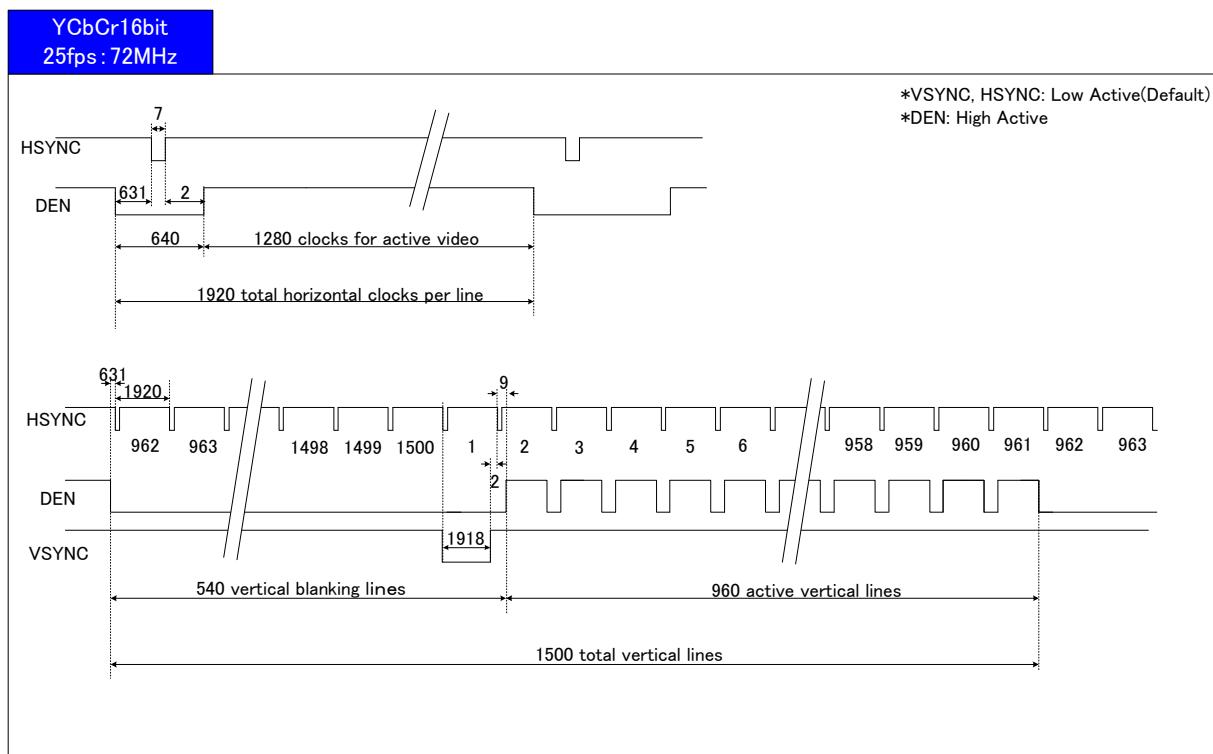


Fig. 8-8. Pulse Output Synchronous Signal Timing  
in Quad-VGA All-pixel Scan Output Mode, DOL3, 25fps

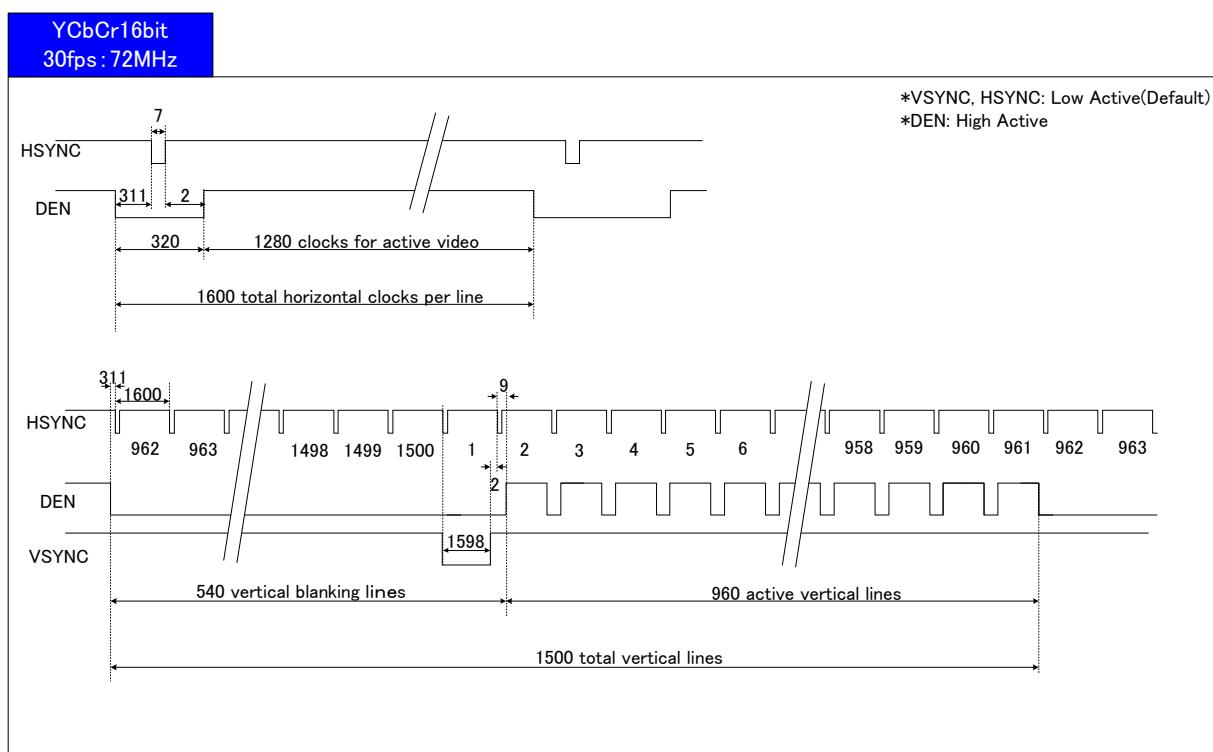


Fig. 8-9. Pulse Output Synchronous Signal Timing  
in Quad-VGA All-pixel Scan Output Mode, DOL3, 30fps

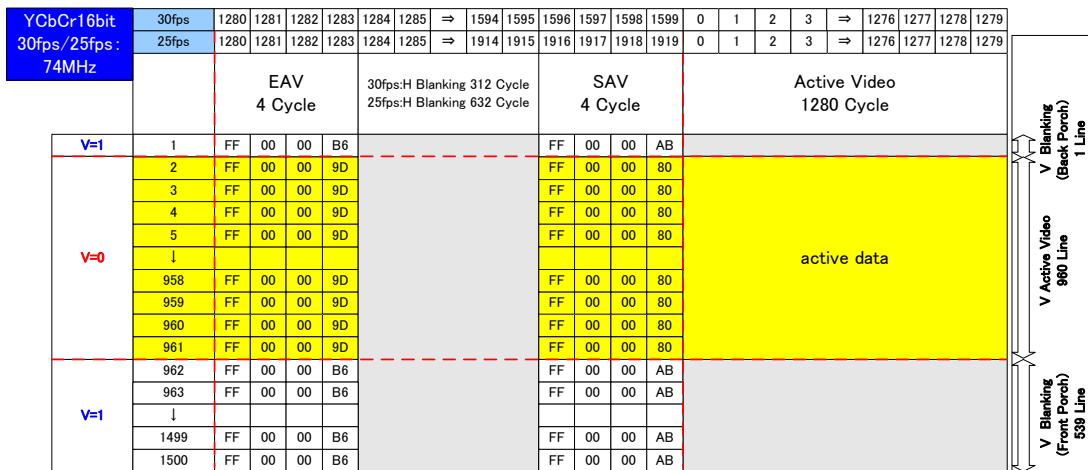


Fig. 8-10. TRC Timing in Quad-VGA All-pixel Scan Mode, DOL3

### 8-4-2. All-pixel Scan V800 Cropping Mode (YCbCr)

The drive mode of All-pixel scan V800 cropping mode in parallel output is shown in Table 8-6. For the detailed timing of each output mode, refer the Fig. number which is described on the table.

Table 8-6. All-pixel Scan V800 Cropping Mode

Picture Size	Output Mode	fps	I/P*1	Valid Size		Output Size		DCK [MHz]	Pulse	TRC
				H	V	H	V			
V800 Crop	Normal / Digital Overlay 2Frame	25	P	1280	800	1650	900	37.125	Fig. 8-11	Fig. 8-13
		30	P			1500		40.5	Fig. 8-12	
		50	P			1650		74.25	Fig. 8-11	
		60	P			1500		81	Fig. 8-12	
	Digital Overlay 3Frame	25	P			1650	1200	49.5	Fig. 8-14	Fig. 8-16
		30	P			1500		54	Fig. 8-15	

\*1 I: Interlace, P: Progressive

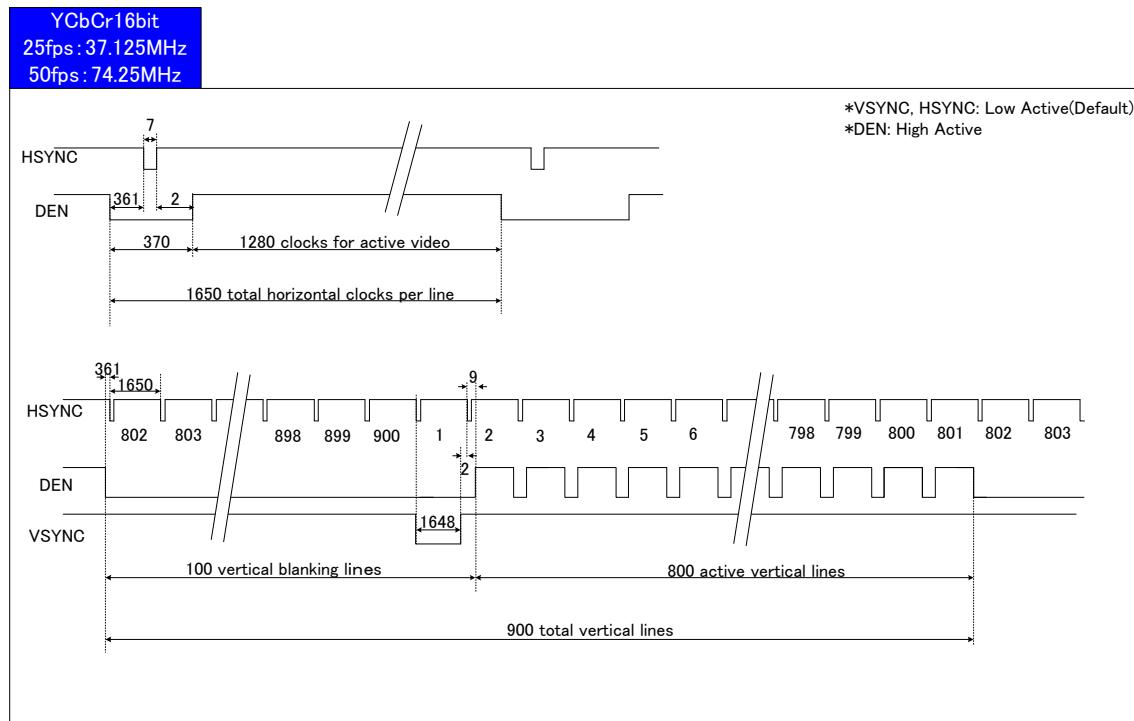


Fig. 8-11. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V800 Cropping Output Mode, Normal / DOL2, 25/50fps

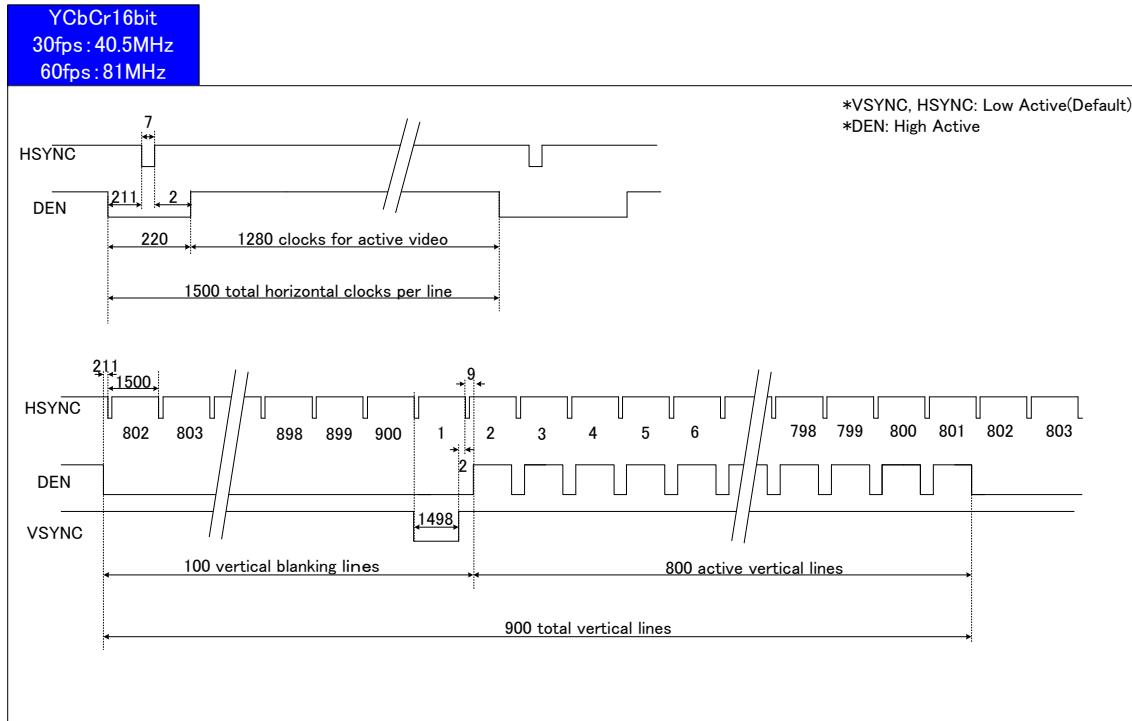


Fig. 8-12. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V800 Cropping Output Mode, Normal / DOL2, 30/60fps

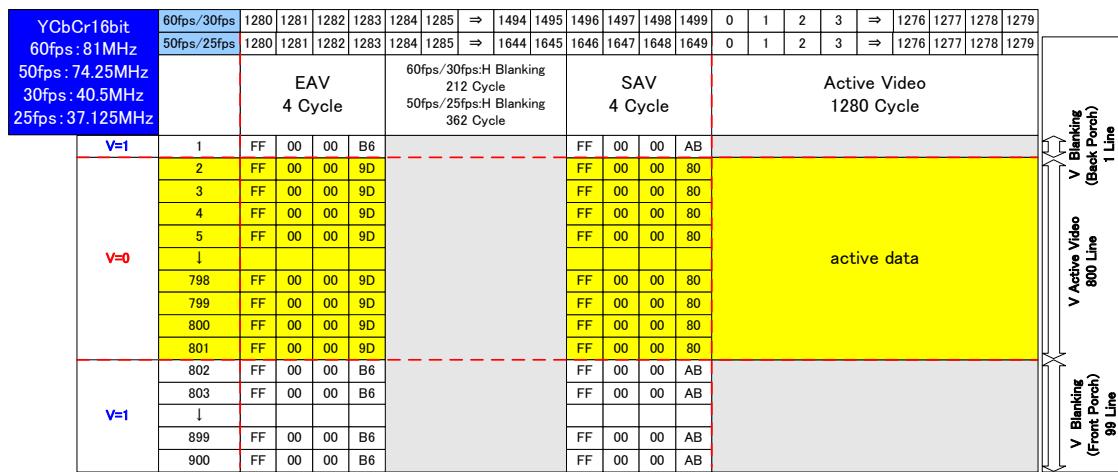


Fig. 8-13. TRC Timing in All-pixel Scan V800 Cropping Mode, Normal/DOL2

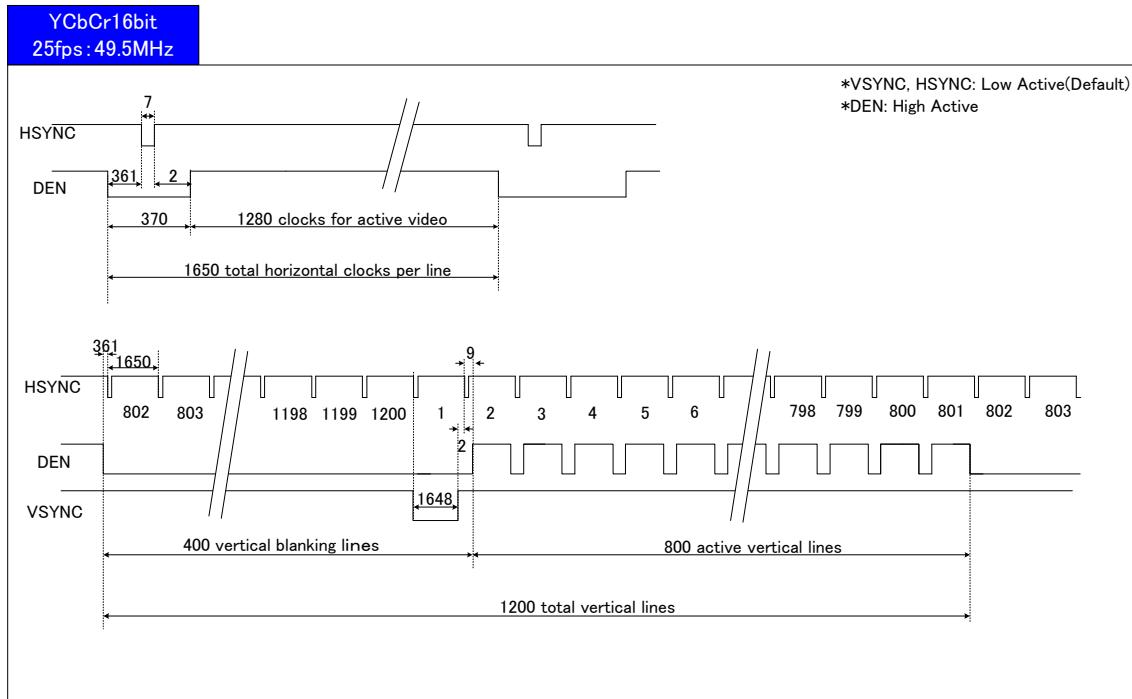


Fig. 8-14. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V800 Cropping Output Mode, DOL3, 25fps

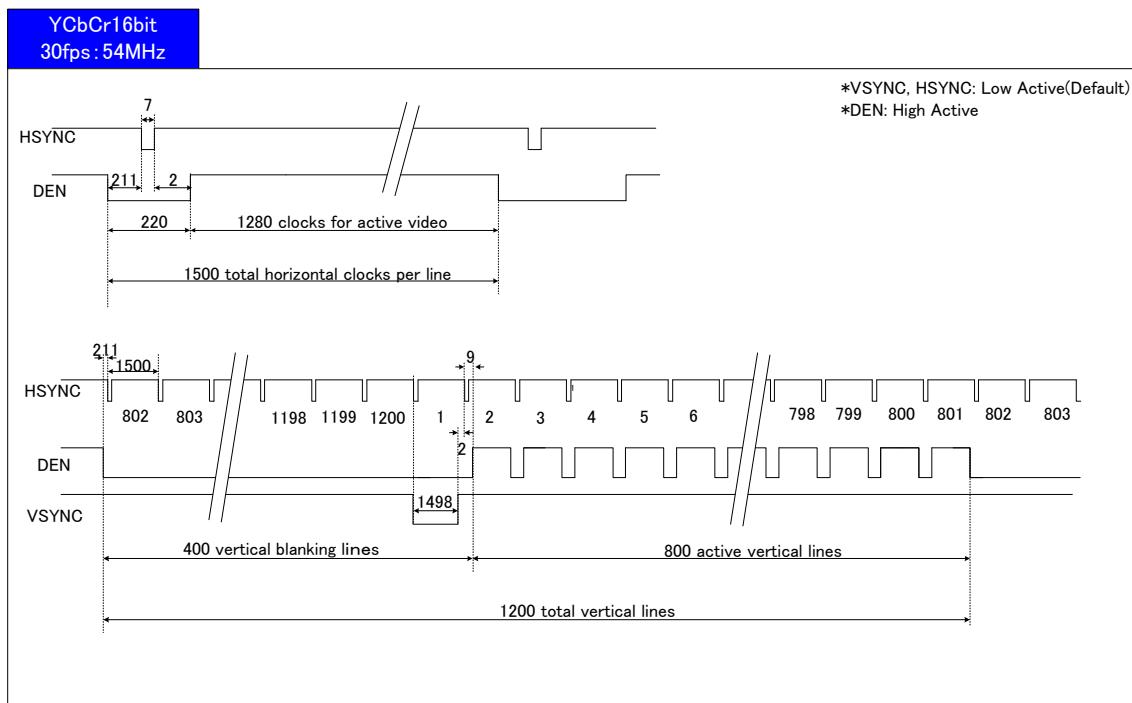


Fig. 8-15. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V800 Cropping Output Mode, DOL3, 30fps

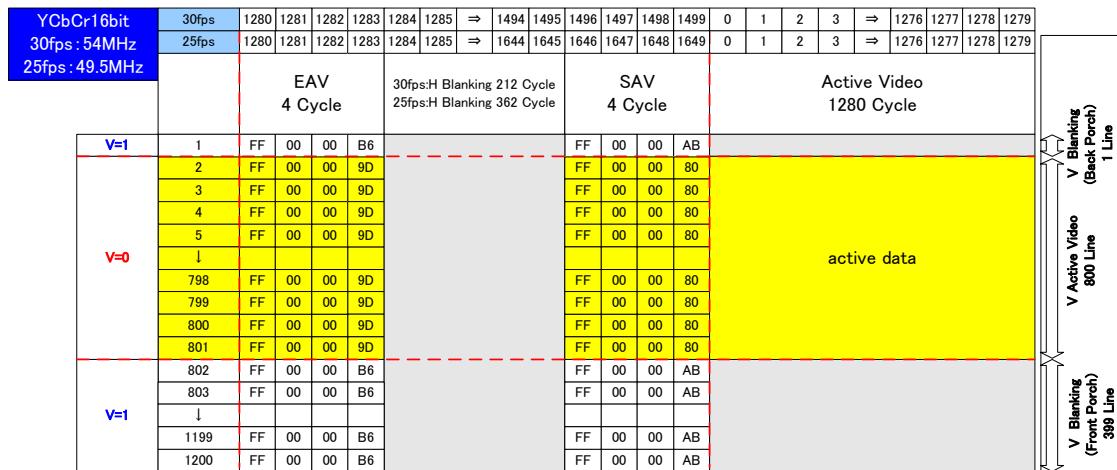


Fig. 8-16. TRC Timing in All-pixel Scan V800 Cropping Mode, DOL3

### 8-4-3. All-pixel Scan V720 Cropping Mode (YCbCr)

The drive mode of All-pixel scan V720 cropping mode in parallel output is shown in Table 8-7. For the detailed timing of each output mode, refer the Fig. number which is described on the table.

Table 8-7. All-pixel Scan V720 Cropping Mode

Picture Size	Output Mode	fps	I/P*1	Valid Size		Output Size		DCK [MHz]	Pulse	TRC
				H	V	H	V			
V720 Crop	Normal / Digital Overlay 2Frame	25	P	1280	720	1650	900	37.125	Fig. 8-17	Fig. 8-19
		30	P			1500		40.5	Fig. 8-18	
		50	P			1650		74.25	Fig. 8-17	
		60	P			1500		81	Fig. 8-18	
	Digital Overlay 3Frame	25	P			1650	1200	49.5	Fig. 8-20	Fig. 8-22
		30	P			1500		54	Fig. 8-21	

\*1 I: Interlace, P: Progressive

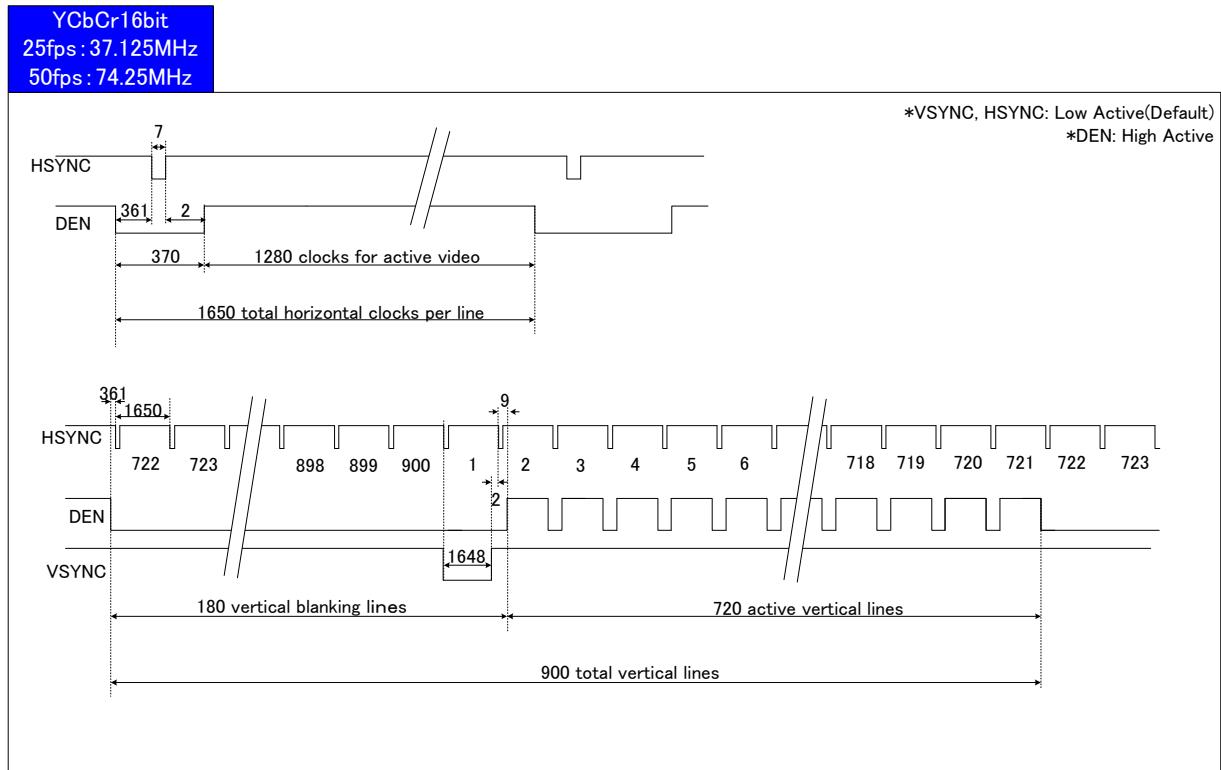


Fig. 8-17. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V720 Cropping Output Mode, Normal / DOL2, 25/50fps

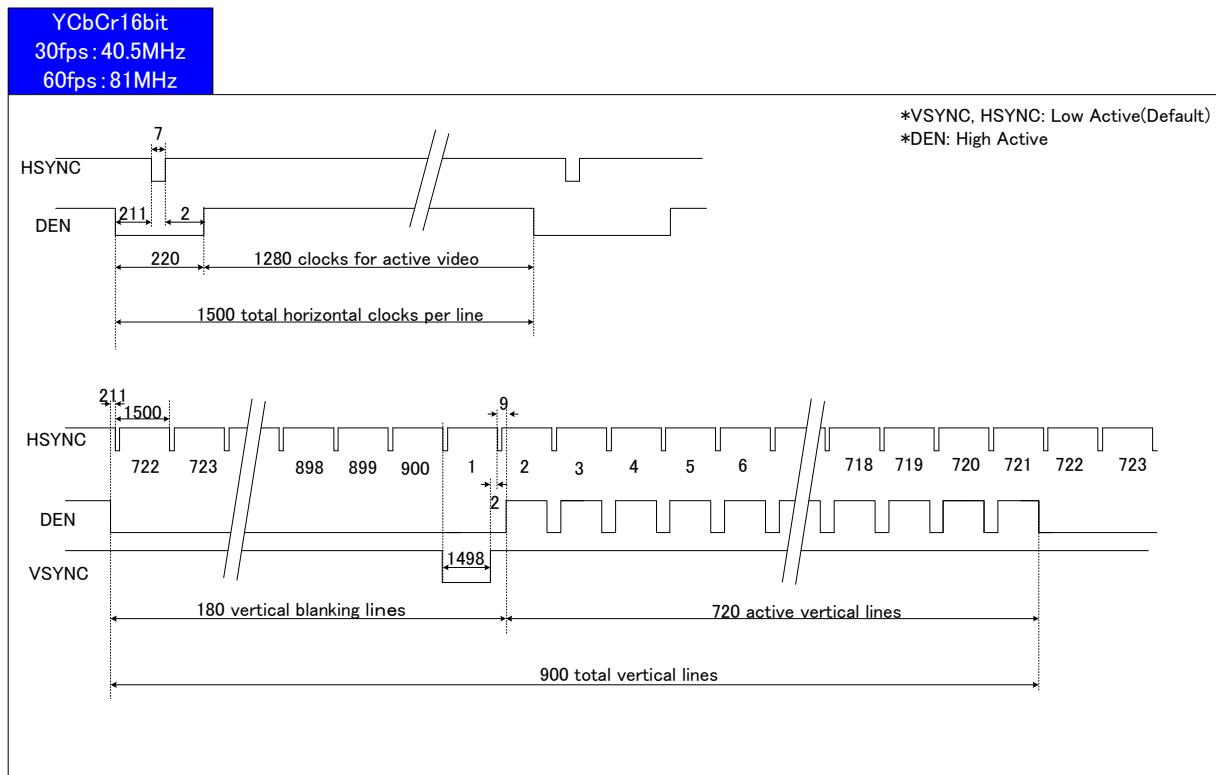


Fig. 8-18. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V720 Cropping Output Mode, Normal / DOL2, 30/60fps

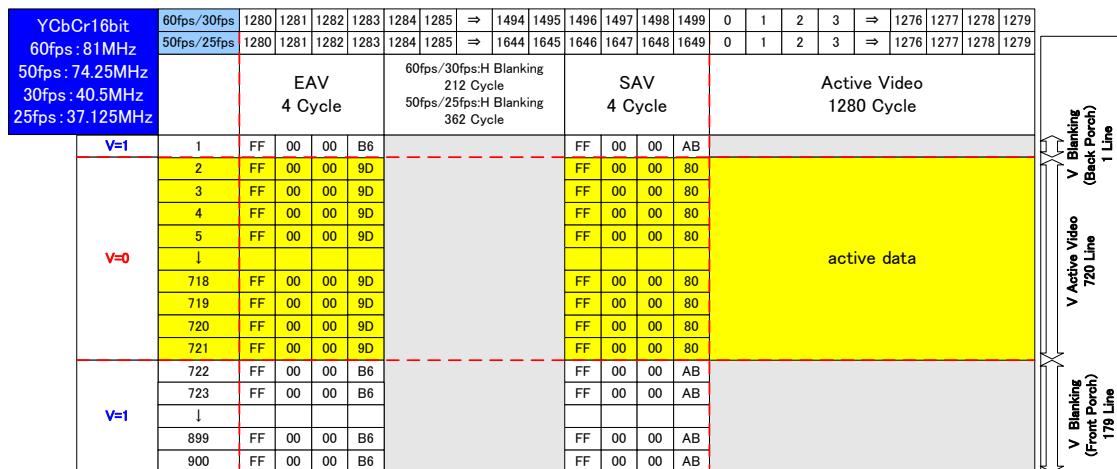


Fig. 8-19. TRC Timing in All-pixel Scan V720 Cropping Mode, Normal/DOL2

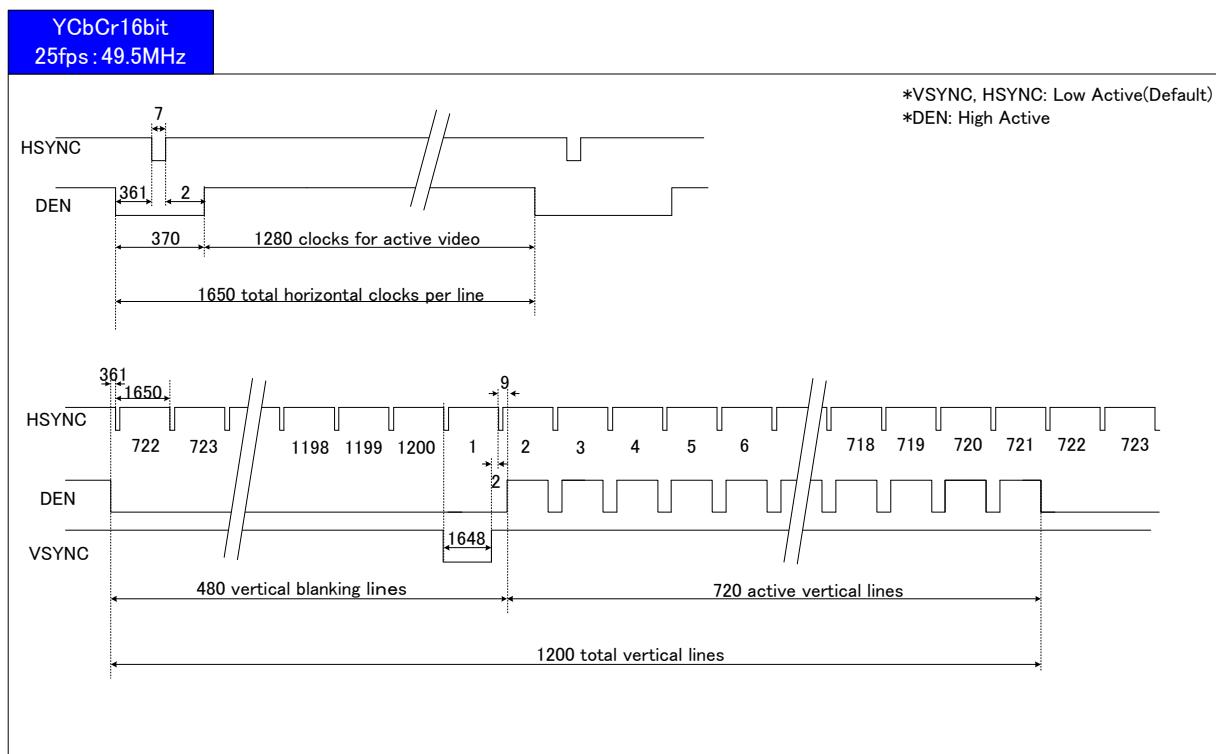


Fig. 8-20. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V720 Cropping Output Mode, DOL3, 25fps

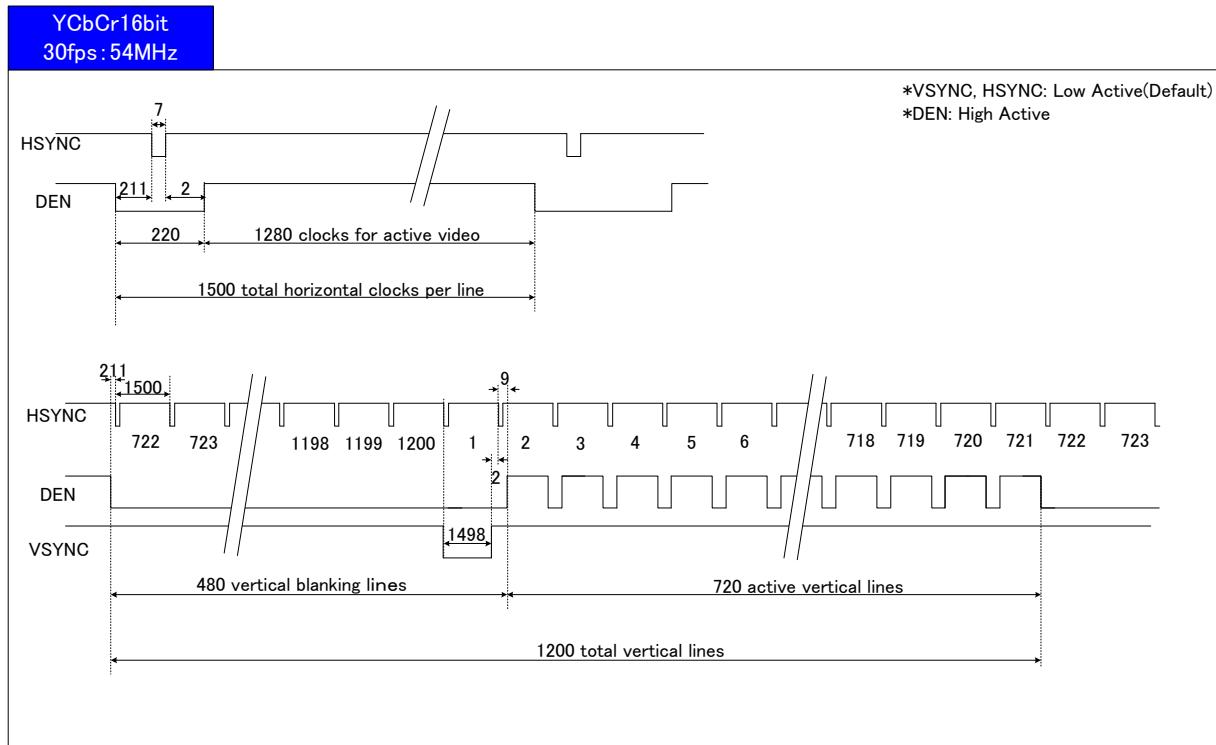


Fig. 8-21. Pulse Output Synchronous Signal Timing  
in All-pixel Scan V720 Cropping Output Mode, DOL3, 30fps

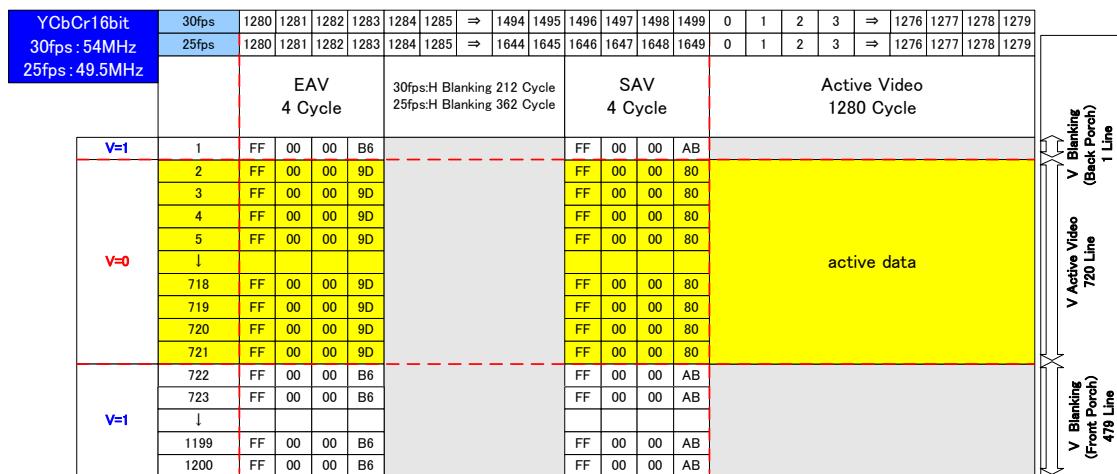


Fig. 8-22. TRC Timing in All-pixel Scan V720 Cropping Mode, DOL3

#### 8-4-4. HD720p (SMPTE296M) Output Mode (YCbCr)

The HD720p mode in parallel output is shown in Table 8-8. For the detailed timing of each output mode, refer the Fig. number which is described on the table.

Table 8-8. HD720p (SMPTE296M) Output Mode

Picture Size	Mode	fps	I/P*1	Valid Size		Output Size		DCK [MHz]	Pulse	TRC
				H	V	H	V			
HD720p SMPTE296M	Normal / Digital Overlap 2Frame	25	P	1280	720	3960	750	74.25	Fig. 8-23 Fig. 8-24 Fig. 8-25 Fig. 8-26	Fig. 8-27
		30	P			3300				
		50	P			1980				
		60	P			1650				

\*1 I: Interlace, P: Progressive

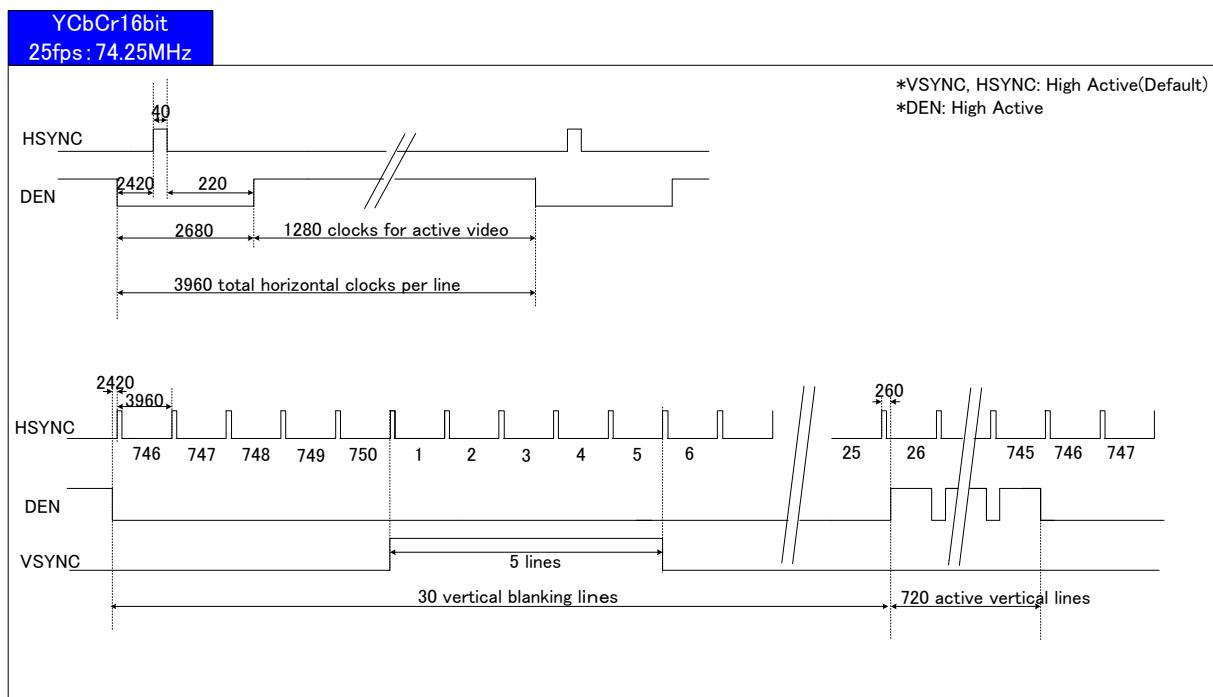


Fig. 8-23. Pulse Output Synchronous Signal Timing in HD720p (SMPTE296M) 25fps

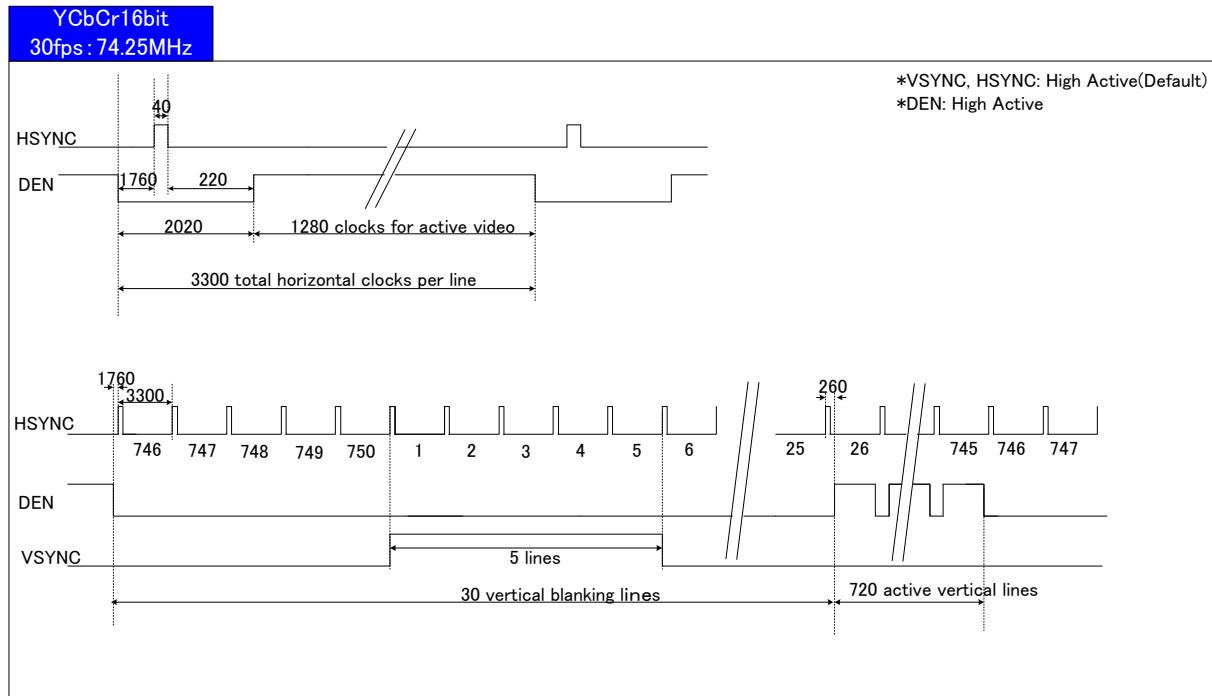


Fig. 8-24. Pulse Output Synchronous Signal Timing in HD720p (SMPTE296M) 30fps

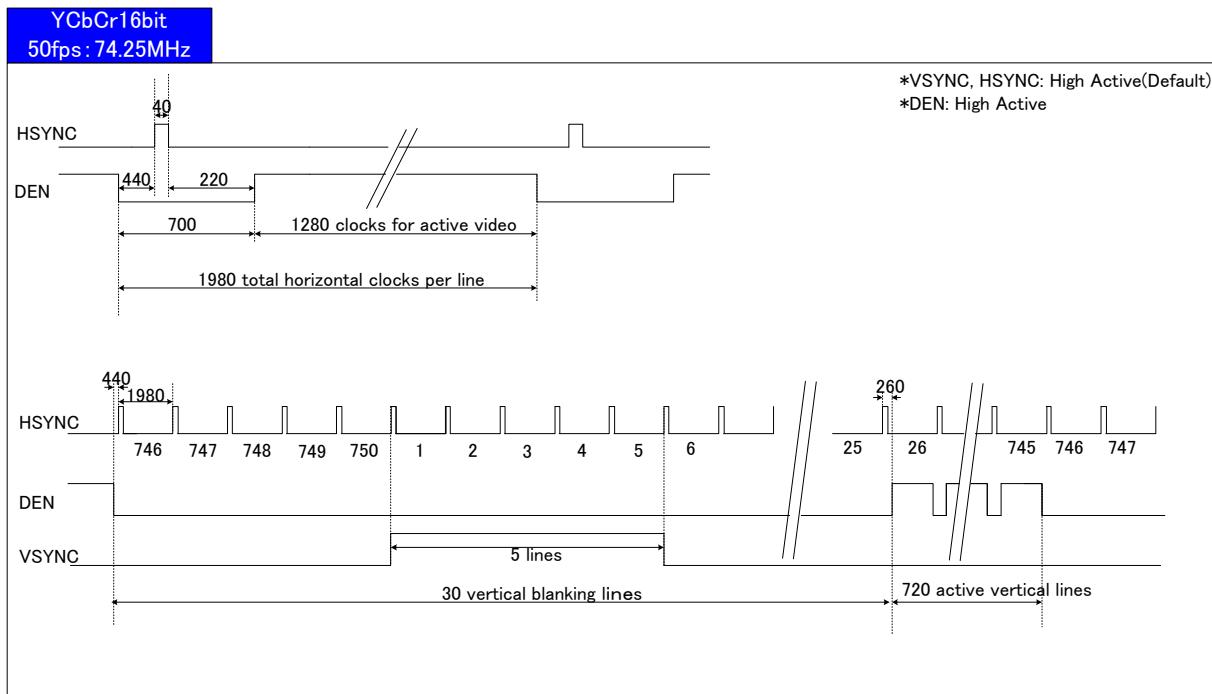


Fig. 8-25. Pulse Output Synchronous Signal Timing in HD720p (SMPTE296M) 50fps

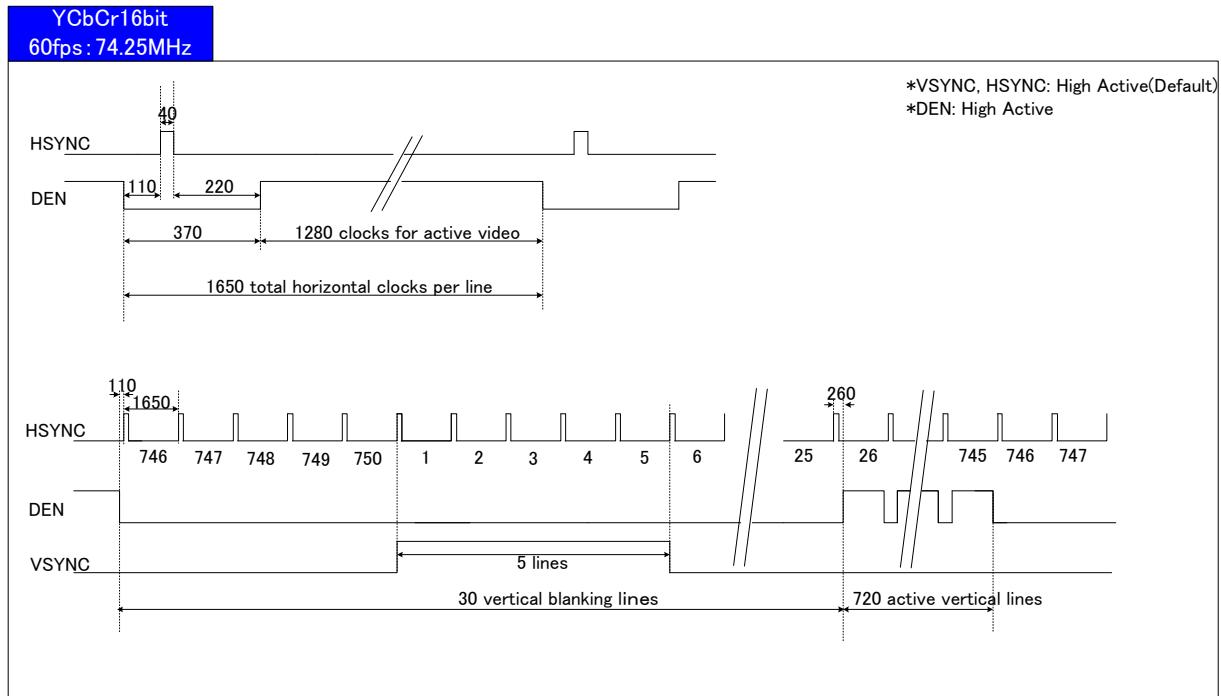


Fig. 8-26. Pulse Output Synchronous Signal Timing in HD720p (SMPTE296M) 60fps

YCbCr16bit 74.25MHz	60fps	1280	1281	1282	1283	1284	1285	$\Rightarrow$	1644	1645	1646	1647	1648	1649	0	1	2	3	$\Rightarrow$	1276	1277	1278	1279
	50fps	1280	1281	1282	1283	1284	1285	$\Rightarrow$	1974	1975	1976	1977	1978	1979	0	1	2	3	$\Rightarrow$	1276	1277	1278	1279
	30fps	1280	1281	1282	1283	1284	1285	$\Rightarrow$	3294	3295	3296	3297	3298	3299	0	1	2	3	$\Rightarrow$	1276	1277	1278	1279
	25fps	1280	1281	1282	1283	1284	1285	$\Rightarrow$	3954	3955	3956	3957	3958	3959	0	1	2	3	$\Rightarrow$	1276	1277	1278	1279
		EAV 4 Cycle				60fps:H Blanking 362 Cycle 50fps:H Blanking 692 Cycle 30fps:H Blanking 2012 Cycle 25fps:H Blanking 2672 Cycle				SAV 4 Cycle				Active Video 1280 Cycle									
<b>V=1</b>	1	FF	00	00	B6				FF	00	00	AB											
	2	FF	00	00	B6				FF	00	00	AB											
	↓								FF	00	00	AB											
	24	FF	00	00	B6				FF	00	00	AB											
	25	FF	00	00	B6				FF	00	00	AB											
<b>V=0</b>	26	FF	00	00	9D				FF	00	00	80											
	27	FF	00	00	9D				FF	00	00	80											
	↓								FF	00	00	80											
	744	FF	00	00	9D				FF	00	00	80											
	745	FF	00	00	9D				FF	00	00	80											
<b>V=1</b>	746	FF	00	00	B6				FF	00	00	AB											
	747	FF	00	00	B6				FF	00	00	AB											
	748	FF	00	00	B6				FF	00	00	AB											
	749	FF	00	00	B6				FF	00	00	AB											
	750	FF	00	00	B6				FF	00	00	AB											

V Blanking (Back Porch) 25 Line  
 V Active Video 720 Line  
 V Blanking (Front Porch) 5 Line

Fig. 8-27. TRC Timing in HD720p (SMPTE296M)

## 8-5. MIPI I/F

### 8-5-1. Description

The ISX017 has MIPI interface, so it can be output from YCbCr format. And, the number of MIPI output Lane is supported either 2-Lane or 4-Lane. The maximum transfer rate per 1-Lane is 756 Mbps/Lane. Note that the MIPI interface is corresponding to progressive output only.

### 8-5-2. Output Pins

The MIPI interface pins are shown in Fig. 8-28.

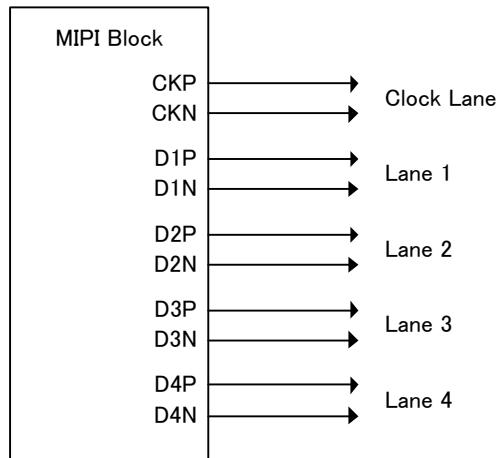


Fig. 8-28 MIPI Output Pins

The signal data is output as differential signal of 1 bit data which was conform to standard;  
MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Ver1.01.00,  
MIPI Alliance Specification for D-PHY Version 1.00.00.

### 8-5-3. YCbCr Output Diagram

The output image diagram of YCbCr output in MIPI format is shown in Fig. 8-29. The YCbCr data is output in the following order: Cb, Y, Cr, Y. Data Type in Packet Header is 0x1E (YUV422 8bit). First, Frame Start Packet is transmitted. Next, the YCbCr data is output. Then, transmission of 1 frame data is finished after transmitting the Frame End packet.

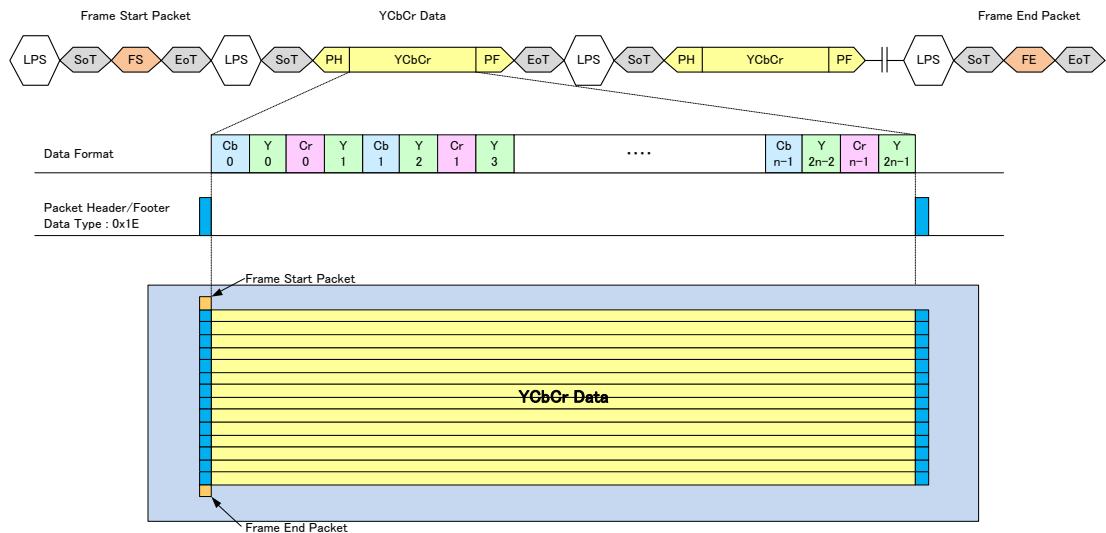


Fig. 8-29. MIPI I/F YCbCr Output Mode

### 8-5-4. RAW Output Diagram

The output image diagram of YCbCr output in MIPI format is shown in Fig. 8-30. The RAW data is output in the raster order. Data Type in Packet Header is 0x1E (YUV422 8bit). First, Frame Start Packet is transmitted. Next, the YCbCr data is output. Then, transmission of 1 frame data is finished after transmitting the Frame End packet.

In addition, the RGBW output after converting to the Bayer data by remosaicing.

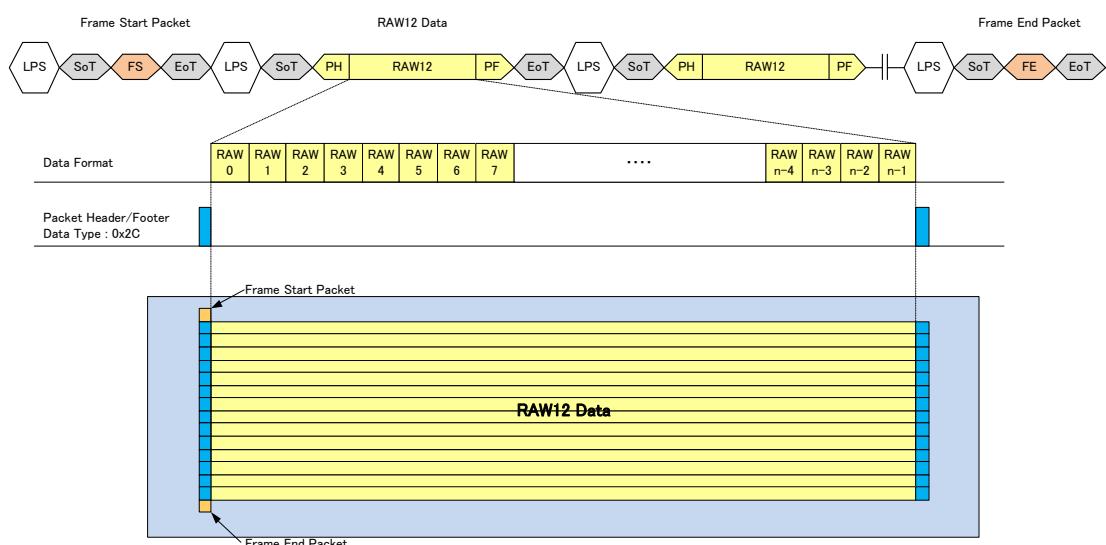


Fig. 8-30. MIPI I/F RAW Output Mode

### 8-6. Detailed Specification of MIPI Output Mode

The transfer rate of MIPI for each output mode in MIPI YCbCr is shown in Table 8-9 - Table 8-12.

Table 8-9 MIPI YCbCr Quad-VGA All-pixel Scan Mode

Picture Size	Mode	fps	I/P*1	Valid Size		MIPI Lane	Output Rate per Lane [Mbps/Lane]	Total Output Rate [Mbps]
				H	V			
Quad-VGA	Normal / Digital Overlap 2Frame	25	P	1280	960	2	378	756
			P			4	378	1512
		30	P			2	378	756
			P			4	378	1512
		50	P			2	756	1512
			P			4	432	1728
		60	P			2	756	1512
			P			4	432	1728
	Digital Overlap 3Frame	25	P	1280	960	2	576	1152
			P			4	288	1152
		30	P			2	576	1152
			P			4	288	1152

\*1 I: Interlace, P: Progressive

Table 8-10. MIPI YCbCr All-pixel Scan V800 Cropping Mode

Picture Size	Mode	fps	I/P*1	Valid Size		MIPI Lane	Output Rate per Lane [Mbps/Lane]	Total Output Rate [Mbps]
				H	V			
V800 Crop	Normal / Digital Overlap 2Frame	25	P	1280	800	2	297	594
			P			4	297	1188
		30	P			2	324	648
			P			4	324	1296
		50	P			2	594	1188
			P			4	297	1188
		60	P			2	648	1296
			P			4	324	1296
	Digital Overlap 3Frame	25	P	1280	800	2	396	792
			P			4	396	1584
		30	P			2	432	864
			P			4	216	864

\*1 I: Interlace, P: Progressive

Table 8-11. MIPI YCbCr All-pixel Scan V720 Cropping Mode

Output Mode		fps	I/P*1	Valid Size		MIPI Lane	Output Rate per Lane [Mbps/Lane]	Total Output Rate [Mbps]
Picture Size	Mode			H	V			
V720 Crop	Normal / Digital Overlay 2Frame	25	P	1280	720	2	297	594
			P			4	297	1188
		30	P			2	324	648
			P			4	324	1296
		50	P			2	594	1188
			P			4	297	1188
		60	P			2	648	1296
			P			4	324	1296
	Digital Overlay 3Frame	25	P			2	396	792
			P			4	396	1584
		30	P			2	432	864
			P			4	216	864

\*1 I: Interlace, P: Progressive

Table 8-12. HD720p (SMPTE296M) Mode

Output Mode		fps	I/P*1	Valid Size		MIPI Lane	Output Rate per Lane [Mbps/Lane]	Total Output Rate [Mbps]
Picture Size	Mode			H	V			
HD720p	Normal / Digital Overlay 2Frame	25	P	1280	720	2	594	1188
			P			4	297	1188
		30	P			2	594	1188
			P			4	297	1188
		50	P			2	594	1188
			P			4	297	1188
		60	P			2	594	1188
			P			4	297	1188

\*1 I: Interlace, P: Progressive

The transfer rate of MIPI for each output mode in MIPI RAW is shown in Table 8-13.

Table 8-13. MIPI RAW Output Mode

Output Mode		fps	I/P*1	Valid Size		MIPI Lane	Output Rate per Lane [Mbps/Lane]	Total Output Rate [Mbps]
Picture Size	Mode			H	V			
Quad-VGA	Normal / Digital Overlap 2Frame	25	P	1296	976	2	324	648
			P			4	324	1296
		30	P			2	324	648
			P			4	324	1296
		50	P			2	648	1296
			P			4	324	1296
		60	P			2	648	1296
			P			4	324	1296
	Digital Overlap 3Frame	25	P			2	432	864
			P			4	216	864
		30	P			2	432	864
			P			4	216	864

\*1 I: Interlace, P: Progressive

## 8-7. Analog Interface

### 8-7-1. Description

The ISX017 has an analog interface, so it can be output the analog composite video-out. It outputs conforming to following standards: the NTSC is standard of SMPTE170M, and the PAL is standard of BT1700. Note that the analog interface is corresponding to interlace output only.

### 8-7-2. Output Pins

The output pin of the analog output is shown in Fig. 8-31. The analog composite output is output from VDAOUP pin.

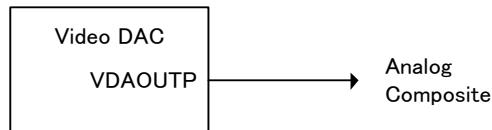


Fig. 8-31. Analog Composite Output Pin

## 8-8. Detailed Specification of Analog Output Mode

The output mode of the analog output is shown in Table 8-14. There are three kind of output mode which frequency differ in both NTSC and PAL each. Effective output image is conforming to the output standard, but the resolutions will be different image because these sampling frequencies are different.

Table 8-14. Analog Output Mode

Analog Spec	Output Mode		fps	I/P*1	Sampling Frequency [MHz]	Video Spec
	Picture H Size	Mode				
NTSC	1280	Normal / Digital Overlap 2Frame	59.94	I	45	SMPTE170M
	960			I	36	
	720			I	27	
PAL	1280	Normal / Digital Overlap 2Frame	50	I	45	BT1700
	960			I	36	
	720			I	27	

\*1 I: Interlace, P: Progressive

## 9. Power-on/off Sequence

The power-on / off sequences are shown below. Do not supply voltage to each I/O pin when the ISX017 is power-off state.

### 9-1. Power-on Sequence (Auto mode determination)

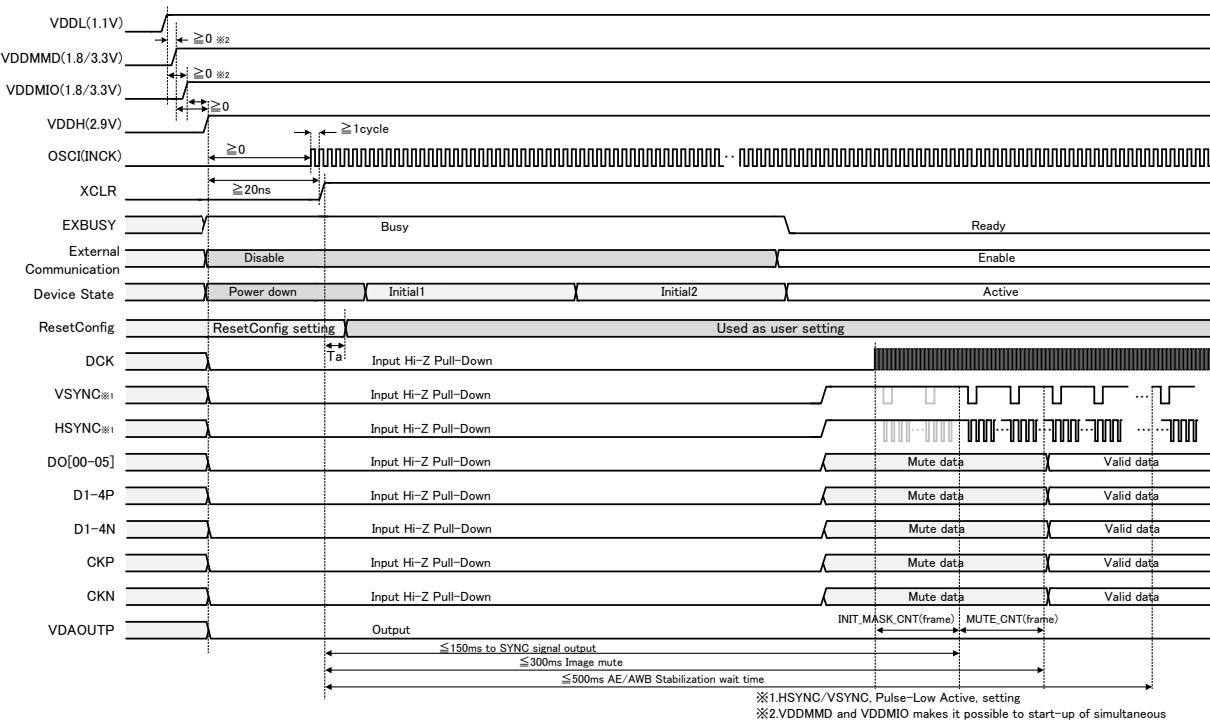


Fig. 9-1. Power-on Sequence of Parallel Output (Auto mode determination)

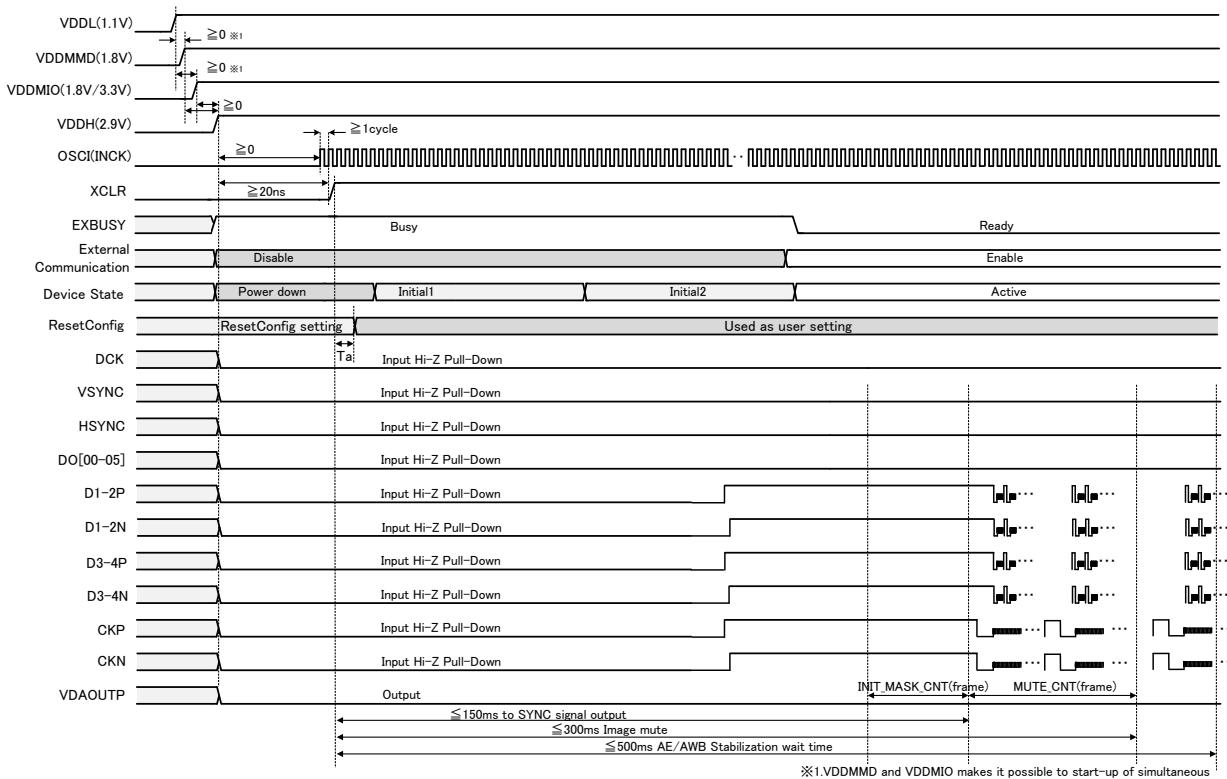


Fig. 9-2. Power-on Sequence of MIPI Output (Auto mode determination)

This section describes the power-on sequence specified in advance by Reset Config / Serial-Flash.

First, turn On the power supplies in the following order: VDDL (1.1 V) → VDDMMMD (1.8 / 3.3 V) → VDDMIO (1.8 / 3.3 V) → VDDH (2.9 V). Then start inputting INCK. Hold XCLR at the Low level for 1 cycle or more after the power supplies and INCK input have stabilized. After XCLR cancel (after changed to High level), start-up processing will be started. (Initial 1). In addition, the signal from the Reset Config pin will be latched to determine the start-up default status when using XCR cancel timing. To achieve a stable latch, maintain the input signal for the Reset Config pin to a minimum of  $T_a$ -Min after the XCLR is cancelled. In addition, cancel the control for the Reset Config pin within  $T_b$ -Max after the XCLR is cancelled to use a normal GPIO after start-up. (For Reset Config, refer the section 9-4. ) Shift directly to processing Initial 2 after the processing of Initial 1 is completed. When Initial 2 is completed and changes to Active, the ISX017 will start outputting the output signals. During the first several frames, a specified number of invalid frames (Mute) are output, and then effective images will start to be output. In Active, EXBUSY will be Low, and the ISX016 will accept communications from the Host. However, if communications from the Host are received while communication is disabled, the response to the communication for each transmission type is shown below.

- UART : No response
- I<sup>2</sup>C : NACK
- SPI : No response

Table 9-1. Timing of Power-on sequence

Symbol	Description	Min.	Max.	Unit
T <sub>a</sub>	Reset Config pin input value holding period after XCLR is cancelled	500	T.B.D.	ns

## 9-2. Power-on Sequence (Manual mode determination)

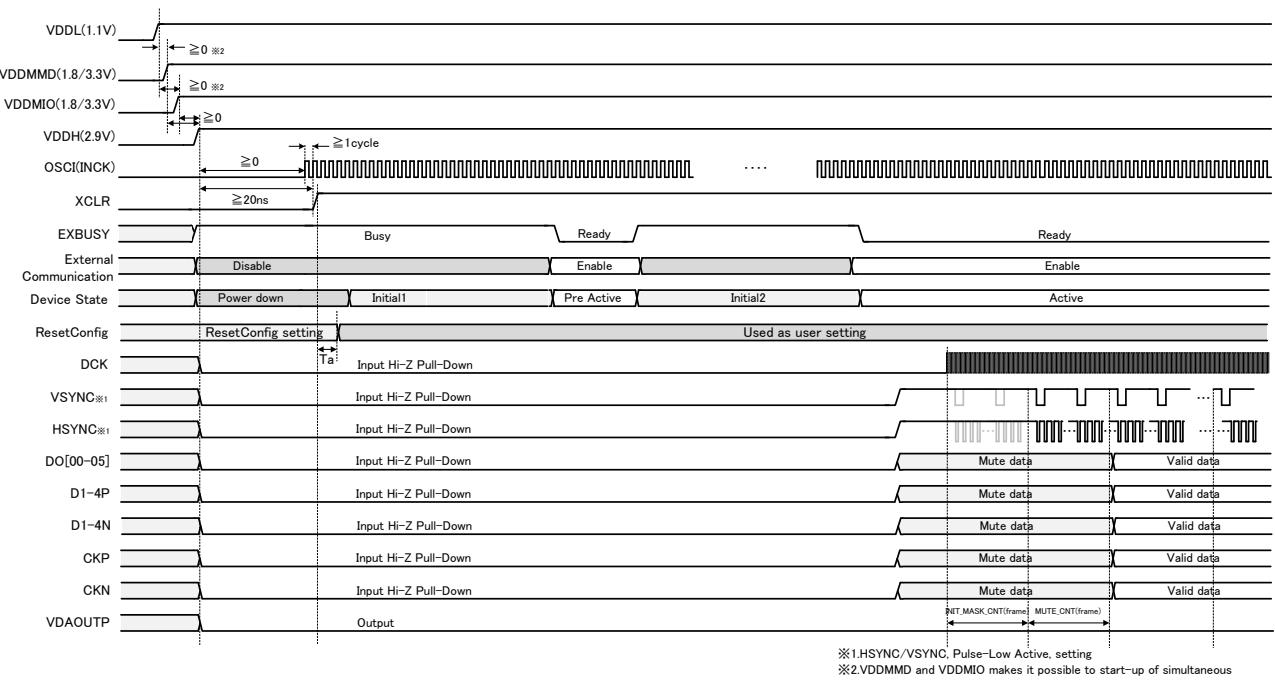


Fig. 9-3. Power-on Sequence of Parallel Output (Manual mode determination)

This section describes the power-on sequence for specified operation modes for HOST communications during start-up. This sequence is essentially the same as that in Chapter 9-1. (Auto mode determination). The difference is that PreActive exists between Initial 1 and Initial 2. In PreActive, EXBUSY will be Low level and it will be possible to communication from HOST. Here, it changes to the state that is waiting for designation of operation mode, and when the designation is complete, begins start-up sequence again according to the operating mode (Initial 2). The EXBUSY will be High level in Initial 2, and will not accept communication from the Host in this state. When Initial 2 is completed and changes to Active, then the ISX017 will start to output the output signals.

### 9-3. Power-off Sequence

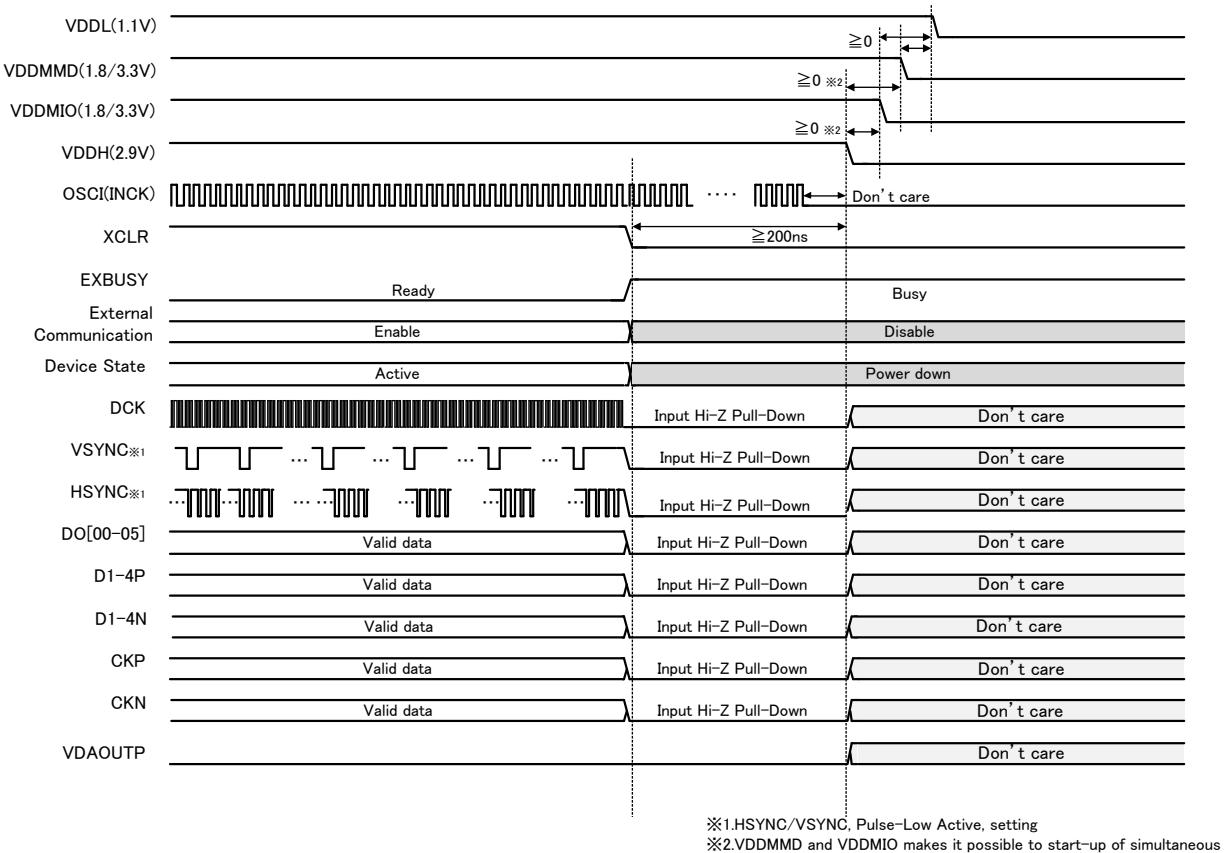


Fig. 9-4. Power-off sequence

If XCLR is set to enable (Low level), all signals will be stopped, and EXBUSY will be High level. After that, stop INCK inputs and turn Off the power supplies in the following order: VDDH (2.9 V) → VDDMIO (1.8 / 3.3 V) → VDDMMD (1.8 / 3.3 V) → VDDL (1.1 V).

#### 9-4. Reset Config

The ISX017 has a function that decides the system status after start-up according to the pin conditions after reset is cancelled. This function is achieved using GPIO2, HSYNC, and DO00 to DO05. The details are shown below.

Table 9-2. Functions determined by Reset Config

Function	PIN	Description															
Operating mode	DO00 HSYNC	Select from 4 modes that set in advance by Serial-Flash															
I <sup>2</sup> C slave address	DO01 DO02	Possible to select the I <sup>2</sup> C Slave address from four of the followings. In addition, possible to set arbitrary address to Serial-Flash.  <table border="1"><thead><tr><th>DO01</th><th>DO02</th><th>Slave Address</th></tr></thead><tbody><tr><td>Low</td><td>Low</td><td>0x18</td></tr><tr><td>Low</td><td>High</td><td>0x19</td></tr><tr><td>High</td><td>Low</td><td>0x1A</td></tr><tr><td>High</td><td>High</td><td>0x1B</td></tr></tbody></table>	DO01	DO02	Slave Address	Low	Low	0x18	Low	High	0x19	High	Low	0x1A	High	High	0x1B
DO01	DO02	Slave Address															
Low	Low	0x18															
Low	High	0x19															
High	Low	0x1A															
High	High	0x1B															
Communication Method	DO03 DO04 DO05	Select external communication method from followings. UART / I <sup>2</sup> C / SPI															
Debug/TEST	GPIO2 FSYNC VSYNC	Don't drive High.															

## 10. Device Status

The ISX017 has the following device statuses: Initial1, PreActive, Initial2, and Active.

When turning the power on, the ISX017 system sets the device status as Initial1 as the default. The device status when the power is on can be read by accessing the status register from the HOST, unless the BUSY signal is High.

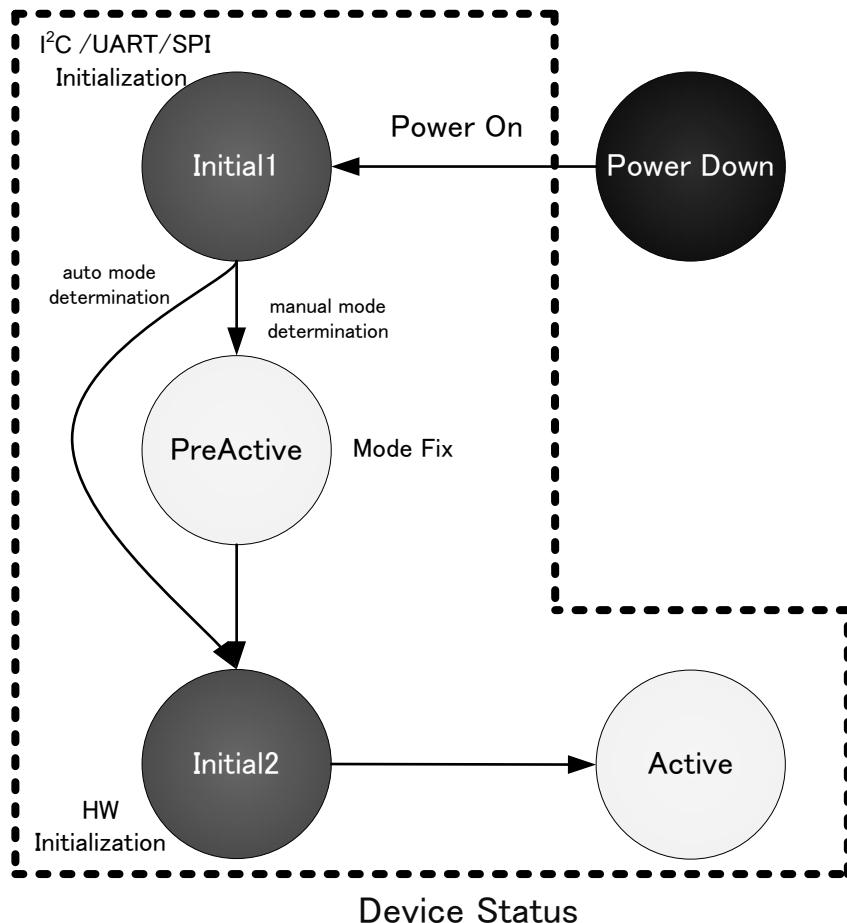


Fig. 10-1. Device status transitions

Table 10-1. Device Status and Transition Destination

Status	Description	Transition Destination
Initial1	Operated by INCK, set control communication channel, and initialize external pins.	When output mode undetermined; PreActive
		When output mode is determined; Initial2
PreActive	Access from external Host via communication channel is receivable. PreActive condition will be kept until output mode is set via external communication channel.	Initial2
Initial2	Initialize PLL and image sensor. Each setting for output mode and various hardware blocks will be initialized.	Active
Active	Release BUSY condition, and access from external Host via communication channel is receivable. Start outputting SYNC signal, and image data will be output normally following Mute image data for certain period of time.	---

## 11. ISP Description

### 11-1. Outline

The ISP consists of a block that corrects the input data from the sensor, a block that generates the data for performing AF, AE and AWB control, a block that generates YC data and performs various picture quality corrections, and a block that converts the data according to the output format.

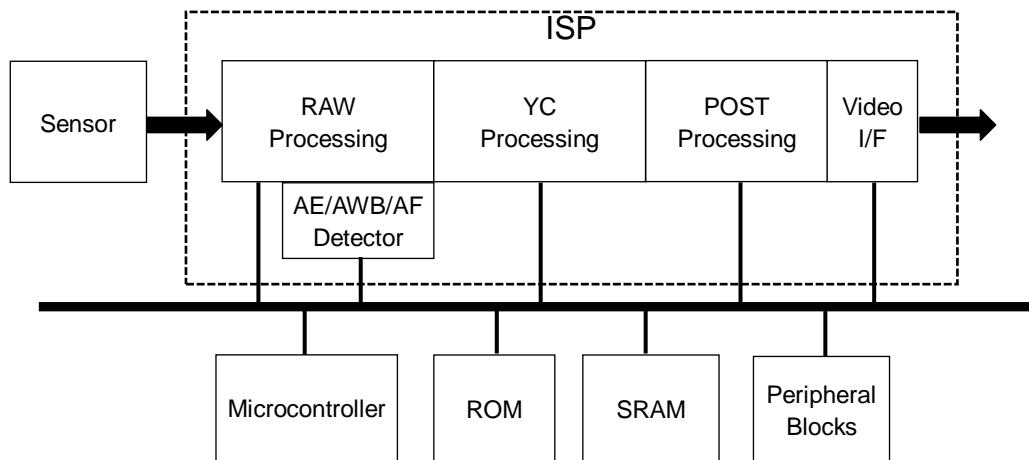


Fig. 11-1. ISP Data flow diagram

## 11-2. Signal Processing Block

The signal processing block configuration is as shown in the figure below.

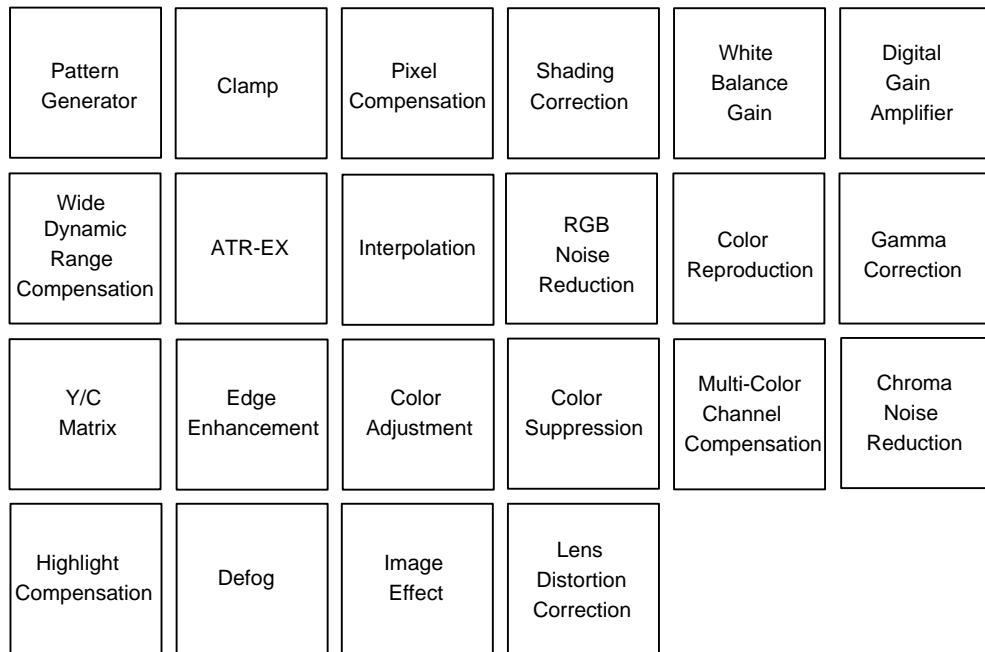


Fig. 11-2. Image signal processing blocks

### Pattern Generator

This system has four different built-in test patterns. Normally sensor image data is output passing through the sensor output, and the following image data can be output instead of image data per the setting.

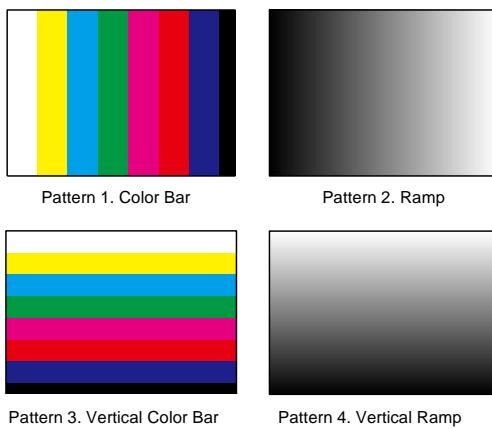


Fig. 11-3. Test Pattern

### Clamp

The image data is adjusted based on the calculation of optical black (OB) of the sensor block. The detected OB data is processed appropriately by the on-chip microcomputer, and the image data is controlled by changing the clamp value to achieve the optimum picture.

### Defect Correction

This function dynamically compensates for white and black pixels. This dynamic compensation discriminates between the white and black pixels automatically during operation. The correction number has no limit.

**Shading Correction**

Different shading correction can be applied to each color. In addition, a two-dimensional mesh-like shading gain can be set.

**White Balance Gain**

RGB gain is adjusted for each color to correct the sensitivity difference. This processing is used for white balance control. The appropriate gain setting is performed automatically based on the color temperature.

**Digital Gain Amplifier**

This function adjusts the overall gain, and is used when switching the camera sensitivity.

**WDR Composition**

Long exposure signals and short exposure signals from the sensor output are composed appropriately.

**Remosaicing**

This function after separating the IR component from the RGBW array, to convert the Bayer array from it.

**Gradation Correction (ATR-EX)**

This function compresses image data luminance range by detecting the distribution of brightness of the image frame data and automatically generating appropriate tone curve.

**Color Interpolation**

This function processes mosaic array data for all RGB color array data. This includes a circuit for suppressing false colors that are likely to occur during processing, but the image resolution will not be degraded.

**RGB Noise Reduction**

This function reduces noise on RGB signals. The appropriate adjustment is automatically performed during high sensitivity and in other cases when color noise easily appears.

**Color Reproduction Correction**

This function compensates for the spectral sensitivity of the sensor, and improves color reproducibility.

**Edge Enhancement**

This function performs edge enhancement processing by adjusting multiple frequency bands individually on both the horizontal and vertical axes.

**Gamma Correction**

This function performs gamma correction for each color signal. The gamma curve can be set arbitrarily.

**Y/C Conversion**

The R, G and B signals are converted to luminance and chrominance signals in this block.

**Color Adjustment**

This function adjusts hue and saturation in the color difference space.

**Chroma Suppression**

This function suppresses the chroma signal in high light areas, low light areas, low color saturation areas, and on the edges.

**Specific Color Correction**

This function compensates for the chroma signal in designated areas of the color difference space.

**Color Noise Reduction**

This function performs noise reduction for the chroma signal.

**Artifact Correction**

This function reduces artifacts seen on moving object when the WDR from composition is processed.

**Defog**

This function automatically detects foggy conditions and emphasizes the contrast.

**Highlight Correction**

This function modulates luminance gradation in high light areas and to make the areas visible.

**Image Effect**

In addition to normal image output, the following image effects can also be set.



Fig. 11-4. Image Effect

**Vignetting Correction**

Correct vignetting by stretching the image only in the horizontal direction according to the vertical position.

### 11-3. AE/AWB/AF Block

This block obtains the photometry data used for Auto Exposure, Auto White Balance, and Auto Focus control.

#### **AE Detection**

The AE Detection block provides necessary data for exposure control. The output data consists of the followings; the integrated value of the luminance signal within the area which divided by designated block size, and the histogram data which divided by designated luminance level.

#### **AWB Detection**

The AWB Detection block provides necessary data for the white balance control. The output data is the integrated value of the color signal within the area which divided by designated block size.

#### **AF Detection**

The AF Detection block provides necessary data for the contrast auto focus control. The output data is the integrated value of the high frequency component in the designated detection range.

#### 11-4. Post (Resize, Privacy Masking, On Screen Display), Video I/F Block

The POST block changes (reduces) the image size, displays the privacy mask or the font, and converts output format.

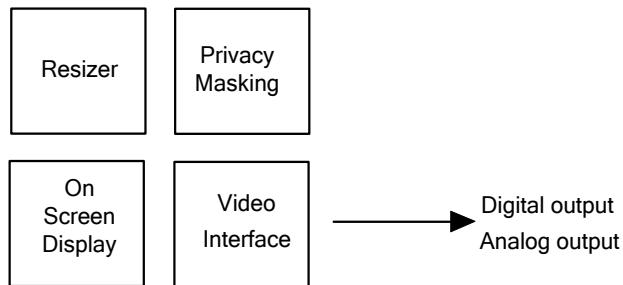


Fig. 11-5. Post blocks

##### Resize

This block reduces the image. It supports up to 1/2 the input image.

##### Privacy Mask

This function to conceal designated area by monochromatic or mosaic.  
It can designate up to 16 areas.

##### On Screen Display

This function displays the font as like menu onto the screen.  
It can be designated 455 kinds of font (English, French, German, Spanish, Russian, Portuguese, Simplified Chinese Character, Numerals and Symbols), and up to 40 kind of user-defined font.

##### Video Interface

Each signal is output by the format which is described in output format; the digital output which conformed to Rec.709 standard, the analog output which conformed to Rec.601 (NTSC / PAL), and so on.

---

## 12. Description of Camera Control

### 12-1. Outline

The ISX017 supports two camera auto modes as below.

- ◆ Auto Exposure
- ◆ Auto White Balance

### 12-2. Camera Automatic Control Function

#### Auto Exposure

Auto exposure (AE) dynamically controls the shutter speed, sensor analog gain, and the digital gain of the signal-processing block so that the image data is always a constant brightness. The brightness of the image data is evaluated from the data captured in a detection circuit. The detection circuit divides an image frame into multiple sections (areas), and controls exposure based on the luminance integral value within each area to realize the optimum brightness. The following four Auto Exposure algorithms can be selected.

- ◆ Average photometry
- ◆ Spot photometry
- ◆ Center-weighted photometry
- ◆ Histogram photometry

Average photometry performs control so that the average value (average detection value for the image) of the detection values obtained from the detection areas matches the target value.

Spot photometry performs control so that the detection value of the center frame matches the target value.

Center-weighted photometry performs control so that the average detection value for the image, obtained by giving the detection value of the center area a higher weighting among the detection values obtained from multiple detection areas, matches the target value.

Histogram photometry performs control to obtain an optimum exposure in various scenes by automatically changing weighting according to the distribution of detection values obtained from multiple detection areas and matches the target value.

AE performs control to keep the image brightness constant, and the target brightness can be corrected externally. The correction level is provided by an EV value, and correction can be performed in 0.3 EV steps from -2 EV to 2 EV.

#### Auto White Balance

Auto White Balance (AWB) controls the output levels of R, G, and B signals using software to control to the proper level so that the white balance of the image is maintained independently from the color temperature of the subject. The color temperature is estimated using data obtained from a detection circuit. The current color temperature is estimated from the color temperature obtained from the detection circuit and the control value (gain), and the gain is adjusted to enable the ideal color reproduction. The following Auto White Balance algorithms can be selected.

- ◆ AUTO
- ◆ Preset

### 13. Application Circuit

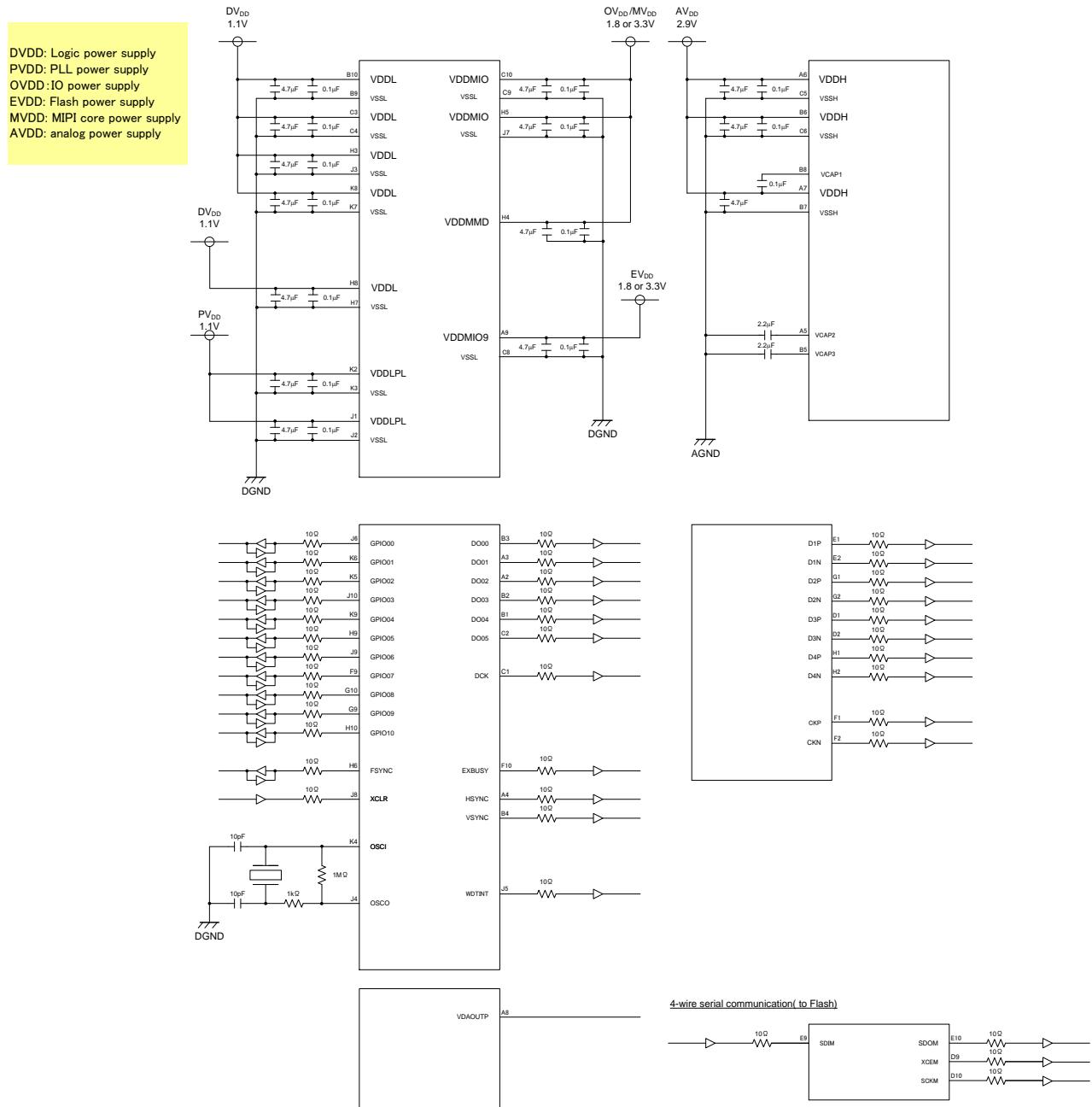


Fig. 13-1. Application Circuit (Parallel Output)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

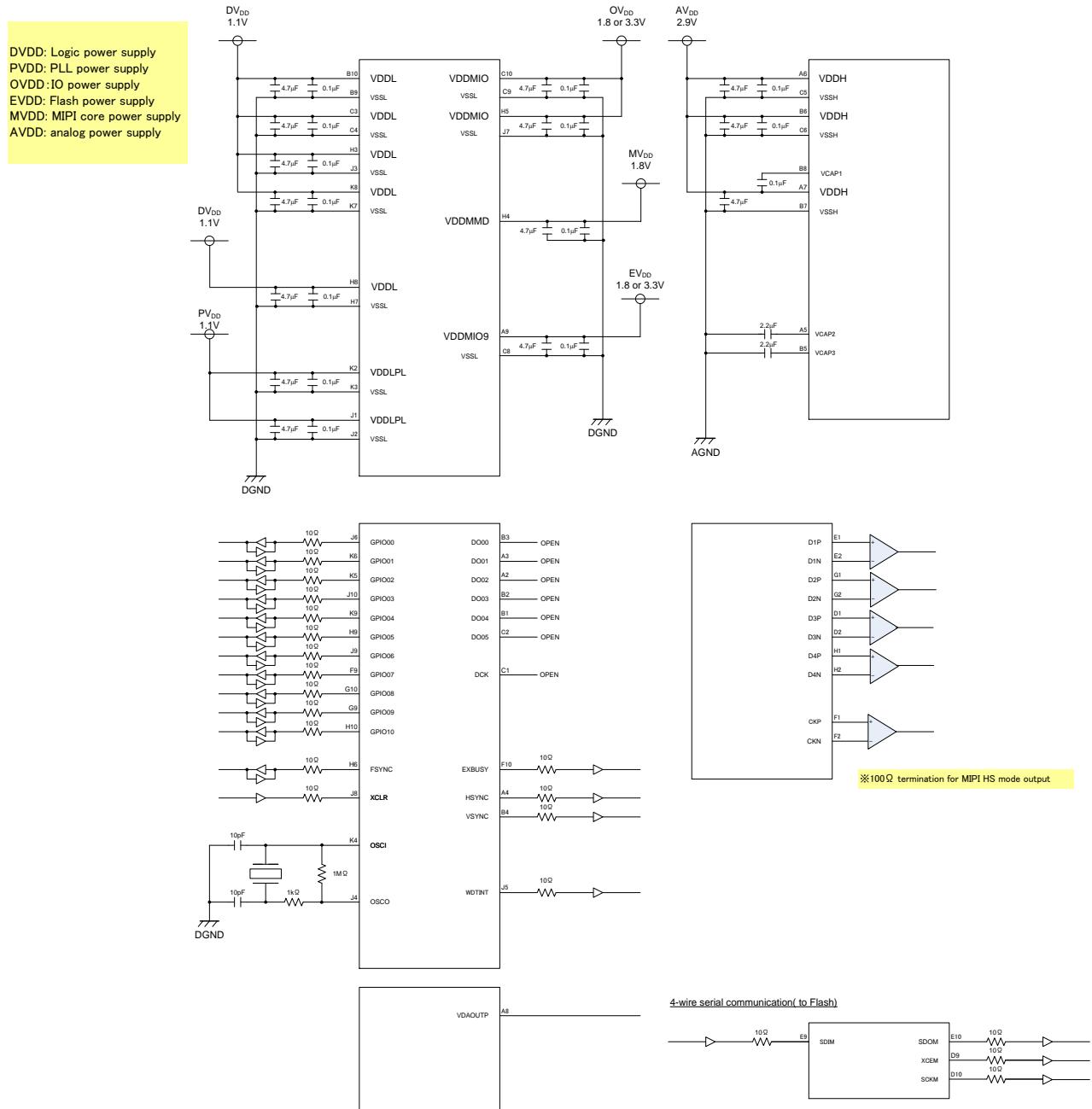


Fig. 13-2. Application Circuit (MIPI Output)

Application circuits shown are typical examples illustrating the operation of the devices.  
 Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## 14. Spot Pixel Specification

### 14-1. Spot Pixel Specification

Table 14-1. Spot Pixel Specification ( $T_j = 60^{\circ}\text{C}$ )



### 14-2. Measurement Method for Spot Pixels

With Standard image condition II, device driver shall be set within bias condition and clock voltage condition. Configure the drive circuit according to the example and measure.

#### 1. Black or white pixels at high light

After adjusting the luminous intensity so that the average value  $VG$  of the G signal outputs is T.B.D. mV, measure the local dip point (black pixel at high light,  $V_{iB}$ ) and peak point (white pixel at high light,  $V_{iK}$ ) in the  $W_g$  /  $W_{rb}$  /  $G$  /  $R$  /  $B$  signal output  $V_i$  ( $i = W_g$  /  $W_{rb}$  /  $G$  /  $R$  /  $B$ ), and substitute the value into the following formula.

$$\text{Spot pixel level } D = ((V_{iB} \text{ or } V_{iK}) / \text{Average value of } V_i) \times 100 [\%]$$

#### 2. White pixels in dark

Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

#### 3. Black pixels at signal saturated

Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

## 15. Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.") Cosmic radiation is one of the causes of White Pixels. Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as establishment of quality assurance standards on white pixels in the dark. White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensors devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space. Note that all White Pixels cannot be compensated although automatic compensation systems for White Pixels In dark signals are already adopted in the PRODUCTS.

### [For Your Reference] The Annual number of White Pixels Occurrence Caused by Cosmic Radiation

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by cosmic radiation in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

#### Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of White Pixel occurrence when compensation systems not in operation	Annual number of White Pixel occurrence when compensation systems in operation
5.6 mV or higher	T.B.D. pcs	Approx. 1/ T.B.D. of annual number of White Pixel occurrence when compensation systems not in operation
10.0 mV or higher	T.B.D. pcs	
24.0 mV or higher	T.B.D. pcs	
50.0 mV or higher	T.B.D. pcs	
72.0 mV or higher	T.B.D. pcs	

- Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.
- Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have been conducted over a specific time period and in a specific environment.
- Note 3) The Annual number of White Pixel occurrence when compensation systems in operation shown above is theoretical value placing the device in the light-obstructed state. This data does not guarantee the upper limits of the Annual number of White Pixels occurrence.
- Note 4) As this data does not take occurrence of White Pixels caused by alpha radiation into account, White Pixels are likely to occur at higher value than the rate set forth in such data.

#### For Your Reference:

The annual number of White Pixels occurrence caused by cosmic radiation at an altitude of 3,000 meters will be from 5 to 10 times higher than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence caused by cosmic radiation in such areas approximately doubles when compared with that in Tokyo.

Material\_No.08-0.0.1

## 16. CRA Characteristics

The recommended CRA characteristics is 0.0 degrees all over the image height (0 - 100%), because the target E.P.D. is infinite.

\*We assume that the worst case of E.P.D. is -30mm. The CRA characteristics of -30mm E.P.D. is described below.  
The real CRA should be smaller than the table below.

(Exit Pupil Distance: -30 mm)

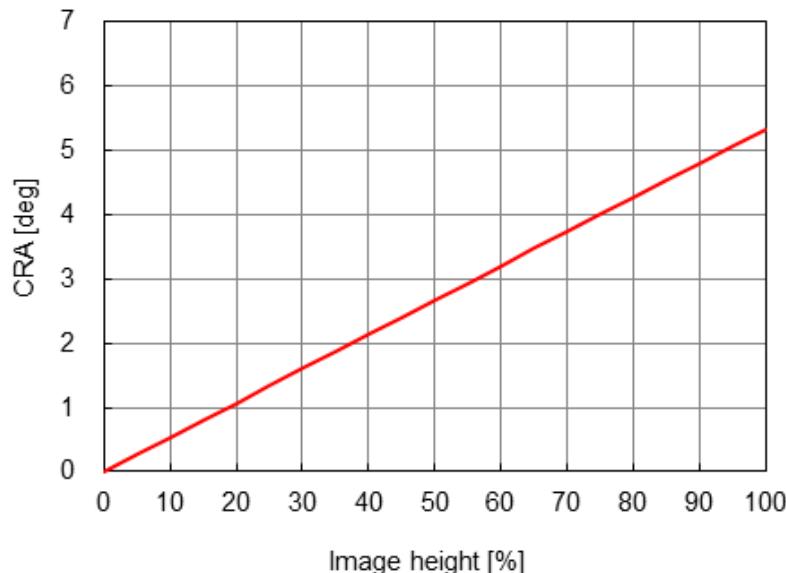


Fig. 16-1. CRA Characteristics

Table 16-1. CRA Characteristics

Image Height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
10	0.28	0.53
20	0.56	1.07
30	0.84	1.60
40	1.12	2.14
50	1.40	2.67
60	1.68	3.21
70	1.96	3.74
80	2.24	4.27
90	2.52	4.80
100	2.80	5.33

## 17. Package Outline (TENTATIVE)

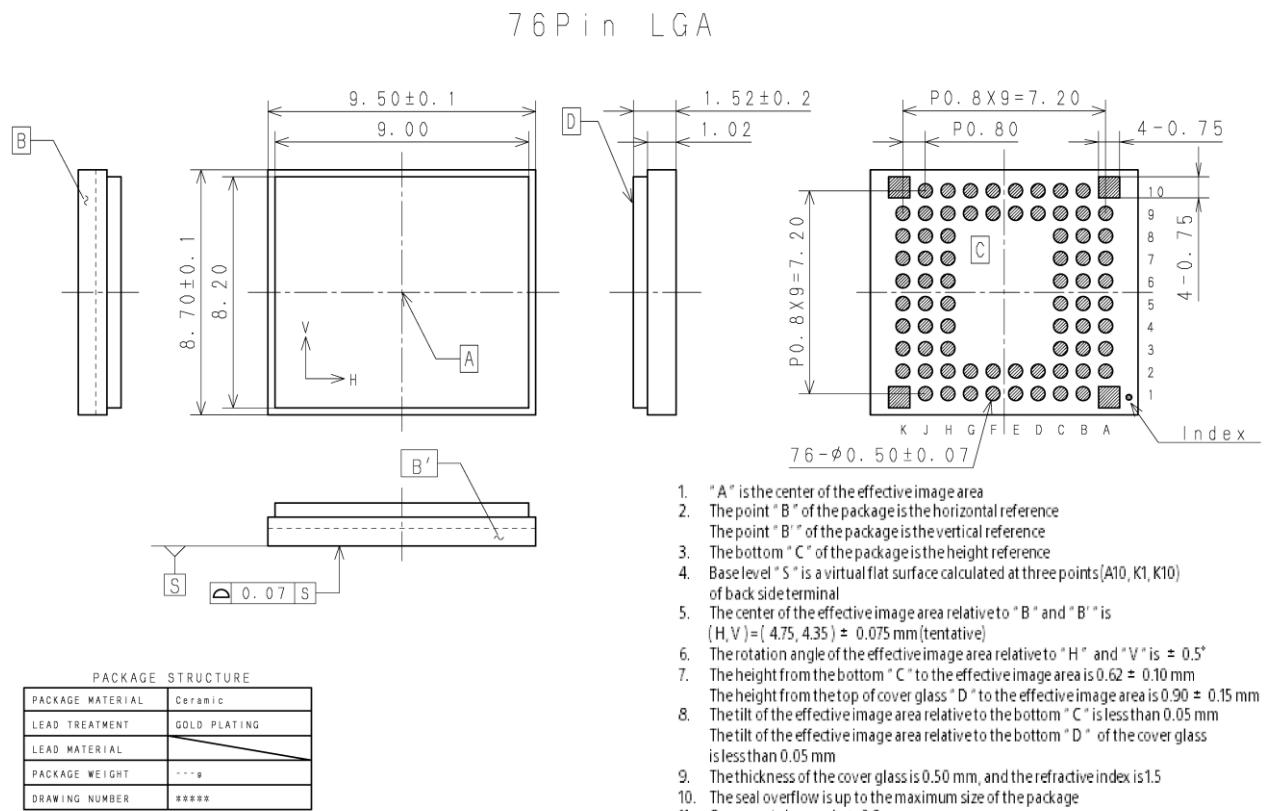


Fig. 17-1. Package Outline

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## 18. Notes On Handling

### 1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- (1) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- (2) Use a wrist strap when handling directly.
- (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
- (4) Ionized air is recommended for discharge when handling image sensors.
- (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

### 2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

- (1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
- (2) Do not touch the glass surface with hand and make any object contact with it.  
If dust or other is stuck to a glass surface, blow it off with an air blower.  
(For dust stuck through static electricity, ionized air is recommended.)
- (3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
- (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

### 3. Installing (attaching)

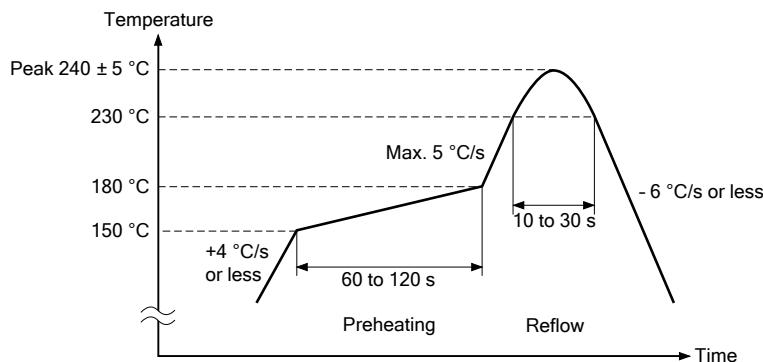
- (1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
- (2) The adhesive may cause the marking on the rear surface to disappear.
- (3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
- (4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
- (5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

#### 4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

##### (1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



##### (2) Reflow conditions

- (a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
- (b) Perform the reflow soldering only one time.
- (c) Finish reflow soldering within 72 h after unsealing the degassed packing.  
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
- (d) Perform re-baking only one time under the condition at 125 °C for 24 h.

##### (3) Others

- (a) Carry out evaluation for the solder joint reliability in your company.
- (b) After the reflow, the paste residue of protective tape may remain around the seal glass.  
(The paste residue of protective tape should be ignored except remarkable one.)
- (c) Note that X-ray inspection may damage characteristics of the sensor.

#### 5. Others

- (1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
- (2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
- (3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
- (4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
- (5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

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**List of Trademark Logos and Definition Statements**

\* Exmor RS is a trademark of Sony Corporation. The Exmor RS is a Sony's CMOS image sensor with high-resolution, high-performance and compact size by replacing a supporting substrate in Exmor R™ which changed fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type, with layered chips formed signal processing circuits.



\* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per  $1 \mu\text{m}^2$  (color product, when imaging with a 706 cd/m<sup>2</sup> light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

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**Revision History**

Date	Revision	Page	Description
26 Jan. 2014	0.1	-	First edition
13 Feb. 2015	0.2	11, 12 62, 64, 65 75, 76 81	Correct pin names. Update the power ON/OFF sequence. Update the Application circuit. Add the comment to "5. Others."