This chapter provides a general description of the High-End Timer (N2HET). The N2HET is a software-controlled timer with a dedicated specialized timer micromachine and a set of 30 instructions. The N2HET micromachine is connected to a port of up to 32 input/output (I/O) pins.

1.1 N2HET Registers

summarizes all the N2HET registers. The base address for the control registers is FFF7 B800h for N2HET1 and FFF7 B900h for N2HET2.

1-1. N2HET Registers

Offset	Acronym	Register Name	Section
00	HETGCR	Global Configuration Register	
04h	HETPFR	Prescale Factor Register	
08h	HETADDR	NHET Current Address Register	
0Ch	HETOFF0	Offset Index Priority Level 0 Register	
10h	HETOFF1	Offset Index Priority Level 1 Register	
14h	HETINTENAS	Interrupt Enable Set Register	
18h	HETINTENAC	Interrupt Enable Clear Register	
1Ch	HETEXC1	Exception Control Register 1	
20h	HETEXC2	Exception Control Register 2	
24h	HETPRY	Interrupt Priority Register	
28h	HETFLG	Interrupt Flag Register	
2Ch	HETAND	AND Share Control Register	
34h	HETHRSH	HR Share Control Register	
38h	HETXOR	HR XOR-Share Control Register	
3Ch	HETREQENS	Request Enable Set Register	
40h	HETREQENC	Request Enable Clear Register	
44h	HETREQDS	Request Destination Select Register	
4Ch	HETDIR	NHET Direction Register	
50h	HETDIN	NHET Data Input Register	
54h	HETDOUT	NHET Data Output Register	
58h	HETDSET	NHET Data Set Register	
5Ch	HETDCLR	NHET Data Clear Register	
60h	HETPDR	NHET Open Drain Register	
64h	HETPULDIS	NHET Pull Disable Register	
68h	HETPSL	NHET Pull Select Register	
74h	HETPCR	Parity Control Register	
78h	HETPAR	Parity Address Register	
7Ch	HETPPR	Parity Pin Register	
80h	HETSFPRLD	Suppression Filter Preload Register	
84h	HETSFENA	Suppression Filter Enable Register	
8Ch	HETLBPSEL	Loop Back Pair Select Register	
90h	HETLBPDIR	Loop Back Pair Direction Register	
94h	HETPINDIS	NHET Pin Disable Register	
9Ch	HWAPINSEL	HWAG Pin Select Register	
A0h	HWAGCR0	HWAG Global Control Register 0	
A8h	HWAGCR1	HWAG Global Control Register 1	
ACh	HWAINTENAS	HWAG Interrupt Enable Set Register	
B0h	HWAINTENAC	HWAG Interrupt Enable Clear Register	
B4h	HWAPRYS	HWAG Interrupt Priority Set Register	
B8h	HWAPRYC	HWAG Interrupt Priority Set Register	
BCh	HWAFLG	HWAG Interrupt Flag Register	
C0h	HWAOFF0	HWAG Offset Index Priority Level 0 Register	
C4h	HWAOFF1	HWAG Offset Index Priority Level 1 Register	

1-1. N2HET Registers (continued)

Offset	Acronym	Register Name	Section
C8h	HWAACNT	HWAG Angle Count Register	
CCh	HWAPCNT0	HWAG Period Count Register 0	
D0h	HWAPCNT1	HWAG Period Count Register 1	
D4h	HWASTWD	HWAG Step Width Register	
D8h	HWATHNUM	HWAG Tooth Number Register	
DCh	HWATHCNT	HWAG Tooth Count Register	
E0h	HWAFIL0	HWAG Filter Register 0	
E8h	HWAFIL1	HWAG Filter Register 1	
F0h	HWAANGI	HWAG Angle Increment Register	

1.1.1 HETGCR Register

N2HET1: offset = FFF7 B800h; **N2HET2:** offset = FFF7 B900h

1-1. Global Configuration Register (HETGCR)

31	25	24	23	22	21	20	19	18	17	16
Reserved		HET PIN ENA	Rsvd.	MP		Reserved		PPF	IS	CMS
R-0		R/W-1	R-0	R/W-0		R-0		R/W-0	R/W-0	R/W-0

15	1	0
Reserved		TO
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-2. HETGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
25-31	Reserved	R	0	Read returns 0. Writes have no effect.
24	HETPINENA	R/W	1	Enables the output buffers of the pin structures depending on the value of nDIS and DIR.x when PINDIS.x is set. This bit is automatically cleared whenever the nDIS pin (input port) value is 0. 0 = GLOBAL_TRIP_DIS : Output buffer structures are not affected by the nDIS input. 1 = GLOBAL_TRIP_ENA : If the nDIS input is zero, and the bit PINDIS.x is set, then the output buffer of pin NHET[x] will be disabled.
23	Reserved	R	0	Read returns 0. Writes have no effect.
21-22	MP	R/W	0	Master Priority: Determines priority of HTU versus CPU/DMA to N2HET RAM 0 = PRI_HTU_LOW : Arbitration to N2HET RAM is fixed with HTU as lowest priority. 1 = PRI_HTU_HI : Arbitration to N2HET RAM is fixed with HTU as highest priority. 2 = PRI_RR : Arbitration to N2HET RAM follows a round-robin scheme. 3 = Reserved.
19-20	Reserved	R	0	Read returns 0. Writes have no effect.
18	PPF	R/W	0	Protect Program Fields: Determines whether the CPU(s), HTU, and DMA can make changes to the program field of the N2HET instruction RAM while the N2HET is executing (TO=1). Note that this bit protects only to the program field of the N2HET instruction RAM, not the Control and Data Fields. 0 = PPF_OFF : Protect Program Fields feature is off. 1 = PPF_ON : Protect Program Fields feature is on. While the N2HET is executing, access to the program field by the CPU(s), HTU, and DMA is read only.
17	IS	R/W	0	Ignore Suspend: When Ignore Suspend = 0, the timer operation is stopped on suspend (the current timer instruction is completed). Timer RAM can be freely accessed during suspend. When set to 1, the suspend is ignored and the N2HET continues operating. 0 = IS_OFF : N2HET stops executing while the CPU is in suspended. 1 = IS_ON : N2HET ignores the CPU suspend state.

1-2. HETGCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMS	R/W	0	Clock Master / Slave: This bit is used to synchronize multi-N2HETs. If set (N2HET is master), the N2HET outputs a signal to synchronize the prescalers of the slave N2HET. By default, this bit is reset, which means a slave configuration. For independent N2HET operation this bit should be set to 1. 0 = CMS_SLAVE : N2HET is configured as a clock slave and synchronizes to another N2HET. 1 = CMS_MASTER: N2HET is configured as a clock master.
1-15	Reserved	R	0	Read returns 0. Writes have no effect.
0	TO	R/W	0	Turn On/Off: When TO = 0, the timer program stops executing. Turn-off is automatically delayed until the current timer program loop is completed. Turn-off does not affect the content of the timer RAM, ALU registers, or control registers. Turn-off resets all flags. 0 = TO_OFF: N2HET stops executing at the next loop resolution clock. 1 = TO_ON : is configured as a clock master.

1.1.2 HETPFR Register

N2HET1: offset = FFF7 B804h; **N2HET2:** offset = FFF7 B904h

1-2. Prescale Factor Register (HETPFR)

31	17	16
Reserved		
R-0		

15	11	10	8	7	6	5	0
Reserved		LRPFC		Reserved		HRPFC	
R-0		R/WP-0		R-0		R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

1-3. HETPFR Register Field Descriptions

Bit	Field	Type	Reset	Description
11-31	Reserved	R	0	Read returns 0. Writes have no effect.
8-10	LRPFC	R/W	0	Loop Resolution Pre-scale Factor Code - Writable only from Privilege Mode 0 = LRPFC_DIV1 : Prescale factor lr is /1. 1 = LRPFC_DIV2 : Prescale factor lr is /2. 2 = LRPFC_DIV4 : Prescale factor lr is /4. 3 = LRPFC_DIV8: Prescale factor lr is /8. 4 = LRPFC_DIV16 : Prescale factor lr is /16. 5 = LRPFC_DIV32 : Prescale factor lr is /32. 6 = LRPFC_DIV64 : Prescale factor lr is /64. 7 = LRPFC_DIV128 : Prescale factor lr is /128.
6-7	Reserved	R	0	Read returns 0. Writes have no effect.

1-3. HETPFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-5	HRPFC	R/W	0	High Resolution Pre-scale Factor Code - Writable only from Privilege Mode 0 = HRPFC_DIV1 : Prescale factor hr is /1. 1 = HRPFC_DIV2 : Prescale factor hr is /2. 2 = HRPFC_DIV3 : Prescale factor hr is /3. 3 = HRPFC_DIV4 : Prescale factor hr is /4. 4 = HRPFC_DIV5 : Prescale factor hr is /5. 5 = HRPFC_DIV6 : Prescale factor hr is /6. 6 = HRPFC_DIV7 : Prescale factor hr is /7. 7 = HRPFC_DIV8 : Prescale factor hr is /8. 8 = HRPFC_DIV9 : Prescale factor hr is /9. 9 = HRPFC_DIV10 : Prescale factor hr is /10. 10 = HRPFC_DIV11 : Prescale factor hr is /11. 11 = HRPFC_DIV12 : Prescale factor hr is /12. 12 = HRPFC_DIV13 : Prescale factor hr is /13. 13 = HRPFC_DIV14 : Prescale factor hr is /14. 14 = HRPFC_DIV15 : Prescale factor hr is /15. 15 = HRPFC_DIV16 : Prescale factor hr is /16. 16 = HRPFC_DIV17 : Prescale factor hr is /17. 17 = HRPFC_DIV18 : Prescale factor hr is /18. 18 = HRPFC_DIV19 : Prescale factor hr is /19. 19 = HRPFC_DIV20 : Prescale factor hr is /20. 20 = HRPFC_DIV21 : Prescale factor hr is /21. 21 = HRPFC_DIV22 : Prescale factor hr is /22. 22 = HRPFC_DIV23 : Prescale factor hr is /23. 23 = HRPFC_DIV24 : Prescale factor hr is /24. 24 = HRPFC_DIV25 : Prescale factor hr is /25. 25 = HRPFC_DIV26 : Prescale factor hr is /26. 26 = HRPFC_DIV27 : Prescale factor hr is /27. 27 = HRPFC_DIV28 : Prescale factor hr is /28. 28 = HRPFC_DIV29 : Prescale factor hr is /29. 29 = HRPFC_DIV30 : Prescale factor hr is /30. 30 = HRPFC_DIV31 : Prescale factor hr is /31. 31 = HRPFC_DIV32 : Prescale factor hr is /32. 32 = HRPFC_DIV33 : Prescale factor hr is /33. 33 = HRPFC_DIV34 : Prescale factor hr is /34. 34 = HRPFC_DIV35 : Prescale factor hr is /35. 35 = HRPFC_DIV36 : Prescale factor hr is /36. 36 = HRPFC_DIV37 : Prescale factor hr is /37. 37 = HRPFC_DIV38 : Prescale factor hr is /38. 38 = HRPFC_DIV39 : Prescale factor hr is /39. 39 = HRPFC_DIV40 : Prescale factor hr is /40.

1-3. HETPFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				40 = HRPFC_DIV41 : Prescale factor hr is /41.
				41 = HRPFC_DIV42 : Prescale factor hr is /42.
				42 = HRPFC_DIV43 : Prescale factor hr is /43.
				43 = HRPFC_DIV44 : Prescale factor hr is /44.
				44 = HRPFC_DIV45 : Prescale factor hr is /45.
				45 = HRPFC_DIV46 : Prescale factor hr is /46.
				46 = HRPFC_DIV47 : Prescale factor hr is /47.
				47 = HRPFC_DIV48 : Prescale factor hr is /48.
				48 = HRPFC_DIV49 : Prescale factor hr is /49.
				49 = HRPFC_DIV50 : Prescale factor hr is /50.
				50 = HRPFC_DIV51 : Prescale factor hr is /51.
				51 = HRPFC_DIV52 : Prescale factor hr is /52.
				52 = HRPFC_DIV53 : Prescale factor hr is /53.
				53 = HRPFC_DIV54 : Prescale factor hr is /54.
				54 = HRPFC_DIV55 : Prescale factor hr is /55.
				55 = HRPFC_DIV56 : Prescale factor hr is /56.
				56 = HRPFC_DIV57 : Prescale factor hr is /57.
				57 = HRPFC_DIV58 : Prescale factor hr is /58.
				58 = HRPFC_DIV59 : Prescale factor hr is /59.
				59 = HRPFC_DIV60 : Prescale factor hr is /60.
				60 = HRPFC_DIV61 : Prescale factor hr is /61.
				61 = HRPFC_DIV62 : Prescale factor hr is /62.
				62 = HRPFC_DIV63 : Prescale factor hr is /63.
				63 = HRPFC_DIV64 : Prescale factor hr is /64.

1.1.3 HETADDR Register

N2HET1: offset = FFF7 B808h; **N2HET2:** offset = FFF7 B908h

1-3. N2HET Current Address (HETADDR)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		HETADDR	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-4. HETADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
9-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-8	HETADDR	R	0	N2HET Current Address: Read: Returns the current N2HET program address.

1.1.4 HETOFF0 Register

N2HET1: offset = FFF7 B80Ch; **N2HET2:** offset = FFF7 B90Ch

1-4. Offset Index Priority Level 0 Register (HETOFF0)

31	16
Reserved	
R-0	

15	6	5	0
Reserved		OFFSET1	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-5. HETOFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-31	Reserved	R	0	Read returns 0. Writes have no effect.

1-5. HETOFF0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-5	OFFSET0	R	0	Priority Level 0 Interrupt Offset. Reading from this register returns the highest priority interrupt pending on the priority level 0 and clears the corresponding flag in the HETFLG register, unless the read occurs during emulation mode. Offset values are encoded as follows: 0 = HET_INT_NONE: There are currently no priority level interrupts pending. 1 = HET_INT_32NP0: Instruction 32*N + 0 Interrupt Pending (0, 32, 64...) 2 = HET_INT_32NP1: Instruction 32*N + 1 Interrupt Pending (1, 33, 65...) 3 = HET_INT_32NP2: Instruction 32*N + 2 Interrupt Pending 4 = HET_INT_32NP3: Instruction 32*N + 3 Interrupt Pending 5 = HET_INT_32NP4: Instruction 32*N + 4 Interrupt Pending 6 = HET_INT_32NP5: Instruction 32*N + 5 Interrupt Pending 7 = HET_INT_32NP6: Instruction 32*N + 6 Interrupt Pending 8 = HET_INT_32NP7: Instruction 32*N + 7 Interrupt Pending 9 = HET_INT_32NP8: Instruction 32*N + 8 Interrupt Pending 10 = HET_INT_32NP9: Instruction 32*N + 9 Interrupt Pending 11 = HET_INT_32NP10: Instruction 32*N + 10 Interrupt Pending 12 = HET_INT_32NP11: Instruction 32*N + 11 Interrupt Pending 13 = HET_INT_32NP12: Instruction 32*N + 12 Interrupt Pending 14 = HET_INT_32NP13: Instruction 32*N + 13 Interrupt Pending 15 = HET_INT_32NP14: Instruction 32*N + 14 Interrupt Pending 16 = HET_INT_32NP15: Instruction 32*N + 15 Interrupt Pending 17 = HET_INT_32NP16: Instruction 32*N + 16 Interrupt Pending 18 = HET_INT_32NP17: Instruction 32*N + 17 Interrupt Pending 19 = HET_INT_32NP18: Instruction 32*N + 18 Interrupt Pending 20 = HET_INT_32NP19: Instruction 32*N + 19 Interrupt Pending 21 = HET_INT_32NP20: Instruction 32*N + 20 Interrupt Pending 22 = HET_INT_32NP21: Instruction 32*N + 21 Interrupt Pending 23 = HET_INT_32NP22: Instruction 32*N + 22 Interrupt Pending 24 = HET_INT_32NP23: Instruction 32*N + 23 Interrupt Pending 25 = HET_INT_32NP24: Instruction 32*N + 24 Interrupt Pending 26 = HET_INT_32NP25: Instruction 32*N + 25 Interrupt Pending 27 = HET_INT_32NP26: Instruction 32*N + 26 Interrupt Pending 28 = HET_INT_32NP27: Instruction 32*N + 27 Interrupt Pending 29 = HET_INT_32NP28: Instruction 32*N + 28 Interrupt Pending 30 = HET_INT_32NP29: Instruction 32*N + 29 Interrupt Pending 31 = HET_INT_32NP30: Instruction 32*N + 30 Interrupt Pending 32 = HET_INT_32NP31: Instruction 32*N + 31 Interrupt Pending 33 = HET_INT_PRGM_OVRFL : Program Overflow Interrupt Pending 34 = HET_INT_APCNT_UNRFL : APCNT Underflow Interrupt Pending 35 = HET_INT_APCNT_OVRFL : APCNT Overflow Interrupt Pending

1.1.5 HETOFF1 Register

N2HET1: offset = FFF7 B810h; **N2HET2:** offset = FFF7 B910h

1-5. Offset Index Priority Level 1 Register (HETOFF1)

31	16
Reserved	
R-0	

15	6	5	0
Reserved		OFFSET2	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-6. HETOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-31	Reserved	R	0	Read returns 0. Writes have no effect.

1-6. HETOFF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-5	OFFSET1	R	0	Priority Level 1 Interrupt Offset. Reading from this register returns the highest priority interrupt pending on priority level 1 and clears the corresponding flag in the HETFLG register, unless the read occurs during emulation mode. Offset values are encoded as follows: 0 = HET_INT_NONE: There are currently no priority level 1 Interrupts pending. 1 = HET_INT_32NP0: Instruction 32*N + 0 Interrupt Pending (0, 32, 64...) 2 = HET_INT_32NP1: Instruction 32*N + 1 Interrupt Pending (1, 33, 65...) 3 = HET_INT_32NP2: Instruction 32*N + 2 Interrupt Pending 4 = HET_INT_32NP3: Instruction 32*N + 3 Interrupt Pending 5 = HET_INT_32NP4: Instruction 32*N + 4 Interrupt Pending 6 = HET_INT_32NP5: Instruction 32*N + 5 Interrupt Pending 7 = HET_INT_32NP6: Instruction 32*N + 6 Interrupt Pending 8 = HET_INT_32NP7: Instruction 32*N + 7 Interrupt Pending 9 = HET_INT_32NP8: Instruction 32*N + 8 Interrupt Pending 10 = HET_INT_32NP9: Instruction 32*N + 9 Interrupt Pending 11 = HET_INT_32NP10: Instruction 32*N + 10 Interrupt Pending 12 = HET_INT_32NP11: Instruction 32*N + 11 Interrupt Pending 13 = HET_INT_32NP12: Instruction 32*N + 12 Interrupt Pending 14 = HET_INT_32NP13: Instruction 32*N + 13 Interrupt Pending 15 = HET_INT_32NP14: Instruction 32*N + 14 Interrupt Pending 16 = HET_INT_32NP15: Instruction 32*N + 15 Interrupt Pending 17 = HET_INT_32NP16: Instruction 32*N + 16 Interrupt Pending 18 = HET_INT_32NP17: Instruction 32*N + 17 Interrupt Pending 19 = HET_INT_32NP18: Instruction 32*N + 18 Interrupt Pending 20 = HET_INT_32NP19: Instruction 32*N + 19 Interrupt Pending 21 = HET_INT_32NP20: Instruction 32*N + 20 Interrupt Pending 22 = HET_INT_32NP21: Instruction 32*N + 21 Interrupt Pending 23 = HET_INT_32NP22: Instruction 32*N + 22 Interrupt Pending 24 = HET_INT_32NP23: Instruction 32*N + 23 Interrupt Pending 25 = HET_INT_32NP24: Instruction 32*N + 24 Interrupt Pending 26 = HET_INT_32NP25: Instruction 32*N + 25 Interrupt Pending 27 = HET_INT_32NP26: Instruction 32*N + 26 Interrupt Pending 28 = HET_INT_32NP27: Instruction 32*N + 27 Interrupt Pending 29 = HET_INT_32NP28: Instruction 32*N + 28 Interrupt Pending 30 = HET_INT_32NP29: Instruction 32*N + 29 Interrupt Pending 31 = HET_INT_32NP30: Instruction 32*N + 30 Interrupt Pending 32 = HET_INT_32NP31: Instruction 32*N + 31 Interrupt Pending 33 = HET_INT_PRGM_OVRFL : Program Overflow Interrupt Pending 34 = HET_INT_APCNT_UNRFL : APCNT Underflow Interrupt Pending 35 = HET_INT_APCNT_OVRFL : APCNT Overflow Interrupt Pending

1.1.6 HETINTENAS Register

N2HET1: offset = FFF7 B814h; **N2HET2:** offset = FFF7 B914h

1-6. Interrupt Enable Set Register (HETINTENAS)

31															16
HETINTENAS															
R/W-0															
15															0
HETINTENAS															
R/W-0															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-7. HETINTENAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETINTENAS_31	R/W1S	0	Enables N2HET Interrupt 31 0 = HETINTENAS_31_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_31_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
30	HETINTENAS_30	R/W1S	0	Enables N2HET Interrupt 30 0 = HETINTENAS_30_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_30_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
29	HETINTENAS_29	R/W1S	0	Enables N2HET Interrupt 29 0 = HETINTENAS_29_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_29_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
28	HETINTENAS_28	R/W1S	0	Enables N2HET Interrupt 28 0 = HETINTENAS_28_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_28_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
27	HETINTENAS_27	R/W1S	0	Enables N2HET Interrupt 27 0 = HETINTENAS_27_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_27_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
26	HETINTENAS_26	R/W1S	0	Enables N2HET Interrupt 26 0 = HETINTENAS_26_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_26_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
25	HETINTENAS_25	R/W1S	0	Enables N2HET Interrupt 25 0 = HETINTENAS_25_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_25_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
24	HETINTENAS_24	R/W1S	0	Enables N2HET Interrupt 24 0 = HETINTENAS_24_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_24_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
23	HETINTENAS_23	R/W1S	0	Enables N2HET Interrupt 23 0 = HETINTENAS_23_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_23_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt

1-7. HETINTENAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETINTENAS_22	R/W1S	0	Enables N2HET Interrupt 22 0 = HETINTENAS_22_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_22_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
21	HETINTENAS_21	R/W1S	0	Enables N2HET Interrupt 21 0 = HETINTENAS_21_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_21_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
20	HETINTENAS_20	R/W1S	0	Enables N2HET Interrupt 20 0 = HETINTENAS_20_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_20_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
19	HETINTENAS_19	R/W1S	0	Enables N2HET Interrupt 19 0 = HETINTENAS_19_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_19_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
18	HETINTENAS_18	R/W1S	0	Enables N2HET Interrupt 18 0 = HETINTENAS_18_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_18_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
17	HETINTENAS_17	R/W1S	0	Enables N2HET Interrupt 17 0 = HETINTENAS_17_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_17_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
16	HETINTENAS_16	R/W1S	0	Enables N2HET Interrupt 16 0 = HETINTENAS_16_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_16_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
15	HETINTENAS_15	R/W1S	0	Enables N2HET Interrupt 15 0 = HETINTENAS_15_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_15_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
14	HETINTENAS_14	R/W1S	0	Enables N2HET Interrupt 14 0 = HETINTENAS_14_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_14_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
13	HETINTENAS_13	R/W1S	0	Enables N2HET Interrupt 13 0 = HETINTENAS_13_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_13_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
12	HETINTENAS_12	R/W1S	0	Enables N2HET Interrupt 12 0 = HETINTENAS_12_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_12_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
11	HETINTENAS_11	R/W1S	0	Enables N2HET Interrupt 11 0 = HETINTENAS_11_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_11_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt

1-7. HETINTENAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETINTENAS_10	R/W1S	0	Enables N2HET Interrupt 10 0 = HETINTENAS_10_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_10_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
9	HETINTENAS_9	R/W1S	0	Enables N2HET Interrupt 9 0 = HETINTENAS_9_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_9_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
8	HETINTENAS_8	R/W1S	0	Enables N2HET Interrupt 8 0 = HETINTENAS_8_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_8_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
7	HETINTENAS_7	R/W1S	0	Enables N2HET Interrupt 7 0 = HETINTENAS_7_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_7_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
6	HETINTENAS_6	R/W1S	0	Enables N2HET Interrupt 6 0 = HETINTENAS_6_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_6_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
5	HETINTENAS_5	R/W1S	0	Enables N2HET Interrupt 5 0 = HETINTENAS_5_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_5_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
4	HETINTENAS_4	R/W1S	0	Enables N2HET Interrupt 4 0 = HETINTENAS_4_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_4_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
3	HETINTENAS_3	R/W1S	0	Enables N2HET Interrupt 3 0 = HETINTENAS_3_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_3_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
2	HETINTENAS_2	R/W1S	0	Enables N2HET Interrupt 2 0 = HETINTENAS_2_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_2_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
1	HETINTENAS_1	R/W1S	0	Enables N2HET Interrupt 1 0 = HETINTENAS_1_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_1_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt
0	HETINTENAS_0	R/W1S	0	Enables N2HET Interrupt 0 0 = HETINTENAS_0_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAS_0_ENA : Read: Interrupt Is Enabled, Write: Enables Interrupt

1.1.7 HETINTENAC Register

N2HET1: offset = FFF7 B818h; **N2HET2:** offset = FFF7 B918h

1-7. Interrupt Enable Clear (HETINTENAC)

31															16
HETINTENAC															
R/W-0															
15															0
HETINTENAC															
R/W-0															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-8. HETINTENAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETINTENAC_31	R/W1C	0	Disables N2HET Interrupt 31 0 = HETINTENAC_31_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_31_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
30	HETINTENAC_30	R/W1C	0	Disables N2HET Interrupt 30 0 = HETINTENAC_30_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_30_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
29	HETINTENAC_29	R/W1C	0	Disables N2HET Interrupt 29 0 = HETINTENAC_29_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_29_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
28	HETINTENAC_28	R/W1C	0	Disables N2HET Interrupt 28 0 = HETINTENAC_28_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_28_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
27	HETINTENAC_27	R/W1C	0	Disables N2HET Interrupt 27 0 = HETINTENAC_27_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_27_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
26	HETINTENAC_26	R/W1C	0	Disables N2HET Interrupt 26 0 = HETINTENAC_26_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_26_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
25	HETINTENAC_25	R/W1C	0	Disables N2HET Interrupt 25 0 = HETINTENAC_25_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_25_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
24	HETINTENAC_24	R/W1C	0	Disables N2HET Interrupt 24 0 = HETINTENAC_24_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_24_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
23	HETINTENAC_23	R/W1C	0	Disables N2HET Interrupt 23 0 = HETINTENAC_23_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_23_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
22	HETINTENAC_22	R/W1C	0	Disables N2HET Interrupt 22 0 = HETINTENAC_22_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_22_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt

1-8. HETINTENAC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	HETINTENAC_21	R/W1C	0	Disables N2HET Interrupt 21 0 = HETINTENAC_21_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_21_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
20	HETINTENAC_20	R/W1C	0	Disables N2HET Interrupt 20 0 = HETINTENAC_20_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_20_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
19	HETINTENAC_19	R/W1C	0	Disables N2HET Interrupt 19 0 = HETINTENAC_19_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_19_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
18	HETINTENAC_18	R/W1C	0	Disables N2HET Interrupt 18 0 = HETINTENAC_18_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_18_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
17	HETINTENAC_17	R/W1C	0	Disables N2HET Interrupt 17 0 = HETINTENAC_17_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_17_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
16	HETINTENAC_16	R/W1C	0	Disables N2HET Interrupt 16 0 = HETINTENAC_16_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_16_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
15	HETINTENAC_15	R/W1C	0	Disables N2HET Interrupt 15 0 = HETINTENAC_15_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_15_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
14	HETINTENAC_14	R/W1C	0	Disables N2HET Interrupt 14 0 = HETINTENAC_14_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_14_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
13	HETINTENAC_13	R/W1C	0	Disables N2HET Interrupt 13 0 = HETINTENAC_13_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_13_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
12	HETINTENAC_12	R/W1C	0	Disables N2HET Interrupt 12 0 = HETINTENAC_12_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_12_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
11	HETINTENAC_11	R/W1C	0	Disables N2HET Interrupt 11 0 = HETINTENAC_11_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_11_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
10	HETINTENAC_10	R/W1C	0	Disables N2HET Interrupt 10 0 = HETINTENAC_10_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_10_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt

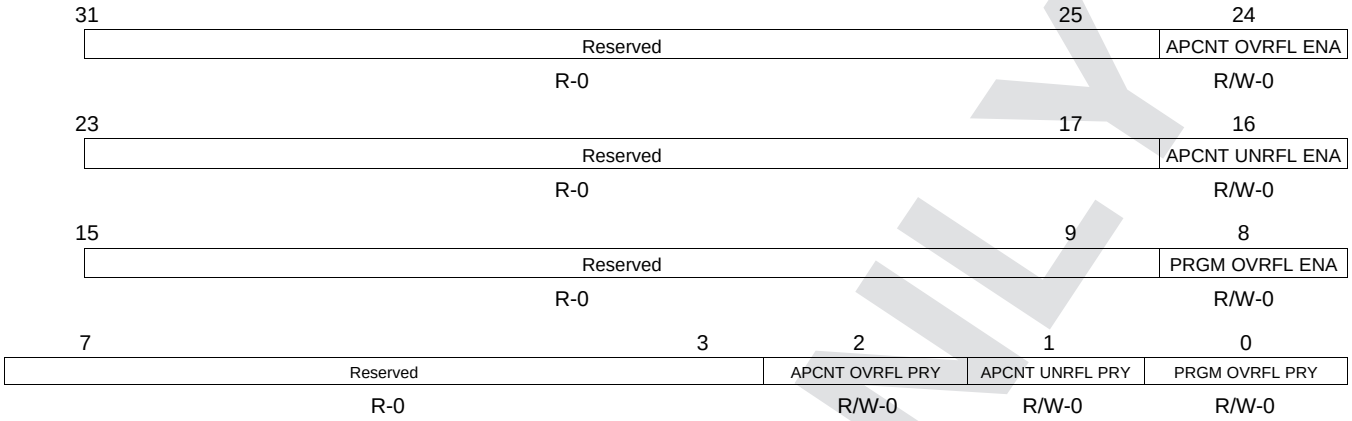
1-8. HETINTENAC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	HETINTENAC_9	R/W1C	0	Disables N2HET Interrupt 9 0 = HETINTENAC_9_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_9_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
8	HETINTENAC_8	R/W1C	0	Disables N2HET Interrupt 8 0 = HETINTENAC_8_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_8_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
7	HETINTENAC_7	R/W1C	0	Disables N2HET Interrupt 7 0 = HETINTENAC_7_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_7_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
6	HETINTENAC_6	R/W1C	0	Disables N2HET Interrupt 6 0 = HETINTENAC_6_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_6_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
5	HETINTENAC_5	R/W1C	0	Disables N2HET Interrupt 5 0 = HETINTENAC_5_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_5_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
4	HETINTENAC_4	R/W1C	0	Disables N2HET Interrupt 4 0 = HETINTENAC_4_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_4_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
3	HETINTENAC_3	R/W1C	0	Disables N2HET Interrupt 3 0 = HETINTENAC_3_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_3_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
2	HETINTENAC_2	R/W1C	0	Disables N2HET Interrupt 2 0 = HETINTENAC_2_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_2_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
1	HETINTENAC_1	R/W1C	0	Disables N2HET Interrupt 1 0 = HETINTENAC_1_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_1_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt
0	HETINTENAC_0	R/W1C	0	Disables N2HET Interrupt 0 0 = HETINTENAC_0_DIS : Read: Interrupt is Disabled, Write: No Effect 1 = HETINTENAC_0_ENA : Read: Interrupt Is Enabled, Write: Disables Interrupt

1.1.8 HETEXC1 Register

N2HET1: offset = FFF7 B81Ch; **N2HET2:** offset = FFF7 B91Ch

1-8. Exception Control Register (HETEXC1)



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-9. HETEXC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
25-31	Reserved	R	0	Read returns 0. Writes have no effect.
24	APCNT_OVRFL_ENA	R/W	0	APCNT Overflow Exception Interrupt Enable 0 = APCNT_OVRFL_INT_DIS : Interrupt is Disabled 1 = APCNT_OVRFL_INT_ENA : Interrupt is Enabled
17-23	Reserved	R	0	Read returns 0. Writes have no effect.
16	APCNT_UNRFL_ENA	R/W	0	APCNT Underflow Exception Interrupt Enable 0 = APCNT_UNRFL_INT_DIS : Interrupt is Disabled 1 = APCNT_UNRFL_INT_ENA : Interrupt is Enabled
9-15	Reserved	R	0	Read returns 0. Writes have no effect.
8	PRGM_OVRFL_ENA	R/W	0	Program Overflow Exception Interrupt Enable 0 = PRGM_OVRFL_INT_DIS : Interrupt is Disabled 1 = PRGM_OVRFL_INT_ENA : Interrupt is Enabled
3-7	Reserved	R	0	Read returns 0. Writes have no effect.
2	APCNT_OVRFL_PRY	R/W	0	APCNT Overflow Exception Interrupt Priority 0 = APCNT_OVRFL_INT_PRY_1 : Interrupt Routed to Priority Level 1 (Low) 1 = APCNT_OVRFL_INT_PRY_0 : Interrupt Routed to Priority Level 0 (High)
1	APCNT_UNRFL_PRY	R/W	0	APCNT Underflow Exception Interrupt Priority 0 = APCNT_UNRFL_INT_PRY_1 : Interrupt Routed to Priority Level 1 (Low) 1 = APCNT_UNRFL_INT_PRY_0 : Interrupt Routed to Priority Level 0 (High)

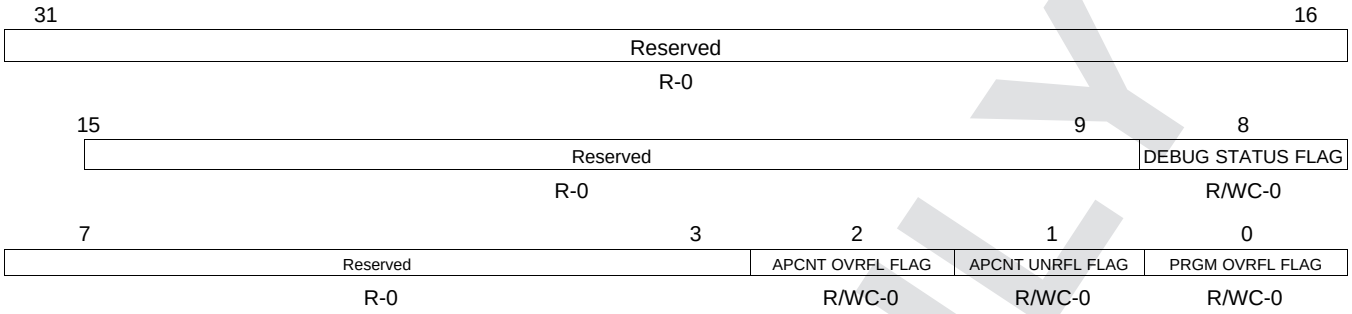
1-9. HETEXC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PRGM_OVRFL_PRY	R/W	0	ProgramOverflow Exception Interrupt Priority 0 = PRGM_OVRFL_INT_PRY_1 : Interrupt Routed to Priority Level 1 (Low) 1 = PRGM_OVRFL_INT_PRY_0 : Interrupt Routed to Priority Level 0 (High)

1.1.9 HETEXC2 Register

N2HET1: offset = FFF7 B820h; **N2HET2:** offset = FFF7 B920h

1-9. Exception Control Register 2 (HETEXC2)



LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

1-10. HETEXC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
9-31	Reserved	R	0	Read returns 0. Writes have no effect.
8	DEBUG_STATUS_FLAG	R/WC	0	Debug Status Flag: This flag is set when the N2HET has stopped at a breakpoint. If this flag is cleared, it means that either the N2HET is running, has not been started, or it has stopped at a breakpoint but the flag was cleared and the N2HET has not yet been restarted. Write one to clear. 0 = HET_RUN : HET is not stopped at a breakpoint. 1 = HET_BRK : HET is stopped at a breakpoint
3-7	Reserved	R	0	Read returns 0. Writes have no effect.
2	APCNT_OVRFL_FLAG	R/WC	0	APCNT Overflow Flag: 0 = APCNT_OVRFL_CLR: APCNT Overflow Exception has not occurred since the flag was cleared. 1 = APCNT_OVRFL_SET : APCNT Overflow Exception has occurred.
1	APCNT_UNDFL_FLAG	R/WC	0	APCNT Underflow Flag: 0 = APCNT_UNDFL_CLR: APCNT Underflow Exception has not occurred since the flag was cleared. 1 = APCNT_UNDFL_SET : APCNT Underflow Exception has occurred.
0	PRGM_OVERFL_FLAG	R/WC	0	Program Overflow Flag: 0 = PRGM_OVRFL_CLR: APCNT Overflow Exception has not occurred since the flag was cleared. 1 = PRGM_OVRFL_SET : APCNT Overflow Exception has occurred.

1.1.10 HETPRY Register

N2HET1: offset = FFF7 B824h; **N2HET2:** offset = FFF7 B924h

1-10. Interrupt Priority Register (HETPRY)

31	16
HETPRY	
R/WP-0	

15	0
HETPRY	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

1-11. HETPRY Register Field Descriptions

Bit	Field	Type	Reset	Description
0-31	HETPRY	R/W	0	HET Interrupt Priority Level bits - Write in Privilege Mode Only 0 = HET_INT_PRY_1 : Interrupt Routed to Priority Level 1 (Low) 1 = HET_INT_PRY_0 : Interrupt Routed to Priority Level 0 (High)

1.1.11 HETFLG Register

N2HET1: offset = FFF7 B828h; **N2HET2:** offset = FFF7 B928h

1-11. Interrupt Flag Register (HETFLG)

31	16
HETFLAG	
R/WC-0	

15	0
HETFLAG	
R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset; X = Unknown

1-12. HETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
0-31	HETFLAG	R/W1C	0	Interrupt Flag Register Bits - Write one to Clear. Bit x is set when an interrupt condition has occurred on one of the instructions x+0, x+32, x+64.... The flag position x (in the register) is decoded from the five LSBs of the instruction address that generated the interrupt. The hardware will set the flag only if the interrupt enable bit (in the corresponding instruction) is set. The flag will be set even if bit x in the Interrupt Enable Set Register (HETINTENAS) is not enabled. Enabling bit x in HETINTENAS is required if an interrupt should be generated. Clearing the flag can be done by writing a one to the flag. Alternatively reading the corresponding Offset Index Priority Level 0 Register (HETOFF0) or Offset Index Priority Level 1 Register (HETOFF1) will automatically clear the flag. 0 = HET_INT_CLR: No N2HET instruction interrupt for this channel has occurred since the flag was cleared. 1 = HET_INT_SET : An N2HET instruction interrupt for this channel has occurred since the flag was cleared.

1.1.12 HETAND Register

N2HET1: offset = FFF7 B82Ch; **N2HET2:** offset = FFF7 B92Ch

1-12. AND Share Control Register (HETAND)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
ANDSHARE31/30	ANDSHARE29/28	ANDSHARE27/26	ANDSHARE25/24	ANDSHARE23/22	ANDSHARE21/20	ANDSHARE19/18	ANDSHARE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
ANDSHARE15/14	ANDSHARE13/12	ANDSHARE11/10	ANDSHARE9/8	ANDSHARE7/6	ANDSHARE5/4	ANDSHARE3/2	ANDSHARE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-13. HETAND Register Field Descriptions

Bit	Field	Type	Reset	Description
16-31	Reserved	R	0	Read returns 0. Writes have no effect.
15	ANDSHARE_31_30	R/W	0	Controls AND sharing of pins N2HET[31] and N2HET[30]. 0 = ANDSHARE_31_30_DIS : AND sharing disabled. 1 = ANDSHARE_31_30_ENA: AND sharing enabled
14	ANDSHARE_29_28	R/W	0	Controls AND sharing of pins N2HET[29] and N2HET[28]. 0 = ANDSHARE_29_28_DIS : AND sharing disabled. 1 = ANDSHARE_29_28_ENA: AND sharing enabled
13	ANDSHARE_27_26	R/W	0	Controls AND sharing of pins N2HET[27] and N2HET[26]. 0 = ANDSHARE_27_26_DIS : AND sharing disabled. 1 = ANDSHARE_27_26_ENA: AND sharing enabled
12	ANDSHARE_25_24	R/W	0	Controls AND sharing of pins N2HET[25] and N2HET[24]. 0 = ANDSHARE_25_24_DIS : AND sharing disabled. 1 = ANDSHARE_25_24_ENA: AND sharing enabled
11	ANDSHARE_23_22	R/W	0	Controls AND sharing of pins N2HET[24] and N2HET[22]. 0 = ANDSHARE_23_22_DIS : AND sharing disabled. 1 = ANDSHARE_23_22_ENA: AND sharing enabled
10	ANDSHARE_21_20	R/W	0	Controls AND sharing of pins N2HET[21] and N2HET[20]. 0 = ANDSHARE_21_20_DIS : AND sharing disabled. 1 = ANDSHARE_21_20_ENA: AND sharing enabled
9	ANDSHARE_19_18	R/W	0	Controls AND sharing of pins N2HET[19] and N2HET[18]. 0 = ANDSHARE_19_18_DIS : AND sharing disabled. 1 = ANDSHARE_19_18_ENA: AND sharing enabled
8	ANDSHARE_17_16	R/W	0	Controls AND sharing of pins N2HET[17] and N2HET[16]. 0 = ANDSHARE_17_16_DIS : AND sharing disabled. 1 = ANDSHARE_17_16_ENA: AND sharing enabled

1-13. HETAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ANDSHARE_15_14	R/W	0	Controls AND sharing of pins N2HET[15] and N2HET[14]. 0 = ANDSHARE_15_14_DIS : AND sharing disabled. 1 = ANDSHARE_15_14_ENA: AND sharing enabled
6	ANDSHARE_13_12	R/W	0	Controls AND sharing of pins N2HET[13] and N2HET[12]. 0 = ANDSHARE_13_12_DIS : AND sharing disabled. 1 = ANDSHARE_13_12_ENA: AND sharing enabled
5	ANDSHARE_11_10	R/W	0	Controls AND sharing of pins N2HET[11] and N2HET[10]. 0 = ANDSHARE_11_10_DIS : AND sharing disabled. 1 = ANDSHARE_11_10_ENA: AND sharing enabled
4	ANDSHARE_9_8	R/W	0	Controls AND sharing of pins N2HET[9] and N2HET[8]. 0 = ANDSHARE_9_8_DIS : AND sharing disabled. 1 = ANDSHARE_9_8_ENA: AND sharing enabled
3	ANDSHARE_7_6	R/W	0	Controls AND sharing of pins N2HET[7] and N2HET[6]. 0 = ANDSHARE_7_6_DIS : AND sharing disabled. 1 = ANDSHARE_7_6_ENA: AND sharing enabled
2	ANDSHARE_5_4	R/W	0	Controls AND sharing of pins N2HET[5] and N2HET[4]. 0 = ANDSHARE_5_4_DIS : AND sharing disabled. 1 = ANDSHARE_5_4_ENA: AND sharing enabled
1	ANDSHARE_3_2	R/W	0	Controls AND sharing of pins N2HET[3] and N2HET[2]. 0 = ANDSHARE_3_2_DIS : AND sharing disabled. 1 = ANDSHARE_3_2_ENA: AND sharing enabled
0	ANDSHARE_1_0	R/W	0	Controls AND sharing of pins N2HET[1] and N2HET[0]. 0 = ANDSHARE_1_0_DIS : AND sharing disabled. 1 = ANDSHARE_1_0_ENA: AND sharing enabled

1.1.13 HETHRSH Register

N2HET1: offset = FFF7 B834h; **N2HET2:** offset = FFF7 B934h

1-13. HR Share Control Register (HETHRSH)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															
15	14	13	12	11	10	9	8								
HRSHARE31/30	HRSHARE29/28	HRSHARE27/26	HRSHARE25/24	HRSHARE23/22	HRSHARE21/20	HRSHARE19/18	HRSHARE17/16								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0								
7	6	5	4	3	2	1	0								
HRSHARE15/14	HRSHARE13/12	HRSHARE11/10	HRSHARE9/8	HRSHARE7/6	HRSHARE5/4	HRSHARE3/2	HRSHARE1/0								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-14. HETHRSH Register Field Descriptions

Bit	Field	Type	Reset	Description
16-31	Reserved	R	0	Read returns 0. Writes have no effect.
15	HRSHARE_31_30	R/W	0	Controls HR sharing of pins N2HET[31] and N2HET[30]. 0 = HRSHARE_31_30_DIS : HR sharing disabled. 1 = HRSHARE_31_30_ENA: HR sharing enabled
14	HRSHARE_29_28	R/W	0	Controls HR sharing of pins N2HET[29] and N2HET[28]. 0 = HRSHARE_29_28_DIS : HR sharing disabled. 1 = HRSHARE_29_28_ENA: HR sharing enabled
13	HRSHARE_27_26	R/W	0	Controls HR sharing of pins N2HET[27] and N2HET[26]. 0 = HRSHARE_27_26_DIS : HR sharing disabled. 1 = HRSHARE_27_26_ENA: HR sharing enabled
12	HRSHARE_25_24	R/W	0	Controls HR sharing of pins N2HET[25] and N2HET[24]. 0 = HRSHARE_25_24_DIS : HR sharing disabled. 1 = HRSHARE_25_24_ENA: HR sharing enabled
11	HRSHARE_23_22	R/W	0	Controls HR sharing of pins N2HET[24] and N2HET[22]. 0 = HRSHARE_23_22_DIS : HR sharing disabled. 1 = HRSHARE_23_22_ENA: HR sharing enabled
10	HRSHARE_21_20	R/W	0	Controls HR sharing of pins N2HET[21] and N2HET[20]. 0 = HRSHARE_21_20_DIS : HR sharing disabled. 1 = HRSHARE_21_20_ENA: HR sharing enabled
9	HRSHARE_19_18	R/W	0	Controls HR sharing of pins N2HET[19] and N2HET[18]. 0 = HRSHARE_19_18_DIS : HR sharing disabled. 1 = HRSHARE_19_18_ENA: HR sharing enabled
8	HRSHARE_17_16	R/W	0	Controls HR sharing of pins N2HET[17] and N2HET[16]. 0 = HRSHARE_17_16_DIS : HR sharing disabled. 1 = HRSHARE_17_16_ENA: HR sharing enabled

1-14. HETHRSH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	HRSHARE_15_14	R/W	0	Controls HR sharing of pins N2HET[15] and N2HET[14]. 0 = HRSHARE_15_14_DIS : HR sharing disabled. 1 = HRSHARE_15_14_ENA: HR sharing enabled
6	HRSHARE_13_12	R/W	0	Controls HR sharing of pins N2HET[13] and N2HET[12]. 0 = HRSHARE_13_12_DIS : HR sharing disabled. 1 = HRSHARE_13_12_ENA: HR sharing enabled
5	HRSHARE_11_10	R/W	0	Controls HR sharing of pins N2HET[11] and N2HET[10]. 0 = HRSHARE_11_10_DIS : HR sharing disabled. 1 = HRSHARE_11_10_ENA: HR sharing enabled
4	HRSHARE_9_8	R/W	0	Controls HR sharing of pins N2HET[9] and N2HET[8]. 0 = HRSHARE_9_8_DIS : HR sharing disabled. 1 = HRSHARE_9_8_ENA: HR sharing enabled
3	HRSHARE_7_6	R/W	0	Controls HR sharing of pins N2HET[7] and N2HET[6]. 0 = HRSHARE_7_6_DIS : HR sharing disabled. 1 = HRSHARE_7_6_ENA: HR sharing enabled
2	HRSHARE_5_4	R/W	0	Controls HR sharing of pins N2HET[5] and N2HET[4]. 0 = HRSHARE_5_4_DIS : HR sharing disabled. 1 = HRSHARE_5_4_ENA: HR sharing enabled
1	HRSHARE_3_2	R/W	0	Controls HR sharing of pins N2HET[3] and N2HET[2]. 0 = HRSHARE_3_2_DIS : HR sharing disabled. 1 = HRSHARE_3_2_ENA: HR sharing enabled
0	HRSHARE_1_0	R/W	0	Controls HR sharing of pins N2HET[1] and N2HET[0]. 0 = HRSHARE_1_0_DIS : HR sharing disabled. 1 = HRSHARE_1_0_ENA: HR sharing enabled

1.1.14 HETXOR Register

N2HET1: offset = FFF7 B838h; **N2HET2:** offset = FFF7 B938h

1-14. XOR Share Control Register (HETXOR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															
15	14	13	12	11	10	9	8								
XORSHARE31/30	XORSHARE29/28	XORSHARE27/26	XORSHARE25/24	XORSHARE23/22	XORSHARE21/20	XORSHARE19/18	XORSHARE17/16								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0								
7	6	5	4	3	2	1	0								
XORSHARE15/14	XORSHARE13/12	XORSHARE11/10	XORSHARE9/8	XORSHARE7/6	XORSHARE5/4	XORSHARE3/2	XORSHARE1/0								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-15. HETXOR Register Field Descriptions

Bit	Field	Type	Reset	Description
16-31	Reserved	R	0	Read returns 0. Writes have no effect.
15	XORSHARE_31_30	R/W	0	Controls XOR sharing of pins N2HET[31] and N2HET[30]. 0 = XORSHARE_31_30_DIS : XOR sharing disabled. 1 = XORSHARE_31_30_ENA: XOR sharing enabled
14	XORSHARE_29_28	R/W	0	Controls XOR sharing of pins N2HET[29] and N2HET[28]. 0 = XORSHARE_29_28_DIS : XOR sharing disabled. 1 = XORSHARE_29_28_ENA: XOR sharing enabled
13	XORSHARE_27_26	R/W	0	Controls XOR sharing of pins N2HET[27] and N2HET[26]. 0 = XORSHARE_27_26_DIS : XOR sharing disabled. 1 = XORSHARE_27_26_ENA: XOR sharing enabled
12	XORSHARE_25_24	R/W	0	Controls XOR sharing of pins N2HET[25] and N2HET[24]. 0 = XORSHARE_25_24_DIS : XOR sharing disabled. 1 = XORSHARE_25_24_ENA: XOR sharing enabled
11	XORSHARE_23_22	R/W	0	Controls XOR sharing of pins N2HET[24] and N2HET[22]. 0 = XORSHARE_23_22_DIS : XOR sharing disabled. 1 = XORSHARE_23_22_ENA: XOR sharing enabled
10	XORSHARE_21_20	R/W	0	Controls XOR sharing of pins N2HET[21] and N2HET[20]. 0 = XORSHARE_21_20_DIS : XOR sharing disabled. 1 = XORSHARE_21_20_ENA: XOR sharing enabled
9	XORSHARE_19_18	R/W	0	Controls XOR sharing of pins N2HET[19] and N2HET[18]. 0 = XORSHARE_19_18_DIS : XOR sharing disabled. 1 = XORSHARE_19_18_ENA: XOR sharing enabled
8	XORSHARE_17_16	R/W	0	Controls XOR sharing of pins N2HET[17] and N2HET[16]. 0 = XORSHARE_17_16_DIS : XOR sharing disabled. 1 = XORSHARE_17_16_ENA: XOR sharing enabled

1-15. HETXOR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	XORSHARE_15_14	R/W	0	Controls XOR sharing of pins N2HET[15] and N2HET[14]. 0 = XORSHARE_15_14_DIS : XOR sharing disabled. 1 = XORSHARE_15_14_ENA: XOR sharing enabled
6	XORSHARE_13_12	R/W	0	Controls XOR sharing of pins N2HET[13] and N2HET[12]. 0 = XORSHARE_13_12_DIS : XOR sharing disabled. 1 = XORSHARE_13_12_ENA: XOR sharing enabled
5	XORSHARE_11_10	R/W	0	Controls XOR sharing of pins N2HET[11] and N2HET[10]. 0 = XORSHARE_11_10_DIS : XOR sharing disabled. 1 = XORSHARE_11_10_ENA: XOR sharing enabled
4	XORSHARE_9_8	R/W	0	Controls XOR sharing of pins N2HET[9] and N2HET[8]. 0 = XORSHARE_9_8_DIS : XOR sharing disabled. 1 = XORSHARE_9_8_ENA: XOR sharing enabled
3	XORSHARE_7_6	R/W	0	Controls XOR sharing of pins N2HET[7] and N2HET[6]. 0 = XORSHARE_7_6_DIS : XOR sharing disabled. 1 = XORSHARE_7_6_ENA: XOR sharing enabled
2	XORSHARE_5_4	R/W	0	Controls XOR sharing of pins N2HET[5] and N2HET[4]. 0 = XORSHARE_5_4_DIS : XOR sharing disabled. 1 = XORSHARE_5_4_ENA: XOR sharing enabled
1	XORSHARE_3_2	R/W	0	Controls XOR sharing of pins N2HET[3] and N2HET[2]. 0 = XORSHARE_3_2_DIS : XOR sharing disabled. 1 = XORSHARE_3_2_ENA: XOR sharing enabled
0	XORSHARE_1_0	R/W	0	Controls XOR sharing of pins N2HET[1] and N2HET[0]. 0 = XORSHARE_1_0_DIS : XOR sharing disabled. 1 = XORSHARE_1_0_ENA: XOR sharing enabled

1.1.15 HETREQENS Register

Note: The request line can trigger a DMA control packet (DMA channel), an HTU double control packet (DCP) or both simultaneously. The HETREQDS register determines to which module(s) the N2HET request line n is assigned**Note:** A disabled request line does not memorize old requests. So there are no pending requests to service after enabling request line n..

1-15. Request Enable Set Register (HETREQENS)

31							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
REQ ENA 7	REQ ENA 6	REQ ENA 5	REQ ENA 4	REQ ENA 3	REQ ENA 2	REQ ENA 1	REQ ENA 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-16. HETREQENS Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	REQENA_7	R/W1S	0	Enable DMA Request Enable 7 Set 0 = REQENA_7_DIS : Write: No Effect, Read: DMA Request 7 disabled. 1 = REQENA_7_ENA: Write: Enables DMA Request 7, Read: DMA Request 7 is enabled
6	REQENA_6	R/W1S	0	Enable DMA Request Enable 6 Set 0 = REQENA_6_DIS : Write: No Effect, Read: DMA Request 6 disabled. 1 = REQENA_6_ENA: Write: Enables DMA Request 6, Read: DMA Request 6 is enabled
5	REQENA_5	R/W1S	0	Enable DMA Request Enable 5 Set 0 = REQENA_5_DIS : Write: No Effect, Read: DMA Request 5 disabled. 1 = REQENA_5_ENA: Write: Enables DMA Request 5, Read: DMA Request 5 is enabled
4	REQENA_4	R/W1S	0	Enable DMA Request Enable 4 Set 0 = REQENA_4_DIS : Write: No Effect, Read: DMA Request 4 disabled. 1 = REQENA_4_ENA: Write: Enables DMA Request 4, Read: DMA Request 4 is enabled
3	REQENA_3	R/W1S	0	Enable DMA Request Enable 3 Set 0 = REQENA_3_DIS : Write: No Effect, Read: DMA Request 3 disabled. 1 = REQENA_3_ENA: Write: Enables DMA Request 3, Read: DMA Request 3 is enabled
2	REQENA_2	R/W1S	0	Enable DMA Request Enable 2 Set 0 = REQENA_2_DIS : Write: No Effect, Read: DMA Request 2 disabled. 1 = REQENA_2_ENA: Write: Enables DMA Request 2, Read: DMA Request 2 is enabled

1-16. HETREQENS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	REQENA_1	R/W1S	0	Enable DMA Request Enable 1 Set 0 = REQENA_1_DIS : Write: No Effect, Read: DMA Request 1 disabled. 1 = REQENA_1_ENA: Write: Enables DMA Request 1, Read: DMA Request 1 is enabled
0	REQENA_0	R/W1S	0	Enable DMA Request Enable 0 Set 0 = REQENA_0_DIS : Write: No Effect, Read: DMA Request 0 disabled. 1 = REQENA_0_ENA: Write: Enables DMA Request 0, Read: DMA Request 0 is enabled

1.1.16 HETREQENC Register

N2HET1: offset = FFF7 B840h; **N2HET2:** offset = FFF7 B940h

1-16. Request Enable Clear Register (HETREQENC)

31							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
REQ DIS 7	REQ DIS 6	REQ DIS 5	REQ DIS 4	REQ DIS 3	REQ DIS 2	REQ DIS 1	REQ DIS 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-17. HETREQENC Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	REQENA_7	R/W1C	0	Enable DMA Request Enable 7 Clear 0 = REQENA_7_DIS : Write: No Effect, Read: DMA Request 7 disabled. 1 = REQENA_7_ENA: Write: Disables DMA Request 7, Read: DMA Request 7 is enabled
6	REQENA_6	R/W1C	0	Enable DMA Request Enable 6 Clear 0 = REQENA_6_DIS : Write: No Effect, Read: DMA Request 6 disabled. 1 = REQENA_6_ENA: Write: Disables DMA Request 6, Read: DMA Request 6 is enabled
5	REQENA_5	R/W1C	0	Enable DMA Request Enable 5 Clear 0 = REQENA_5_DIS : Write: No Effect, Read: DMA Request 5 disabled. 1 = REQENA_5_ENA: Write: Disables DMA Request 5, Read: DMA Request 5 is enabled
4	REQENA_4	R/W1C	0	Enable DMA Request Enable 4 Clear 0 = REQENA_4_DIS : Write: No Effect, Read: DMA Request 4 disabled. 1 = REQENA_4_ENA: Write: Disables DMA Request 4, Read: DMA Request 4 is enabled
3	REQENA_3	R/W1C	0	Enable DMA Request Enable 3 Clear 0 = REQENA_3_DIS : Write: No Effect, Read: DMA Request 3 disabled. 1 = REQENA_3_ENA: Write: Disables DMA Request 3, Read: DMA Request 3 is enabled
2	REQENA_2	R/W1C	0	Enable DMA Request Enable 2 Clear 0 = REQENA_2_DIS : Write: No Effect, Read: DMA Request 2 disabled. 1 = REQENA_2_ENA: Write: Disables DMA Request 2, Read: DMA Request 2 is enabled
1	REQENA_1	R/W1C	0	Enable DMA Request Enable 1 Clear 0 = REQENA_1_DIS : Write: No Effect, Read: DMA Request 1 disabled. 1 = REQENA_1_ENA: Write: Disables DMA Request 1, Read: DMA Request 1 is enabled

1-17. HETREQENC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REQENA_0	R/W1C	0	Enable DMA Request Enable 0 Clear 0 = REQENA_0_DIS : Write: No Effect, Read: DMA Request 0 disabled. 1 = REQENA_0_ENA: Write: Disables DMA Request 0, Read: DMA Request 0 is enabled

1.1.17 HETREQDS Register

N2HET1: offset = FFF7 B844h; **N2HET2:** offset = FFF7 B944h

1-17. Request Destination Select Register (HETREQDS) [offset = FFF7 B844h]

31	24	23	22	21	20	19	18	17	16
Reserved		TDBS 7	TDBS 6	TDBS 5	TDBS 4	TDBS 3	TDBS 2	TDBS 1	TDBS 0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	8	7	6	5	4	3	2	1	0
Reserved		TDS 7	TDS 6	TDS 5	TDS 4	TDS 3	TDS 2	TDS 1	TDS 0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-18. HETREQDS Register Field Descriptions

Bit	Field	Type	Reset	Description
24-31	Reserved	R	0	Read returns 0. Writes have no effect.
23	TDBS_7	R/W	0	Transfer Request 7 Destination - Both HTU and DMA 0 = TDBS_7_HTU_OR_DMA : Destination of N2HET DMA Request 7 is Controlled by bit TDS_7 1 = TDBS_7_HTU_AND_DMA: Request 7 is routed to both HTU and DMA, bit TDS_7 is ignored
22	TDBS_6	R/W	0	Transfer Request 6 Destination - Both HTU and DMA 0 = TDBS_6_HTU_OR_DMA : Destination of N2HET DMA Request 6 is Controlled by bit TDS_6 1 = TDBS_6_HTU_AND_DMA : Request 6 is routed to both HTU and DMA, bit TDS_6 is ignored
21	TDBS_5	R/W	0	Transfer Request 5 Destination - Both HTU and DMA 0 = TDBS_5_HTU_OR_DMA : Destination of N2HET DMA Request 5 is Controlled by bit TDS_5 1 = TDBS_5_HTU_AND_DMA : Request 5 is routed to both HTU and DMA, bit TDS_5 is ignored
20	TDBS_4	R/W	0	Transfer Request 4 Destination - Both HTU and DMA 0 = TDBS_4_HTU_OR_DMA : Destination of N2HET DMA Request 4 is Controlled by bit TDS_4 1 = TDBS_4_HTU_AND_DMA : Request 4 is routed to both HTU and DMA, bit TDS_4 is ignored
19	TDBS_3	R/W	0	Transfer Request 3 Destination - Both HTU and DMA 0 = TDBS_3_HTU_OR_DMA : Destination of N2HET DMA Request 3 is Controlled by bit TDS_3 1 = TDBS_3_HTU_AND_DMA : Request 3 is routed to both HTU and DMA, bit TDS_3 is ignored
18	TDBS_2	R/W	0	Transfer Request 2 Destination - Both HTU and DMA 0 = TDBS_2_HTU_OR_DMA : Destination of N2HET DMA Request 2 is Controlled by bit TDS_2 1 = TDBS_2_HTU_AND_DMA : Request 2 is routed to both HTU and DMA, bit TDS_2 is ignored

1-18. HETREQDS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	TDBS_1	R/W	0	Transfer Request 1 Destination - Both HTU and DMA 0 = TDBS_1_HTU_OR_DMA : Destination of N2HET DMA Request 1 is Controlled by bit TDS_1 1 = TDBS_1_HTU_AND_DMA : Request 1 is routed to both HTU and DMA, bit TDS_1 is ignored
16	TDBS_0	R/W	0	Transfer Request 0 Destination - Both HTU and DMA 0 = TDBS_0_HTU_OR_DMA : Destination of N2HET DMA Request 0 is Controlled by bit TDS_0 1 = TDBS_0_HTU_AND_DMA : Request 0 is routed to both HTU and DMA, bit TDS_0 is ignored
8-15	Reserved	R	0	Read returns 0. Writes have no effect.
7	TDS_7	R/W	0	Transfer Request 7 Destination - Valid only when TDSB_7 is zero. 0 = TDS_7_HTU : Destination of N2HET DMA Request 7 is HTU 1 = TDS_7_DMA : Destination of N2HET DMA Request 7 is DMA
6	TDS_6	R/W	0	Transfer Request 6 Destination - Valid only when TDSB_6 is zero. 0 = TDS_6_HTU : Destination of N2HET DMA Request 6 is HTU 1 = TDS_6_DMA : Destination of N2HET DMA Request 6 is DMA
5	TDS_5	R/W	0	Transfer Request 5 Destination - Valid only when TDSB_5 is zero. 0 = TDS_5_HTU : Destination of N2HET DMA Request 5 is HTU 1 = TDS_5_DMA : Destination of N2HET DMA Request 5 is DMA
4	TDS_4	R/W	0	Transfer Request 4 Destination - Valid only when TDSB_4 is zero. 0 = TDS_4_HTU : Destination of N2HET DMA Request 4 is HTU 1 = TDS_4_DMA : Destination of N2HET DMA Request 4 is DMA
3	TDS_3	R/W	0	Transfer Request 3 Destination - Valid only when TDSB_3 is zero. 0 = TDS_3_HTU : Destination of N2HET DMA Request 3 is HTU 1 = TDS_3_DMA : Destination of N2HET DMA Request 3 is DMA
2	TDS_2	R/W	0	Transfer Request 2 Destination - Valid only when TDSB_2 is zero. 0 = TDS_2_HTU : Destination of N2HET DMA Request 2 is HTU 1 = TDS_2_DMA : Destination of N2HET DMA Request 2 is DMA
1	TDS_1	R/W	0	Transfer Request 1 Destination - Valid only when TDSB_1 is zero. 0 = TDS_1_HTU : Destination of N2HET DMA Request 1 is HTU 1 = TDS_1_DMA : Destination of N2HET DMA Request 1 is DMA
0	TDS_0	R/W	0	Transfer Request 0 Destination - Valid only when TDSB_0 is zero. 0 = TDS_0_HTU : Destination of N2HET DMA Request 0 is HTU 1 = TDS_0_DMA : Destination of N2HET DMA Request 0 is DMA

Please refer to the device data sheet how each of the 8 N2HET request lines are connected to these modules. See also .

1.1.18 HETDIR Register

N2HET1: offset = FFF7 B84Ch; **N2HET2:** offset = FFF7 B94Ch

1-18. N2HET Direction Register (HETDIR)

31															16
HETDIR															
R/W-0															
15															0
HETDIR															
R/W-0															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-19. HETDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETDIR_31	R/W	0	N2HET[31] Pin Data Direction 0 = HETDIR_31_IN : N2HET[31] Pin is configured as input. 1 = HETDIR_31_OUT : N2HET[31] Pin is configured as output.
30	HETDIR_30	R/W	0	N2HET[30] Pin Data Direction 0 = HETDIR_30_IN : N2HET[30] Pin is configured as input. 1 = HETDIR_30_OUT : N2HET[30] Pin is configured as output.
29	HETDIR_29	R/W	0	N2HET[29] Pin Data Direction 0 = HETDIR_29_IN : N2HET[29] Pin is configured as input. 1 = HETDIR_29_OUT : N2HET[29] Pin is configured as output.
28	HETDIR_28	R/W	0	N2HET[28] Pin Data Direction 0 = HETDIR_28_IN : N2HET[28] Pin is configured as input. 1 = HETDIR_28_OUT : N2HET[28] Pin is configured as output.
27	HETDIR_27	R/W	0	N2HET[27] Pin Data Direction 0 = HETDIR_27_IN : N2HET[27] Pin is configured as input. 1 = HETDIR_27_OUT : N2HET[27] Pin is configured as output.
26	HETDIR_26	R/W	0	N2HET[26] Pin Data Direction 0 = HETDIR_26_IN : N2HET[26] Pin is configured as input. 1 = HETDIR_26_OUT : N2HET[26] Pin is configured as output.
25	HETDIR_25	R/W	0	N2HET[25] Pin Data Direction 0 = HETDIR_25_IN : N2HET[25] Pin is configured as input. 1 = HETDIR_25_OUT : N2HET[25] Pin is configured as output.
24	HETDIR_24	R/W	0	N2HET[24] Pin Data Direction 0 = HETDIR_24_IN : N2HET[24] Pin is configured as input. 1 = HETDIR_24_OUT : N2HET[24] Pin is configured as output.
23	HETDIR_23	R/W	0	N2HET[23] Pin Data Direction 0 = HETDIR_23_IN : N2HET[23] Pin is configured as input. 1 = HETDIR_23_OUT : N2HET[23] Pin is configured as output.

1-19. HETDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETDIR_22	R/W	0	N2HET[22] Pin Data Direction 0 = HETDIR_22_IN : N2HET[22] Pin is configured as input. 1 = HETDIR_22_OUT : N2HET[22] Pin is configured as output.
21	HETDIR_21	R/W	0	N2HET[21] Pin Data Direction 0 = HETDIR_21_IN : N2HET[21] Pin is configured as input. 1 = HETDIR_21_OUT : N2HET[21] Pin is configured as output.
20	HETDIR_20	R/W	0	N2HET[20] Pin Data Direction 0 = HETDIR_20_IN : N2HET[20] Pin is configured as input. 1 = HETDIR_20_OUT : N2HET[20] Pin is configured as output.
19	HETDIR_19	R/W	0	N2HET[19] Pin Data Direction 0 = HETDIR_19_IN : N2HET[19] Pin is configured as input. 1 = HETDIR_19_OUT : N2HET[19] Pin is configured as output.
18	HETDIR_18	R/W	0	N2HET[18] Pin Data Direction 0 = HETDIR_18_IN : N2HET[18] Pin is configured as input. 1 = HETDIR_18_OUT : N2HET[18] Pin is configured as output.
17	HETDIR_17	R/W	0	N2HET[17] Pin Data Direction 0 = HETDIR_17_IN : N2HET[17] Pin is configured as input. 1 = HETDIR_17_OUT : N2HET[17] Pin is configured as output.
16	HETDIR_16	R/W	0	N2HET[16] Pin Data Direction 0 = HETDIR_16_IN : N2HET[16] Pin is configured as input. 1 = HETDIR_16_OUT : N2HET[16] Pin is configured as output.
15	HETDIR_15	R/W	0	N2HET[15] Pin Data Direction 0 = HETDIR_15_IN : N2HET[15] Pin is configured as input. 1 = HETDIR_15_OUT : N2HET[15] Pin is configured as output.
14	HETDIR_14	R/W	0	N2HET[14] Pin Data Direction 0 = HETDIR_14_IN : N2HET[14] Pin is configured as input. 1 = HETDIR_14_OUT : N2HET[14] Pin is configured as output.
13	HETDIR_13	R/W	0	N2HET[13] Pin Data Direction 0 = HETDIR_13_IN : N2HET[13] Pin is configured as input. 1 = HETDIR_13_OUT : N2HET[13] Pin is configured as output.
12	HETDIR_12	R/W	0	N2HET[12] Pin Data Direction 0 = HETDIR_12_IN : N2HET[12] Pin is configured as input. 1 = HETDIR_12_OUT : N2HET[12] Pin is configured as output.
11	HETDIR_11	R/W	0	N2HET[11] Pin Data Direction 0 = HETDIR_11_IN : N2HET[11] Pin is configured as input. 1 = HETDIR_11_OUT : N2HET[11] Pin is configured as output.

1-19. HETDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETDIR_10	R/W	0	N2HET[10] Pin Data Direction 0 = HETDIR_10_IN : N2HET[10] Pin is configured as input. 1 = HETDIR_10_OUT : N2HET[10] Pin is configured as output.
9	HETDIR_9	R/W	0	N2HET[9] Pin Data Direction 0 = HETDIR_9_IN : N2HET[9] Pin is configured as input. 1 = HETDIR_9_OUT : N2HET[9] Pin is configured as output.
8	HETDIR_8	R/W	0	N2HET[8] Pin Data Direction 0 = HETDIR_8_IN : N2HET[8] Pin is configured as input. 1 = HETDIR_8_OUT : N2HET[8] Pin is configured as output.
7	HETDIR_7	R/W	0	N2HET[7] Pin Data Direction 0 = HETDIR_7_IN : N2HET[7] Pin is configured as input. 1 = HETDIR_7_OUT : N2HET[7] Pin is configured as output.
6	HETDIR_6	R/W	0	N2HET[6] Pin Data Direction 0 = HETDIR_6_IN : N2HET[6] Pin is configured as input. 1 = HETDIR_6_OUT : N2HET[6] Pin is configured as output.
5	HETDIR_5	R/W	0	N2HET[5] Pin Data Direction 0 = HETDIR_5_IN : N2HET[5] Pin is configured as input. 1 = HETDIR_5_OUT : N2HET[5] Pin is configured as output.
4	HETDIR_4	R/W	0	N2HET[4] Pin Data Direction 0 = HETDIR_4_IN : N2HET[4] Pin is configured as input. 1 = HETDIR_4_OUT : N2HET[4] Pin is configured as output.
3	HETDIR_3	R/W	0	N2HET[3] Pin Data Direction 0 = HETDIR_3_IN : N2HET[3] Pin is configured as input. 1 = HETDIR_3_OUT : N2HET[3] Pin is configured as output.
2	HETDIR_2	R/W	0	N2HET[2] Pin Data Direction 0 = HETDIR_2_IN : N2HET[2] Pin is configured as input. 1 = HETDIR_2_OUT : N2HET[2] Pin is configured as output.
1	HETDIR_1	R/W	0	N2HET[1] Pin Data Direction 0 = HETDIR_1_IN : N2HET[1] Pin is configured as input. 1 = HETDIR_1_OUT : N2HET[1] Pin is configured as output.
0	HETDIR_0	R/W	0	N2HET[0] Pin Data Direction 0 = HETDIR_0_IN : N2HET[0] Pin is configured as input. 1 = HETDIR_0_OUT : N2HET[0] Pin is configured as output.

shows how the register bits of DIR, PULDIS and PULSEL are affecting the N2HET pins.

1.1.19 HETDIN Register

N2HET1: offset = FFF7 B850h; **N2HET2:** offset = FFF7 B950h

1-19. N2HET Data Input Register (HETDIN)

31																16
HETDIN																
R-x																
15																0
HETDIN																
R-x																

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset;

1-20. HETDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETDIN_31	R	X	N2HET[31] Pin Data Input 0 = HETDIN_31_LOW : N2HET[31] Pin input is logic low. 1 = HETDIN_31_HIGH : N2HET[31] Pin input is logic high.
30	HETDIN_30	R	X	N2HET[30] Pin Data Input 0 = HETDIN_30_LOW : N2HET[30] Pin input is logic low. 1 = HETDIN_30_HIGH : N2HET[30] Pin input is logic high.
29	HETDIN_29	R	X	N2HET[29] Pin Data Input 0 = HETDIN_29_LOW : N2HET[29] Pin input is logic low. 1 = HETDIN_29_HIGH : N2HET[29] Pin input is logic high.
28	HETDIN_28	R	X	N2HET[28] Pin Data Input 0 = HETDIN_28_LOW : N2HET[28] Pin input is logic low. 1 = HETDIN_28_HIGH : N2HET[28] Pin input is logic high.
27	HETDIN_27	R	X	N2HET[27] Pin Data Input 0 = HETDIN_27_LOW : N2HET[27] Pin input is logic low. 1 = HETDIN_27_HIGH : N2HET[27] Pin input is logic high.
26	HETDIN_26	R	X	N2HET[26] Pin Data Input 0 = HETDIN_26_LOW : N2HET[26] Pin input is logic low. 1 = HETDIN_26_HIGH : N2HET[26] Pin input is logic high.
25	HETDIN_25	R	X	N2HET[25] Pin Data Input 0 = HETDIN_25_LOW : N2HET[25] Pin input is logic low. 1 = HETDIN_25_HIGH : N2HET[25] Pin input is logic high.
24	HETDIN_24	R	X	N2HET[24] Pin Data Input 0 = HETDIN_24_LOW : N2HET[24] Pin input is logic low. 1 = HETDIN_24_HIGH : N2HET[24] Pin input is logic high.
23	HETDIN_23	R	X	N2HET[23] Pin Data Input 0 = HETDIN_23_LOW : N2HET[23] Pin input is logic low. 1 = HETDIN_23_HIGH : N2HET[23] Pin input is logic high.

1-20. HETDIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETDIN_22	R	X	N2HET[22] Pin Data Input 0 = HETDIN_22_LOW : N2HET[22] Pin input is logic low. 1 = HETDIN_22_HIGH : N2HET[22] Pin input is logic high.
21	HETDIN_21	R	X	N2HET[21] Pin Data Input 0 = HETDIN_21_LOW : N2HET[21] Pin input is logic low. 1 = HETDIN_21_HIGH : N2HET[21] Pin input is logic high.
20	HETDIN_20	R	X	N2HET[20] Pin Data Input 0 = HETDIN_20_LOW : N2HET[20] Pin input is logic low. 1 = HETDIN_20_HIGH : N2HET[20] Pin input is logic high.
19	HETDIN_19	R	X	N2HET[19] Pin Data Input 0 = HETDIN_19_LOW : N2HET[19] Pin input is logic low. 1 = HETDIN_19_HIGH : N2HET[19] Pin input is logic high.
18	HETDIN_18	R	X	N2HET[18] Pin Data Input 0 = HETDIN_18_LOW : N2HET[18] Pin input is logic low. 1 = HETDIN_18_HIGH : N2HET[18] Pin input is logic high.
17	HETDIN_17	R	X	N2HET[17] Pin Data Input 0 = HETDIN_17_LOW : N2HET[17] Pin input is logic low. 1 = HETDIN_17_HIGH : N2HET[17] Pin input is logic high.
16	HETDIN_16	R	X	N2HET[16] Pin Data Input 0 = HETDIN_16_LOW : N2HET[16] Pin input is logic low. 1 = HETDIN_16_HIGH : N2HET[16] Pin input is logic high.
15	HETDIN_15	R	X	N2HET[15] Pin Data Input 0 = HETDIN_15_LOW : N2HET[15] Pin input is logic low. 1 = HETDIN_15_HIGH : N2HET[15] Pin input is logic high.
14	HETDIN_14	R	X	N2HET[14] Pin Data Input 0 = HETDIN_14_LOW : N2HET[14] Pin input is logic low. 1 = HETDIN_14_HIGH : N2HET[14] Pin input is logic high.
13	HETDIN_13	R	X	N2HET[13] Pin Data Input 0 = HETDIN_13_LOW : N2HET[13] Pin input is logic low. 1 = HETDIN_13_HIGH : N2HET[13] Pin input is logic high.
12	HETDIN_12	R	X	N2HET[12] Pin Data Input 0 = HETDIN_12_LOW : N2HET[12] Pin input is logic low. 1 = HETDIN_12_HIGH : N2HET[12] Pin input is logic high.
11	HETDIN_11	R	X	N2HET[11] Pin Data Input 0 = HETDIN_11_LOW : N2HET[11] Pin input is logic low. 1 = HETDIN_11_HIGH : N2HET[11] Pin input is logic high.

1-20. HETDIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETDIN_10	R	X	N2HET[10] Pin Data Input 0 = HETDIN_10_LOW : N2HET[10] Pin input is logic low. 1 = HETDIN_10_HIGH : N2HET[10] Pin input is logic high.
9	HETDIN_9	R	X	N2HET[9] Pin Data Input 0 = HETDIN_9_LOW : N2HET[9] Pin input is logic low. 1 = HETDIN_9_HIGH : N2HET[9] Pin input is logic high.
8	HETDIN_8	R	X	N2HET[8] Pin Data Input 0 = HETDIN_8_LOW : N2HET[8] Pin input is logic low. 1 = HETDIN_8_HIGH : N2HET[8] Pin input is logic high.
7	HETDIN_7	R	X	N2HET[7] Pin Data Input 0 = HETDIN_7_LOW : N2HET[7] Pin input is logic low. 1 = HETDIN_7_HIGH : N2HET[7] Pin input is logic high.
6	HETDIN_6	R	X	N2HET[6] Pin Data Input 0 = HETDIN_6_LOW : N2HET[6] Pin input is logic low. 1 = HETDIN_6_HIGH : N2HET[6] Pin input is logic high.
5	HETDIN_5	R	X	N2HET[5] Pin Data Input 0 = HETDIN_5_LOW : N2HET[5] Pin input is logic low. 1 = HETDIN_5_HIGH : N2HET[5] Pin input is logic high.
4	HETDIN_4	R	X	N2HET[4] Pin Data Input 0 = HETDIN_4_LOW : N2HET[4] Pin input is logic low. 1 = HETDIN_4_HIGH : N2HET[4] Pin input is logic high.
3	HETDIN_3	R	X	N2HET[3] Pin Data Input 0 = HETDIN_3_LOW : N2HET[3] Pin input is logic low. 1 = HETDIN_3_HIGH : N2HET[3] Pin input is logic high.
2	HETDIN_2	R	X	N2HET[2] Pin Data Input 0 = HETDIN_2_LOW : N2HET[2] Pin input is logic low. 1 = HETDIN_2_HIGH : N2HET[2] Pin input is logic high.
1	HETDIN_1	R	X	N2HET[1] Pin Data Input 0 = HETDIN_1_LOW : N2HET[1] Pin input is logic low. 1 = HETDIN_1_HIGH : N2HET[1] Pin input is logic high.
0	HETDIN_0	R	X	N2HET[0] Pin Data Input 0 = HETDIN_0_LOW : N2HET[0] Pin input is logic low. 1 = HETDIN_0_HIGH : N2HET[0] Pin input is logic high.

1.1.20 HETDOUT Register

N2HET1: offset = FFF7 B854h; **N2HET2:** offset = FFF7 B954h

1-20. N2HET Data Output Register (HETDOUT)

31	16
HETDOUT	
R/W-0	

15	0
HETDOUT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

1-21. HETDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETDOUT_31	R/W	0	N2HET[31] Pin Data Output 0 = HETDOUT_31_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_31_HIGH : Read: Input is High, Write: Output is High when Enabled.
30	HETDOUT_30	R/W	0	N2HET[30] Pin Data Output 0 = HETDOUT_30_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_30_HIGH : Read: Input is High, Write: Output is High when Enabled.
29	HETDOUT_29	R/W	0	N2HET[29] Pin Data Output 0 = HETDOUT_29_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_29_HIGH : Read: Input is High, Write: Output is High when Enabled.
28	HETDOUT_28	R/W	0	N2HET[28] Pin Data Output 0 = HETDOUT_28_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_28_HIGH : Read: Input is High, Write: Output is High when Enabled.
27	HETDOUT_27	R/W	0	N2HET[27] Pin Data Output 0 = HETDOUT_27_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_27_HIGH :Read: Input is High, Write: Output is High when Enabled.
26	HETDOUT_26	R/W	0	N2HET[26] Pin Data Output 0 = HETDOUT_26_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_26_HIGH : Read: Input is High, Write: Output is High when Enabled.
25	HETDOUT_25	R/W	0	N2HET[25] Pin Data Output 0 = HETDOUT_25_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_25_HIGH : Read: Input is High, Write: Output is High when Enabled.
24	HETDOUT_24	R/W	0	N2HET[24] Pin Data Output 0 = HETDOUT_24_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_24_HIGH : Read: Input is High, Write: Output is High when Enabled.
23	HETDOUT_23	R/W	0	N2HET[23] Pin Data Output 0 = HETDOUT_23_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_23_HIGH : Read: Input is High, Write: Output is High when Enabled.

1-21. HETDOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETDOUT_22	R/W	0	N2HET[22] Pin Data Output 0 = HETDOUT_22_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_22_HIGH : Read: Input is High, Write: Output is High when Enabled.
21	HETDOUT_21	R/W	0	N2HET[21] Pin Data Output 0 = HETDOUT_21_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_21_HIGH : Read: Input is High, Write: Output is High when Enabled.
20	HETDOUT_20	R/W	0	N2HET[20] Pin Data Output 0 = HETDOUT_20_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_20_HIGH : Read: Input is High, Write: Output is High when Enabled.
19	HETDOUT_19	R/W	0	N2HET[19] Pin Data Output 0 = HETDOUT_19_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_19_HIGH : Read: Input is High, Write: Output is High when Enabled.
18	HETDOUT_18	R/W	0	N2HET[18] Pin Data Output 0 = HETDOUT_18_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_18_HIGH : Read: Input is High, Write: Output is High when Enabled.
17	HETDOUT_17	R/W	0	N2HET[17] Pin Data Output 0 = HETDOUT_17_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_17_HIGH : Read: Input is High, Write: Output is High when Enabled.
16	HETDOUT_16	R/W	0	N2HET[16] Pin Data Output 0 = HETDOUT_16_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_16_HIGH : Read: Input is High, Write: Output is High when Enabled.
15	HETDOUT_15	R/W	0	N2HET[15] Pin Data Output 0 = HETDOUT_15_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_15_HIGH : Read: Input is High, Write: Output is High when Enabled.
14	HETDOUT_14	R/W	0	N2HET[14] Pin Data Output 0 = HETDOUT_14_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_14_HIGH : Read: Input is High, Write: Output is High when Enabled.
13	HETDOUT_13	R/W	0	N2HET[13] Pin Data Output 0 = HETDOUT_13_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_13_HIGH : Read: Input is High, Write: Output is High when Enabled.
12	HETDOUT_12	R/W	0	N2HET[12] Pin Data Output 0 = HETDOUT_12_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_12_HIGH : Read: Input is High, Write: Output is High when Enabled.
11	HETDOUT_11	R/W	0	N2HET[11] Pin Data Output 0 = HETDOUT_11_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_11_HIGH : Read: Input is High, Write: Output is High when Enabled.

1-21. HETDOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETDOUT_10	R/W	0	N2HET[10] Pin Data Output 0 = HETDOUT_10_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_10_HIGH : Read: Input is High, Write: Output is High when Enabled.
9	HETDOUT_9	R/W	0	N2HET[9] Pin Data Output 0 = HETDOUT_9_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_9_HIGH : Read: Input is High, Write: Output is High when Enabled.
8	HETDOUT_8	R/W	0	N2HET[8] Pin Data Output 0 = HETDOUT_8_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_8_HIGH : Read: Input is High, Write: Output is High when Enabled.
7	HETDOUT_7	R/W	0	N2HET[7] Pin Data Output 0 = HETDOUT_7_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_7_HIGH : Read: Input is High, Write: Output is High when Enabled.
6	HETDOUT_6	R/W	0	N2HET[6] Pin Data Output 0 = HETDOUT_6_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_6_HIGH : Read: Input is High, Write: Output is High when Enabled.
5	HETDOUT_5	R/W	0	N2HET[5] Pin Data Output 0 = HETDOUT_5_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_5_HIGH : Read: Input is High, Write: Output is High when Enabled.
4	HETDOUT_4	R/W	0	N2HET[4] Pin Data Output 0 = HETDOUT_4_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_4_HIGH : Read: Input is High, Write: Output is High when Enabled.
3	HETDOUT_3	R/W	0	N2HET[3] Pin Data Output 0 = HETDOUT_3_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_3_HIGH : Read: Input is High, Write: Output is High when Enabled.
2	HETDOUT_2	R/W	0	N2HET[2] Pin Data Output 0 = HETDOUT_2_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_2_HIGH : Read: Input is High, Write: Output is High when Enabled.
1	HETDOUT_1	R/W	0	N2HET[1] Pin Data Output 0 = HETDOUT_1_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_1_HIGH : Read: Input is High, Write: Output is High when Enabled.
0	HETDOUT_0	R/W	0	N2HET[0] Pin Data Output 0 = HETDOUT_0_LOW : Read: Input is Low, Write: Output is Low when Enabled 1 = HETDOUT_0_HIGH : Read: Input is High, Write: Output is High when Enabled.

1.1.21 HETDSET Register

N2HET1: offset = FFF7 B858h; **N2HET2:** offset = FFF7 B958h

1-21. N2HET Data Set Register (HETDSET)

31	16
HETDSET	
R/WS-0	

15	0
HETDSET	
R/WS-0	

LEGEND: R/W = Read/Write; R = Read only; S = Set; -*n* = value after reset

1-22. HETDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETDSET_31	R/W1S	0	N2HET[31] Pin Data Output 0 = HETDSET_31_LOW : Read: HETDOUT_31 is 0, Write: No Effect 1 = HETDSET_31_HIGH : Read: HETDOUT_31 is 1, Write: Sets HETDOUT_31 to 1
30	HETDSET_30	R/W1S	0	N2HET[30] Pin Data Output 0 = HETDSET_30_LOW : Read: HETDOUT_30 is 0, Write: No Effect 1 = HETDSET_30_HIGH : Read: HETDOUT_30 is 1, Write: Sets HETDOUT_30 to 1
29	HETDSET_29	R/W1S	0	N2HET[29] Pin Data Output 0 = HETDSET_29_LOW : Read: HETDOUT_29 is 0, Write: No Effect 1 = HETDSET_29_HIGH : Read: HETDOUT_29 is 1, Write: Sets HETDOUT_29 to 1
28	HETDSET_28	R/W1S	0	N2HET[28] Pin Data Output 0 = HETDSET_28_LOW : Read: HETDOUT_28 is 0, Write: No Effect 1 = HETDSET_28_HIGH : Read: HETDOUT_28 is 1, Write: Sets HETDOUT_28 to 1
27	HETDSET_27	R/W1S	0	N2HET[27] Pin Data Output 0 = HETDSET_27_LOW : Read: HETDOUT_27 is 0, Write: No Effect 1 = HETDSET_27_HIGH :Read: HETDOUT_27 is 1, Write: Sets HETDOUT_27 to 1
26	HETDSET_26	R/W1S	0	N2HET[26] Pin Data Output 0 = HETDSET_26_LOW : Read: HETDOUT_26 is 0, Write: No Effect 1 = HETDSET_26_HIGH : Read: HETDOUT_26 is 1, Write: Sets HETDOUT_26 to 1
25	HETDSET_25	R/W1S	0	N2HET[25] Pin Data Output 0 = HETDSET_25_LOW : Read: HETDOUT_25 is 0, Write: No Effect 1 = HETDSET_25_HIGH : Read: HETDOUT_25 is 1, Write: Sets HETDOUT_25 to 1
24	HETDSET_24	R/W1S	0	N2HET[24] Pin Data Output 0 = HETDSET_24_LOW : Read: HETDOUT_24 is 0, Write: No Effect 1 = HETDSET_24_HIGH : Read: HETDOUT_24 is 1, Write: Sets HETDOUT_24 to 1

1-22. HETDSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	HETDSET_23	R/W1S	0	N2HET[23] Pin Data Output 0 = HETDSET_23_LOW : Read: HETDOUT_23 is 0, Write: No Effect 1 = HETDSET_23_HIGH : Read: HETDOUT_23 is 1, Write: Sets HETDOUT_23 to 1
22	HETDSET_22	R/W1S	0	N2HET[22] Pin Data Output 0 = HETDSET_22_LOW : Read: HETDOUT_22 is 0, Write: No Effect 1 = HETDSET_22_HIGH : Read: HETDOUT_22 is 1, Write: Sets HETDOUT_22 to 1
21	HETDSET_21	R/W1S	0	N2HET[21] Pin Data Output 0 = HETDSET_21_LOW : Read: HETDOUT_21 is 0, Write: No Effect 1 = HETDSET_21_HIGH : Read: HETDOUT_21 is 1, Write: Sets HETDOUT_21 to 1
20	HETDSET_20	R/W1S	0	N2HET[20] Pin Data Output 0 = HETDSET_20_LOW : Read: HETDOUT_20 is 0, Write: No Effect 1 = HETDSET_20_HIGH : Read: HETDOUT_20 is 1, Write: Sets HETDOUT_20 to 1
19	HETDSET_19	R/W1S	0	N2HET[19] Pin Data Output 0 = HETDSET_19_LOW : Read: HETDOUT_19 is 0, Write: No Effect 1 = HETDSET_19_HIGH : Read: HETDOUT_19 is 1, Write: Sets HETDOUT_19 to 1
18	HETDSET_18	R/W1S	0	N2HET[18] Pin Data Output 0 = HETDSET_18_LOW : Read: HETDOUT_18 is 0, Write: No Effect 1 = HETDSET_18_HIGH : Read: HETDOUT_18 is 1, Write: Sets HETDOUT_18 to 1
17	HETDSET_17	R/W1S	0	N2HET[17] Pin Data Output 0 = HETDSET_17_LOW : Read: HETDOUT_17 is 0, Write: No Effect 1 = HETDSET_17_HIGH : Read: HETDOUT_17 is 1, Write: Sets HETDOUT_17 to 1
16	HETDSET_16	R/W1S	0	N2HET[16] Pin Data Output 0 = HETDSET_16_LOW : Read: HETDOUT_16 is 0, Write: No Effect 1 = HETDSET_16_HIGH : Read: HETDOUT_16 is 1, Write: Sets HETDOUT_16 to 1
15	HETDSET_15	R/W1S	0	N2HET[15] Pin Data Output 0 = HETDSET_15_LOW : Read: HETDOUT_15 is 0, Write: No Effect 1 = HETDSET_15_HIGH : Read: HETDOUT_15 is 1, Write: Sets HETDOUT_15 to 1
14	HETDSET_14	R/W1S	0	N2HET[14] Pin Data Output 0 = HETDSET_14_LOW : Read: HETDOUT_14 is 0, Write: No Effect 1 = HETDSET_14_HIGH : Read: HETDOUT_14 is 1, Write: Sets HETDOUT_14 to 1

1-22. HETDSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	HETDSET_13	R/W1S	0	N2HET[13] Pin Data Output 0 = HETDSET_13_LOW : Read: HETDOUT_13 is 0, Write: No Effect 1 = HETDSET_13_HIGH : Read: HETDOUT_13 is 1, Write: Sets HETDOUT_13 to 1
12	HETDSET_12	R/W1S	0	N2HET[12] Pin Data Output 0 = HETDSET_12_LOW : Read: HETDOUT_12 is 0, Write: No Effect 1 = HETDSET_12_HIGH : Read: HETDOUT_12 is 1, Write: Sets HETDOUT_12 to 1
11	HETDSET_11	R/W1S	0	N2HET[11] Pin Data Output 0 = HETDSET_11_LOW : Read: HETDOUT_11 is 0, Write: No Effect 1 = HETDSET_11_HIGH : Read: HETDOUT_11 is 1, Write: Sets HETDOUT_11 to 1
10	HETDSET_10	R/W1S	0	N2HET[10] Pin Data Output 0 = HETDSET_10_LOW : Read: HETDOUT_10 is 0, Write: No Effect 1 = HETDSET_10_HIGH : Read: HETDOUT_10 is 1, Write: Sets HETDOUT_10 to 1
9	HETDSET_9	R/W1S	0	N2HET[9] Pin Data Output 0 = HETDSET_9_LOW : Read: HETDOUT_9 is 0, Write: No Effect 1 = HETDSET_9_HIGH : Read: HETDOUT_9 is 1, Write: Sets HETDOUT_9 to 1
8	HETDSET_8	R/W1S	0	N2HET[8] Pin Data Output 0 = HETDSET_8_LOW : Read: HETDOUT_8 is 0, Write: No Effect 1 = HETDSET_8_HIGH : Read: HETDOUT_8 is 1, Write: Sets HETDOUT_8 to 1
7	HETDSET_7	R/W1S	0	N2HET[7] Pin Data Output 0 = HETDSET_7_LOW : Read: HETDOUT_7 is 0, Write: No Effect 1 = HETDSET_7_HIGH : Read: HETDOUT_7 is 1, Write: Sets HETDOUT_7 to 1
6	HETDSET_6	R/W1S	0	N2HET[6] Pin Data Output 0 = HETDSET_6_LOW : Read: HETDOUT_6 is 0, Write: No Effect 1 = HETDSET_6_HIGH : Read: HETDOUT_6 is 1, Write: Sets HETDOUT_6 to 1
5	HETDSET_5	R/W1S	0	N2HET[5] Pin Data Output 0 = HETDSET_5_LOW : Read: HETDOUT_5 is 0, Write: No Effect 1 = HETDSET_5_HIGH : Read: HETDOUT_5 is 1, Write: Sets HETDOUT_5 to 1
4	HETDSET_4	R/W1S	0	N2HET[4] Pin Data Output 0 = HETDSET_4_LOW : Read: HETDOUT_4 is 0, Write: No Effect 1 = HETDSET_4_HIGH : Read: HETDOUT_4 is 1, Write: Sets HETDOUT_4 to 1

1-22. HETDSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	HETDSET_3	R/W1S	0	N2HET[3] Pin Data Output 0 = HETDSET_3_LOW : Read: HETDOUT_3 is 0, Write: No Effect 1 = HETDSET_3_HIGH : Read: HETDOUT_3 is 1, Write: Sets HETDOUT_3 to 1
2	HETDSET_2	R/W1S	0	N2HET[2] Pin Data Output 0 = HETDSET_2_LOW : Read: HETDOUT_2 is 0, Write: No Effect 1 = HETDSET_2_HIGH : Read: HETDOUT_2 is 1, Write: Sets HETDOUT_2 to 1
1	HETDSET_1	R/W1S	0	N2HET[1] Pin Data Output 0 = HETDSET_1_LOW : Read: HETDOUT_1 is 0, Write: No Effect 1 = HETDSET_1_HIGH : Read: HETDOUT_1 is 1, Write: Setsenum HETDOUT_1 to 1
0	HETDSET_0	R/W1S	0	N2HET[0] Pin Data Output 0 = HETDSET_0_LOW : Read: HETDOUT_0 is 0, Write: No Effect 1 = HETDSET_0_HIGH : Read: HETDOUT_0 is 1, Write: Sets HETDOUT_0 to 1

1.1.22 HETDCLR Register

N2HET1: offset = FFF7 B85Ch; **N2HET2:** offset = FFF7 B95Ch

1-22. N2HET Data Clear Register (HETDCLR)

31	16
HETDCLR	
R/WC-0	
15	0
HETDCLR	
R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

1-23. HETDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETDCLR_31	R/W1C	0	N2HET[31] Pin Data Output 0 = HETDCLR_31_LOW : Read: HETDOUT_31 is 0, Write: No Effect 1 = HETDCLR_31_HIGH : Read: HETDOUT_31 is 1, Write: Clears HETDOUT_31 to 0
30	HETDCLR_30	R/W1C	0	N2HET[30] Pin Data Output 0 = HETDCLR_30_LOW : Read: HETDOUT_30 is 0, Write: No Effect 1 = HETDCLR_30_HIGH : Read: HETDOUT_30 is 1, Write: Clears HETDOUT_30 to 0
29	HETDCLR_29	R/W1C	0	N2HET[29] Pin Data Output 0 = HETDCLR_29_LOW : Read: HETDOUT_29 is 0, Write: No Effect 1 = HETDCLR_29_HIGH : Read: HETDOUT_29 is 1, Write: Clears HETDOUT_29 to 0
28	HETDCLR_28	R/W1C	0	N2HET[28] Pin Data Output 0 = HETDCLR_28_LOW : Read: HETDOUT_28 is 0, Write: No Effect 1 = HETDCLR_28_HIGH : Read: HETDOUT_28 is 1, Write: Clears HETDOUT_28 to 0
27	HETDCLR_27	R/W1C	0	N2HET[27] Pin Data Output 0 = HETDCLR_27_LOW : Read: HETDOUT_27 is 0, Write: No Effect 1 = HETDCLR_27_HIGH :Read: HETDOUT_27 is 1, Write: Clears HETDOUT_27 to 0
26	HETDCLR_26	R/W1C	0	N2HET[26] Pin Data Output 0 = HETDCLR_26_LOW : Read: HETDOUT_26 is 0, Write: No Effect 1 = HETDCLR_26_HIGH : Read: HETDOUT_26 is 1, Write: Clears HETDOUT_26 to 0
25	HETDCLR_25	R/W1C	0	N2HET[25] Pin Data Output 0 = HETDCLR_25_LOW : Read: HETDOUT_25 is 0, Write: No Effect 1 = HETDCLR_25_HIGH : Read: HETDOUT_25 is 1, Write: Clears HETDOUT_25 to 0
24	HETDCLR_24	R/W1C	0	N2HET[24] Pin Data Output 0 = HETDCLR_24_LOW : Read: HETDOUT_24 is 0, Write: No Effect 1 = HETDCLR_24_HIGH : Read: HETDOUT_24 is 1, Write: Clears HETDOUT_24 to 0

1-23. HETDCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	HETDCLR_23	R/W1C	0	N2HET[23] Pin Data Output 0 = HETDCLR_23_LOW : Read: HETDOUT_23 is 0, Write: No Effect 1 = HETDCLR_23_HIGH : Read: HETDOUT_23 is 1, Write: Clears HETDOUT_23 to 0
22	HETDCLR_22	R/W1C	0	N2HET[22] Pin Data Output 0 = HETDCLR_22_LOW : Read: HETDOUT_22 is 0, Write: No Effect 1 = HETDCLR_22_HIGH : Read: HETDOUT_22 is 1, Write: Clears HETDOUT_22 to 0
21	HETDCLR_21	R/W1C	0	N2HET[21] Pin Data Output 0 = HETDCLR_21_LOW : Read: HETDOUT_21 is 0, Write: No Effect 1 = HETDCLR_21_HIGH : Read: HETDOUT_21 is 1, Write: Clears HETDOUT_21 to 0
20	HETDCLR_20	R/W1C	0	N2HET[20] Pin Data Output 0 = HETDCLR_20_LOW : Read: HETDOUT_20 is 0, Write: No Effect 1 = HETDCLR_20_HIGH : Read: HETDOUT_20 is 1, Write: Clears HETDOUT_20 to 0
19	HETDCLR_19	R/W1C	0	N2HET[19] Pin Data Output 0 = HETDCLR_19_LOW : Read: HETDOUT_19 is 0, Write: No Effect 1 = HETDCLR_19_HIGH : Read: HETDOUT_19 is 1, Write: Clears HETDOUT_19 to 0
18	HETDCLR_18	R/W1C	0	N2HET[18] Pin Data Output 0 = HETDCLR_18_LOW : Read: HETDOUT_18 is 0, Write: No Effect 1 = HETDCLR_18_HIGH : Read: HETDOUT_18 is 1, Write: Clears HETDOUT_18 to 0
17	HETDCLR_17	R/W1C	0	N2HET[17] Pin Data Output 0 = HETDCLR_17_LOW : Read: HETDOUT_17 is 0, Write: No Effect 1 = HETDCLR_17_HIGH : Read: HETDOUT_17 is 1, Write: Clears HETDOUT_17 to 0
16	HETDCLR_16	R/W1C	0	N2HET[16] Pin Data Output 0 = HETDCLR_16_LOW : Read: HETDOUT_16 is 0, Write: No Effect 1 = HETDCLR_16_HIGH : Read: HETDOUT_16 is 1, Write: Clears HETDOUT_16 to 0
15	HETDCLR_15	R/W1C	0	N2HET[15] Pin Data Output 0 = HETDCLR_15_LOW : Read: HETDOUT_15 is 0, Write: No Effect 1 = HETDCLR_15_HIGH : Read: HETDOUT_15 is 1, Write: Clears HETDOUT_15 to 0
14	HETDCLR_14	R/W1C	0	N2HET[14] Pin Data Output 0 = HETDCLR_14_LOW : Read: HETDOUT_14 is 0, Write: No Effect 1 = HETDCLR_14_HIGH : Read: HETDOUT_14 is 1, Write: Clears HETDOUT_14 to 0

1-23. HETDCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	HETDCLR_13	R/W1C	0	N2HET[13] Pin Data Output 0 = HETDCLR_13_LOW : Read: HETDOUT_13 is 0, Write: No Effect 1 = HETDCLR_13_HIGH : Read: HETDOUT_13 is 1, Write: Clears HETDOUT_13 to 0
12	HETDCLR_12	R/W1C	0	N2HET[12] Pin Data Output 0 = HETDCLR_12_LOW : Read: HETDOUT_12 is 0, Write: No Effect 1 = HETDCLR_12_HIGH : Read: HETDOUT_12 is 1, Write: Clears HETDOUT_12 to 0
11	HETDCLR_11	R/W1C	0	N2HET[11] Pin Data Output 0 = HETDCLR_11_LOW : Read: HETDOUT_11 is 0, Write: No Effect 1 = HETDCLR_11_HIGH : Read: HETDOUT_11 is 1, Write: Clears HETDOUT_11 to 0
10	HETDCLR_10	R/W1C	0	N2HET[10] Pin Data Output 0 = HETDCLR_10_LOW : Read: HETDOUT_10 is 0, Write: No Effect 1 = HETDCLR_10_HIGH : Read: HETDOUT_10 is 1, Write: Clears HETDOUT_10 to 0
9	HETDCLR_9	R/W1C	0	N2HET[9] Pin Data Output 0 = HETDCLR_9_LOW : Read: HETDOUT_9 is 0, Write: No Effect 1 = HETDCLR_9_HIGH : Read: HETDOUT_9 is 1, Write: Clears HETDOUT_9 to 0
8	HETDCLR_8	R/W1C	0	N2HET[8] Pin Data Output 0 = HETDCLR_8_LOW : Read: HETDOUT_8 is 0, Write: No Effect 1 = HETDCLR_8_HIGH : Read: HETDOUT_8 is 1, Write: Clears HETDOUT_ 8to 0
7	HETDCLR_7	R/W1C	0	N2HET[7] Pin Data Output 0 = HETDCLR_7_LOW : Read: HETDOUT_7 is 0, Write: No Effect 1 = HETDCLR_7_HIGH : Read: HETDOUT_7 is 1, Write: Clears HETDOUT_7 to 0
6	HETDCLR_6	R/W1C	0	N2HET[6] Pin Data Output 0 = HETDCLR_6_LOW : Read: HETDOUT_6 is 0, Write: No Effect 1 = HETDCLR_6_HIGH : Read: HETDOUT_6 is 1, Write: Clears HETDOUT_6 to 0
5	HETDCLR_5	R/W1C	0	N2HET[5] Pin Data Output 0 = HETDCLR_5_LOW : Read: HETDOUT_5 is 0, Write: No Effect 1 = HETDCLR_5_HIGH : Read: HETDOUT_5 is 1, Write: Clears HETDOUT_5 to 0
4	HETDCLR_4	R/W1C	0	N2HET[4] Pin Data Output 0 = HETDCLR_4_LOW : Read: HETDOUT_4 is 0, Write: No Effect 1 = HETDCLR_4_HIGH : Read: HETDOUT_4 is 1, Write: Clears HETDOUT_4 to 0
3	HETDCLR_3	R/W1C	0	N2HET[3] Pin Data Output 0 = HETDCLR_3_LOW : Read: HETDOUT_3 is 0, Write: No Effect 1 = HETDCLR_3_HIGH : Read: HETDOUT_3 is 1, Write: Clears HETDOUT_3 to 0
2	HETDCLR_2	R/W1C	0	N2HET[2] Pin Data Output 0 = HETDCLR_2_LOW : Read: HETDOUT_2 is 0, Write: No Effect 1 = HETDCLR_2_HIGH : Read: HETDOUT_2 is 1, Write: Clears HETDOUT_2 to 0

1-23. HETDCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	HETDCLR_1	R/W1C	0	N2HET[1] Pin Data Output 0 = HETDCLR_1_LOW : Read: HETDOUT_1 is 0, Write: No Effect 1 = HETDCLR_1_HIGH : Read: HETDOUT_1 is 1, Write: Clears HETDOUT_1 to 0
0	HETDCLR_0	R/W1C	0	N2HET[0] Pin Data Output 0 = HETDCLR_0_LOW : Read: HETDOUT_0 is 0, Write: No Effect 1 = HETDCLR_0_HIGH : Read: HETDOUT_0 is 1, Write: Clears HETDOUT_0 to 0

1.1.23 HETPDR Register

Values in this register enable or disable the open drain capability of the data pins.
N2HET1: offset = FFF7 B860h; **N2HET2:** offset = FFF7 B960h

1-23. N2HET Open Drain Register (HETPDR)

31		16
	HETPDR	
	R/W-0	
15		0
	HETPDR	
	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-24. HETPDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETPDR_31	R/W	0	N2HET[31] Pin Drive Mode 0 = HETPDR_31_PP : N2HET[31] Pin Driven in Push-Pull Mode 1 = HETPDR_31_OD : N2HET[31] Pin Driven in Open-Drain Mode
30	HETPDR_30	R/W	0	N2HET[30] Pin Drive Mode 0 = HETPDR_30_PP : N2HET[30] Pin Driven in Push-Pull Mode 1 = HETPDR_30_OD : N2HET[30] Pin Driven in Open-Drain Mode
29	HETPDR_29	R/W	0	N2HET[29] Pin Drive Mode 0 = HETPDR_29_PP : N2HET[29] Pin Driven in Push-Pull Mode 1 = HETPDR_29_OD : N2HET[29] Pin Driven in Open-Drain Mode
28	HETPDR_28	R/W	0	N2HET[28] Pin Drive Mode 0 = HETPDR_28_PP : N2HET[28] Pin Driven in Push-Pull Mode 1 = HETPDR_28_OD : N2HET[28] Pin Driven in Open-Drain Mode
27	HETPDR_27	R/W	0	N2HET[27] Pin Drive Mode 0 = HETPDR_27_PP : N2HET[27] Pin Driven in Push-Pull Mode 1 = HETPDR_27_OD : N2HET[27] Pin Driven in Open-Drain Mode
26	HETPDR_26	R/W	0	N2HET[26] Pin Drive Mode 0 = HETPDR_26_PP : N2HET[26] Pin Driven in Push-Pull Mode 1 = HETPDR_26_OD : N2HET[26] Pin Driven in Open-Drain Mode
25	HETPDR_25	R/W	0	N2HET[25] Pin Drive Mode 0 = HETPDR_25_PP : N2HET[25] Pin Driven in Push-Pull Mode 1 = HETPDR_25_OD : N2HET[25] Pin Driven in Open-Drain Mode
24	HETPDR_24	R/W	0	N2HET[24] Pin Drive Mode 0 = HETPDR_24_PP : N2HET[24] Pin Driven in Push-Pull Mode 1 = HETPDR_24_OD : N2HET[24] Pin Driven in Open-Drain Mode
23	HETPDR_23	R/W	0	N2HET[23] Pin Drive Mode 0 = HETPDR_23_PP : N2HET[23] Pin Driven in Push-Pull Mode 1 = HETPDR_23_OD : N2HET[23] Pin Driven in Open-Drain Mode

1-24. HETPDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETPDR_22	R/W	0	N2HET[22] Pin Drive Mode 0 = HETPDR_22_PP : N2HET[22] Pin Driven in Push-Pull Mode 1 = HETPDR_22_OD : N2HET[22] Pin Driven in Open-Drain Mode
21	HETPDR_21	R/W	0	N2HET[21] Pin Drive Mode 0 = HETPDR_21_PP : N2HET[21] Pin Driven in Push-Pull Mode 1 = HETPDR_21_OD : N2HET[21] Pin Driven in Open-Drain Mode
20	HETPDR_20	R/W	0	N2HET[20] Pin Drive Mode 0 = HETPDR_20_PP : N2HET[20] Pin Driven in Push-Pull Mode 1 = HETPDR_20_OD : N2HET[20] Pin Driven in Open-Drain Mode
19	HETPDR_19	R/W	0	N2HET[19] Pin Drive Mode 0 = HETPDR_19_PP : N2HET[19] Pin Driven in Push-Pull Mode 1 = HETPDR_19_OD : N2HET[19] Pin Driven in Open-Drain Mode
18	HETPDR_18	R/W	0	N2HET[18] Pin Drive Mode 0 = HETPDR_18_PP : N2HET[18] Pin Driven in Push-Pull Mode 1 = HETPDR_18_OD : N2HET[18] Pin Driven in Open-Drain Mode
17	HETPDR_17	R/W	0	N2HET[17] Pin Drive Mode 0 = HETPDR_17_PP : N2HET[17] Pin Driven in Push-Pull Mode 1 = HETPDR_17_OD : N2HET[17] Pin Driven in Open-Drain Mode
16	HETPDR_16	R/W	0	N2HET[16] Pin Drive Mode 0 = HETPDR_16_PP : N2HET[16] Pin Driven in Push-Pull Mode 1 = HETPDR_16_OD : N2HET[16] Pin Driven in Open-Drain Mode
15	HETPDR_15	R/W	0	N2HET[15] Pin Drive Mode 0 = HETPDR_15_PP : N2HET[15] Pin Driven in Push-Pull Mode 1 = HETPDR_15_OD : N2HET[15] Pin Driven in Open-Drain Mode
14	HETPDR_14	R/W	0	N2HET[14] Pin Drive Mode 0 = HETPDR_14_PP : N2HET[14] Pin Driven in Push-Pull Mode 1 = HETPDR_14_OD : N2HET[14] Pin Driven in Open-Drain Mode
13	HETPDR_13	R/W	0	N2HET[13] Pin Drive Mode 0 = HETPDR_13_PP : N2HET[13] Pin Driven in Push-Pull Mode 1 = HETPDR_13_OD : N2HET[13] Pin Driven in Open-Drain Mode
12	HETPDR_12	R/W	0	N2HET[12] Pin Drive Mode 0 = HETPDR_12_PP : N2HET[12] Pin Driven in Push-Pull Mode 1 = HETPDR_12_OD : N2HET[12] Pin Driven in Open-Drain Mode
11	HETPDR_11	R/W	0	N2HET[11] Pin Drive Mode 0 = HETPDR_11_PP : N2HET[11] Pin Driven in Push-Pull Mode 1 = HETPDR_11_OD : N2HET[11] Pin Driven in Open-Drain Mode

1-24. HETPDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETPDR_10	R/W	0	N2HET[10] Pin Drive Mode 0 = HETPDR_10_PP : N2HET[10] Pin Driven in Push-Pull Mode 1 = HETPDR_10_OD : N2HET[10] Pin Driven in Open-Drain Mode
9	HETPDR_9	R/W	0	N2HET[9] Pin Drive Mode 0 = HETPDR_9_PP : N2HET[9] Pin Driven in Push-Pull Mode 1 = HETPDR_9_OD : N2HET[9] Pin Driven in Open-Drain Mode
8	HETPDR_8	R/W	0	N2HET[8] Pin Drive Mode 0 = HETPDR_8_PP : N2HET[8] Pin Driven in Push-Pull Mode 1 = HETPDR_8_OD : N2HET[8] Pin Driven in Open-Drain Mode
7	HETPDR_7	R/W	0	N2HET[7] Pin Drive Mode 0 = HETPDR_7_PP : N2HET[7] Pin Driven in Push-Pull Mode 1 = HETPDR_7_OD : N2HET[7] Pin Driven in Open-Drain Mode
6	HETPDR_6	R/W	0	N2HET[6] Pin Drive Mode 0 = HETPDR_6_PP : N2HET[6] Pin Driven in Push-Pull Mode 1 = HETPDR_6_OD : N2HET[6] Pin Driven in Open-Drain Mode
5	HETPDR_5	R/W	0	N2HET[5] Pin Drive Mode 0 = HETPDR_5_PP : N2HET[5] Pin Driven in Push-Pull Mode 1 = HETPDR_5_OD : N2HET[5] Pin Driven in Open-Drain Mode
4	HETPDR_4	R/W	0	N2HET[4] Pin Drive Mode 0 = HETPDR_4_PP : N2HET[4] Pin Driven in Push-Pull Mode 1 = HETPDR_4_OD : N2HET[4] Pin Driven in Open-Drain Mode
3	HETPDR_3	R/W	0	N2HET[3] Pin Drive Mode 0 = HETPDR_3_PP : N2HET[3] Pin Driven in Push-Pull Mode 1 = HETPDR_3_OD : N2HET[3] Pin Driven in Open-Drain Mode
2	HETPDR_2	R/W	0	N2HET[2] Pin Drive Mode 0 = HETPDR_2_PP : N2HET[2] Pin Driven in Push-Pull Mode 1 = HETPDR_2_OD : N2HET[2] Pin Driven in Open-Drain Mode
1	HETPDR_1	R/W	0	N2HET[1] Pin Drive Mode 0 = HETPDR_1_PP : N2HET[1] Pin Driven in Push-Pull Mode 1 = HETPDR_1_OD : N2HET[1] Pin Driven in Open-Drain Mode
0	HETPDR_0	R/W	0	N2HET[0] Pin Data Output 0 = HETPDR_0_PP : N2HET[0] Pin Driven in Push-Pull Mode 1 = HETPDR_0_OD : N2HET[0] Pin Driven in Open-Drain Mode

1.1.24 HETPULDIS Register

Values in this register enable or disable the pull-up/-down functionality of the pins.
N2HET1: offset = FFF7 B864h; **N2HET2:** offset = FFF7 B964h

1-24. N2HET Pull Disable Register (HETPULDIS)

31	16
HETPULDIS	
R/W-n	
15	0
HETPULDIS	
R/W-n	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; n is device dependent, see device specific data sheet

1-25. HETPULDIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETPULDIS_31	R/W	undef	N2HET[31] Pull Disable 0 = HETPULDIS_31_OFF : N2HET[31] Pin Pull Function Enabled 1 = HETPULDIS_31_ON : N2HET[31] Pin Pull Function Disabled
30	HETPULDIS_30	R/W	undef	N2HET[30] Pull Disable 0 = HETPULDIS_30_OFF : N2HET[30] Pin Pull Function Enabled 1 = HETPULDIS_30_ON : N2HET[30] Pin Pull Function Disabled
29	HETPULDIS_29	R/W	undef	N2HET[29] Pull Disable 0 = HETPULDIS_29_OFF : N2HET[29] Pin Pull Function Enabled 1 = HETPULDIS_29_ON : N2HET[29] Pin Pull Function Disabled
28	HETPULDIS_28	R/W	undef	N2HET[28] Pull Disable 0 = HETPULDIS_28_OFF : N2HET[28] Pin Pull Function Enabled 1 = HETPULDIS_28_ON : N2HET[28] Pin Pull Function Disabled
27	HETPULDIS_27	R/W	undef	N2HET[27] Pull Disable 0 = HETPULDIS_27_OFF : N2HET[27] Pin Pull Function Enabled 1 = HETPULDIS_27_ON : N2HET[27] Pin Pull Function Disabled
26	HETPULDIS_26	R/W	undef	N2HET[26] Pull Disable 0 = HETPULDIS_26_OFF : N2HET[26] Pin Pull Function Enabled 1 = HETPULDIS_26_ON : N2HET[26] Pin Pull Function Disabled
25	HETPULDIS_25	R/W	undef	N2HET[25] Pull Disable 0 = HETPULDIS_25_OFF : N2HET[25] Pin Pull Function Enabled 1 = HETPULDIS_25_ON : N2HET[25] Pin Pull Function Disabled
24	HETPULDIS_24	R/W	undef	N2HET[24] Pull Disable 0 = HETPULDIS_24_OFF : N2HET[24] Pin Pull Function Enabled 1 = HETPULDIS_24_ON : N2HET[24] Pin Pull Function Disabled
23	HETPULDIS_23	R/W	undef	N2HET[23] Pull Disable 0 = HETPULDIS_23_OFF : N2HET[23] Pin Pull Function Enabled 1 = HETPULDIS_23_ON : N2HET[23] Pin Pull Function Disabled

1-25. HETPULDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETPULDIS_22	R/W	undef	N2HET[22] Pull Disable 0 = HETPULDIS_22_OFF : N2HET[22] Pin Pull Function Enabled 1 = HETPULDIS_22_ON : N2HET[22] Pin Pull Function Disabled
21	HETPULDIS_21	R/W	undef	N2HET[21] Pull Disable 0 = HETPULDIS_21_OFF : N2HET[21] Pin Pull Function Enabled 1 = HETPULDIS_21_ON : N2HET[21] Pin Pull Function Disabled
20	HETPULDIS_20	R/W	undef	N2HET[20] Pull Disable 0 = HETPULDIS_20_OFF : N2HET[20] Pin Pull Function Enabled 1 = HETPULDIS_20_ON : N2HET[20] Pin Pull Function Disabled
19	HETPULDIS_19	R/W	undef	N2HET[19] Pull Disable 0 = HETPULDIS_19_OFF : N2HET[19] Pin Pull Function Enabled 1 = HETPULDIS_19_ON : N2HET[19] Pin Pull Function Disabled
18	HETPULDIS_18	R/W	undef	N2HET[18] Pull Disable 0 = HETPULDIS_18_OFF : N2HET[18] Pin Pull Function Enabled 1 = HETPULDIS_18_ON : N2HET[18] Pin Pull Function Disabled
17	HETPULDIS_17	R/W	undef	N2HET[17] Pull Disable 0 = HETPULDIS_17_OFF : N2HET[17] Pin Pull Function Enabled 1 = HETPULDIS_17_ON : N2HET[17] Pin Pull Function Disabled
16	HETPULDIS_16	R/W	undef	N2HET[16] Pull Disable 0 = HETPULDIS_16_OFF : N2HET[16] Pin Pull Function Enabled 1 = HETPULDIS_16_ON : N2HET[16] Pin Pull Function Disabled
15	HETPULDIS_15	R/W	undef	N2HET[15] Pull Disable 0 = HETPULDIS_15_OFF : N2HET[15] Pin Pull Function Enabled 1 = HETPULDIS_15_ON : N2HET[15] Pin Pull Function Disabled
14	HETPULDIS_14	R/W	undef	N2HET[14] Pull Disable 0 = HETPULDIS_14_OFF : N2HET[14] Pin Pull Function Enabled 1 = HETPULDIS_14_ON : N2HET[14] Pin Pull Function Disabled
13	HETPULDIS_13	R/W	undef	N2HET[13] Pull Disable 0 = HETPULDIS_13_OFF : N2HET[13] Pin Pull Function Enabled 1 = HETPULDIS_13_ON : N2HET[13] Pin Pull Function Disabled
12	HETPULDIS_12	R/W	undef	N2HET[12] Pull Disable 0 = HETPULDIS_12_OFF : N2HET[12] Pin Pull Function Enabled 1 = HETPULDIS_12_ON : N2HET[12] Pin Pull Function Disabled
11	HETPULDIS_11	R/W	undef	N2HET[11] Pull Disable 0 = HETPULDIS_11_OFF : N2HET[11] Pin Pull Function Enabled 1 = HETPULDIS_11_ON : N2HET[11] Pin Pull Function Disabled

1-25. HETPULDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETPULDIS_10	R/W	undef	N2HET[10] Pull Disable 0 = HETPULDIS_10_OFF : N2HET[10] Pin Pull Function Enabled 1 = HETPULDIS_10_ON : N2HET[10] Pin Pull Function Disabled
9	HETPULDIS_9	R/W	undef	N2HET[9] Pull Disable 0 = HETPULDIS_9_OFF : N2HET[9] Pin Pull Function Enabled 1 = HETPULDIS_9_ON : N2HET[9] Pin Pull Function Disabled
8	HETPULDIS_8	R/W	undef	N2HET[8] Pull Disable 0 = HETPULDIS_8_OFF : N2HET[8] Pin Pull Function Enabled 1 = HETPULDIS_8_ON : N2HET[8] Pin Pull Function Disabled
7	HETPULDIS_7	R/W	undef	N2HET[7] Pull Disable 0 = HETPULDIS_7_OFF : N2HET[7] Pin Pull Function Enabled 1 = HETPULDIS_7_ON : N2HET[7] Pin Pull Function Disabled
6	HETPULDIS_6	R/W	undef	N2HET[6] Pull Disable 0 = HETPULDIS_6_OFF : N2HET[6] Pin Pull Function Enabled 1 = HETPULDIS_6_ON : N2HET[6] Pin Pull Function Disabled
5	HETPULDIS_5	R/W	undef	N2HET[5] Pull Disable 0 = HETPULDIS_5_OFF : N2HET[5] Pin Pull Function Enabled 1 = HETPULDIS_5_ON : N2HET[5] Pin Pull Function Disabled
4	HETPULDIS_4	R/W	undef	N2HET[4] Pull Disable 0 = HETPULDIS_4_OFF : N2HET[4] Pin Pull Function Enabled 1 = HETPULDIS_4_ON : N2HET[4] Pin Pull Function Disabled
3	HETPULDIS_3	R/W	undef	N2HET[3] Pull Disable 0 = HETPULDIS_3_OFF : N2HET[3] Pin Pull Function Enabled 1 = HETPULDIS_3_ON : N2HET[3] Pin Pull Function Disabled
2	HETPULDIS_2	R/W	undef	N2HET[2] Pull Disable 0 = HETPULDIS_2_OFF : N2HET[2] Pin Pull Function Enabled 1 = HETPULDIS_2_ON : N2HET[2] Pin Pull Function Disabled
1	HETPULDIS_1	R/W	undef	N2HET[1] Pull Disable 0 = HETPULDIS_1_OFF : N2HET[1] Pin Pull Function Enabled 1 = HETPULDIS_1_ON : N2HET[1] Pin Pull Function Disabled
0	HETPULDIS_0	R/W	undef	N2HET[0] Pull Disable 0 = HETPULDIS_0_OFF : N2HET[0] Pin Pull Function Enabled 1 = HETPULDIS_0_ON : N2HET[0] Pin Pull Function Disabled

See device data sheet for which pins provide programmable pullups/pulldowns.

shows how the register bits of HETDIR, HETPULDIS and HETPSL are affecting the N2HET pins.

1.1.25 HETPSL Register

Values in this register select the pull-up or pull-down functionality of the pins.
N2HET1: offset = FFF7 B868h; **N2HET2:** offset = FFF7 B968h

1-25. N2HET Pull Select Register (HETPSL)

31	16
HETPSL	
R/W-0	

15	0
HETPSL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-26. HETPSL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETPSL_31	R/W	0	N2HET[31] Pull Select 0 = HETPSL_31_PD : N2HET[31] Pull Down Selected 1 = HETPSL_31_PU : N2HET[31] Pull Up Selected
30	HETPSL_30	R/W	0	N2HET[30] Pull Select 0 = HETPSL_30_PD : N2HET[30] Pull Down Selected 1 = HETPSL_30_PU : N2HET[30] Pull Up Selected
29	HETPSL_29	R/W	0	N2HET[29] Pull Select 0 = HETPSL_29_PD : N2HET[29] Pull Down Selected 1 = HETPSL_29_PU : N2HET[29] Pull Up Selected
28	HETPSL_28	R/W	0	N2HET[28] Pull Select 0 = HETPSL_28_PD : N2HET[28] Pull Down Selected 1 = HETPSL_28_PU : N2HET[28] Pull Up Selected
27	HETPSL_27	R/W	0	N2HET[27] Pull Select 0 = HETPSL_27_PD : N2HET[27] Pull Down Selected 1 = HETPSL_27_PU : N2HET[27] Pull Up Selected
26	HETPSL_26	R/W	0	N2HET[26] Pull Select 0 = HETPSL_26_PD : N2HET[26] Pull Down Selected 1 = HETPSL_26_PU : N2HET[26] Pull Up Selected
25	HETPSL_25	R/W	0	N2HET[25] Pull Select 0 = HETPSL_25_PD : N2HET[25] Pull Down Selected 1 = HETPSL_25_PU : N2HET[25] Pull Up Selected
24	HETPSL_24	R/W	0	N2HET[24] Pull Select 0 = HETPSL_24_PD : N2HET[24] Pull Down Selected 1 = HETPSL_24_PU : N2HET[24] Pull Up Selected
23	HETPSL_23	R/W	0	N2HET[23] Pull Select 0 = HETPSL_23_PD : N2HET[23] Pull Down Selected 1 = HETPSL_23_PU : N2HET[23] Pull Up Selected

1-26. HETPSL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETPSL_22	R/W	0	N2HET[22] Pull Select 0 = HETPSL_22_PD : N2HET[22] Pull Down Selected 1 = HETPSL_22_PU : N2HET[22] Pull Up Selected
21	HETPSL_21	R/W	0	N2HET[21] Pull Select 0 = HETPSL_21_PD : N2HET[21] Pull Down Selected 1 = HETPSL_21_PU : N2HET[21] Pull Up Selected
20	HETPSL_20	R/W	0	N2HET[20] Pull Select 0 = HETPSL_20_PD : N2HET[20] Pull Down Selected 1 = HETPSL_20_PU : N2HET[20] Pull Up Selected
19	HETPSL_19	R/W	0	N2HET[19] Pull Select 0 = HETPSL_19_PD : N2HET[19] Pull Down Selected 1 = HETPSL_19_PU : N2HET[19] Pull Up Selected
18	HETPSL_18	R/W	0	N2HET[18] Pull Select 0 = HETPSL_18_PD : N2HET[18] Pull Down Selected 1 = HETPSL_18_PU : N2HET[18] Pull Up Selected
17	HETPSL_17	R/W	0	N2HET[17] Pull Select 0 = HETPSL_17_PD : N2HET[17] Pull Down Selected 1 = HETPSL_17_PU : N2HET[17] Pull Up Selected
16	HETPSL_16	R/W	0	N2HET[16] Pull Select 0 = HETPSL_16_PD : N2HET[16] Pull Down Selected 1 = HETPSL_16_PU : N2HET[16] Pull Up Selected
15	HETPSL_15	R/W	0	N2HET[15] Pull Select 0 = HETPSL_15_PD : N2HET[15] Pull Down Selected 1 = HETPSL_15_PU : N2HET[15] Pull Up Selected
14	HETPSL_14	R/W	0	N2HET[14] Pull Select 0 = HETPSL_14_PD : N2HET[14] Pull Down Selected 1 = HETPSL_14_PU : N2HET[14] Pull Up Selected
13	HETPSL_13	R/W	0	N2HET[13] Pull Select 0 = HETPSL_13_PD : N2HET[13] Pull Down Selected 1 = HETPSL_13_PU : N2HET[13] Pull Up Selected
12	HETPSL_12	R/W	0	N2HET[12] Pull Select 0 = HETPSL_12_PD : N2HET[12] Pull Down Selected 1 = HETPSL_12_PU : N2HET[12] Pull Up Selected
11	HETPSL_11	R/W	0	N2HET[11] Pull Select 0 = HETPSL_11_PD : N2HET[11] Pull Down Selected 1 = HETPSL_11_PU : N2HET[11] Pull Up Selected

1-26. HETPSL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETPSL_10	R/W	0	N2HET[10] Pull Select 0 = HETPSL_10_PD : N2HET[10] Pull Down Selected 1 = HETPSL_10_PU : N2HET[10] Pull Up Selected
9	HETPSL_9	R/W	0	N2HET[9] Pull Select 0 = HETPSL_9_PD : N2HET[9] Pull Down Selected 1 = HETPSL_9_PU : N2HET[9] Pull Up Selected
8	HETPSL_8	R/W	0	N2HET[8] Pull Select 0 = HETPSL_8_PD : N2HET[8] Pull Down Selected 1 = HETPSL_8_PU : N2HET[8] Pull Up Selected
7	HETPSL_7	R/W	0	N2HET[7] Pull Select 0 = HETPSL_7_PD : N2HET[7] Pull Down Selected 1 = HETPSL_7_PU : N2HET[7] Pull Up Selected
6	HETPSL_6	R/W	0	N2HET[6] Pull Select 0 = HETPSL_6_PD : N2HET[6] Pull Down Selected 1 = HETPSL_6_PU : N2HET[6] Pull Up Selected
5	HETPSL_5	R/W	0	N2HET[5] Pull Select 0 = HETPSL_5_PD : N2HET[5] Pull Down Selected 1 = HETPSL_5_PU : N2HET[5] Pull Up Selected
4	HETPSL_4	R/W	0	N2HET[4] Pull Select 0 = HETPSL_4_PD : N2HET[4] Pull Down Selected 1 = HETPSL_4_PU : N2HET[4] Pull Up Selected
3	HETPSL_3	R/W	0	N2HET[3] Pull Select 0 = HETPSL_3_PD : N2HET[3] Pull Down Selected 1 = HETPSL_3_PU : N2HET[3] Pull Up Selected
2	HETPSL_2	R/W	0	N2HET[2] Pull Select 0 = HETPSL_2_PD : N2HET[2] Pull Down Selected 1 = HETPSL_2_PU : N2HET[2] Pull Up Selected
1	HETPSL_1	R/W	0	N2HET[1] Pull Select 0 = HETPSL_1_PD : N2HET[1] Pull Down Selected 1 = HETPSL_1_PU : N2HET[1] Pull Up Selected
0	HETPSL_0	R/W	0	N2HET[0] Pull Select 0 = HETPSL_0_PD : N2HET[0] Pull Down Selected 1 = HETPSL_0_PU : N2HET[0] Pull Up Selected

See device data sheet for which pins provide programmable pullups/pulldowns.

shows how the register bits of HETDIR, HETPULDIS and HETPSL are affecting the N2HET pins.

The information of this register is also used to define the pin states after a parity error:

After a parity error all N2HET pins, which are

1. Defined as output pins in the HETDIR register
2. Not defined as open drain pins (with the HETPDR register)
3. Selected with the HETPPR register, will remain outputs, but automatically change their levels in the following way:
   - If the HETPSL register specifies 0 for the pin, it will switch to low level.
   - If the HETPSL register specifies 1 for the pin, it will switch to high level.

This behavior is independent of the value, which register HETPULDIS specifies for the corresponding pin.

1.1.26 HETPCR Register

N2HET1: offset = FFF7 B874h; **N2HET2:** offset = FFF7 B974h

1-26. Parity Control Register (HETPCR)

31								16
Reserved								
R-0								
15		9	8	7		4	3	0
Reserved			TEST	Reserved			PARITY_ENA	
R-0			R/WP-0	R-0			R/WP-5h	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

1-27. HETPCR Register Field Descriptions

Bit	Field	Type	Reset	Description
9-31	Reserved	R	0	Read returns 0. Writes have no effect.
8	TEST	R/WP	0	Test Bit. When this bit is set, the parity bits are mapped into the peripheral RAM frame to make them accessible by the CPU. - Write in privilege mode only. 0 = TEST_DIS : Parity bits are not memory mapped. 1 = TEST_ENA : Parity bits are memory mapped for test purposes.
4-7	Reserved	R	0	Read returns 0. Writes have no effect.
0-3	PARITY_ENA	R/WP	0x5	Enable/disable parity checking. This bit field enables or disables the parity check on read operations and the parity calculation on write operations. If parity checking is enabled and a parity error is detected the N2HET_UERR signal is activated. Note that 0xA is the recommended value to use but any value other than 0x5 enables parity checking. 0x5 = PARITY_DIS : Parity check is disabled. 0xA = PARITY_ENA : Parity check is enabled.

1.1.27 HETPAR Register

In case of a N2HET RAM parity error, PAOFF will contain the offset address of the erroneous 32-bit N2HET RAM field counted from the beginning of the N2HET RAM. Examples: The 32-bit program field of instruction 0 will return 0, the 32-bit control field of instruction 0 will return 1, ..., the 32-bit control field of instruction 1 will return 5, and so on.

1-27. Parity Address Register (HETPAR)

31	16
Reserved	
R-0	

15	13	14	2	1	0
Reserved		PAOFF		Reserved	
R-0		R-X		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; X = Value unchanged after reset

1-28. HETPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
13-31	Reserved	R	0	Read returns 0. Writes have no effect.
2-12	PAOFF	R	X	Parity Error Address Offset. This register holds the offset address of the first parity error, which is detected in N2HET RAM. This error address is frozen from being updated until it is read by the CPU. During emulation mode, this address is frozen even when read. The Parity Error Address Register will not be reset, neither by PORRST nor by any other reset source.
0-1	Reserved	R	0	Read returns 0. Writes have no effect.

1.1.28 HETPPR Register

N2HET1: offset = FFF7 B87Ch; **N2HET2:** offset = FFF7 B97Ch

1-28. Parity Pin Register (HETPPR)

31	16
HETPPR	
R/W-0	

15	0
HETPPR	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-29. HETPPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETPPR_31	R/W	0	N2HET[31] Parity Protect 0 = HETPPR_31_DIS : N2HET[31] is not affected by an N2HET parity error. 1 = HETPPR_31_ENA : N2HET[31] is driven to a known state by an N2HET parity error
30	HETPPR_30	R/W	0	N2HET[30] Parity Protect 0 = HETPPR_30_DIS : N2HET[30] is not affected by an N2HET parity error. 1 = HETPPR_30_ENA : N2HET[30] is driven to a known state by an N2HET parity error
29	HETPPR_29	R/W	0	N2HET[29] Parity Protect 0 = HETPPR_29_DIS : N2HET[29] is not affected by an N2HET parity error. 1 = HETPPR_29_ENA : N2HET[29] is driven to a known state by an N2HET parity error
28	HETPPR_28	R/W	0	N2HET[28] Parity Protect 0 = HETPPR_28_DIS : N2HET[28] is not affected by an N2HET parity error. 1 = HETPPR_28_ENA : N2HET[28] is driven to a known state by an N2HET parity error
27	HETPPR_27	R/W	0	N2HET[27] Parity Protect 0 = HETPPR_27_DIS : N2HET[27] is not affected by an N2HET parity error. 1 = HETPPR_27_ENA : N2HET[27] is driven to a known state by an N2HET parity error
26	HETPPR_26	R/W	0	N2HET[26] Parity Protect 0 = HETPPR_26_DIS : N2HET[26] is not affected by an N2HET parity error. 1 = HETPPR_26_ENA : N2HET[26] is driven to a known state by an N2HET parity error
25	HETPPR_25	R/W	0	N2HET[25] Parity Protect 0 = HETPPR_25_DIS : N2HET[25] is not affected by an N2HET parity error. 1 = HETPPR_25_ENA : N2HET[25] is driven to a known state by an N2HET parity error
24	HETPPR_24	R/W	0	N2HET[24] Parity Protect 0 = HETPPR_24_DIS : N2HET[24] is not affected by an N2HET parity error. 1 = HETPPR_24_ENA : N2HET[24] is driven to a known state by an N2HET parity error

1-29. HETPPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	HETPPR_23	R/W	0	N2HET[23] Parity Protect 0 = HETPPR_23_DIS : N2HET[23] is not affected by an N2HET parity error. 1 = HETPPR_23_ENA : N2HET[23] is driven to a known state by an N2HET parity error
22	HETPPR_22	R/W	0	N2HET[22] Parity Protect 0 = HETPPR_22_DIS : N2HET[22] is not affected by an N2HET parity error. 1 = HETPPR_22_ENA : N2HET[22] is driven to a known state by an N2HET parity error
21	HETPPR_21	R/W	0	N2HET[21] Parity Protect 0 = HETPPR_21_DIS : N2HET[21] is not affected by an N2HET parity error. 1 = HETPPR_21_ENA : N2HET[21] is driven to a known state by an N2HET parity error
20	HETPPR_20	R/W	0	N2HET[20] Parity Protect 0 = HETPPR_20_DIS : N2HET[20] is not affected by an N2HET parity error. 1 = HETPPR_20_ENA : N2HET[20] is driven to a known state by an N2HET parity error
19	HETPPR_19	R/W	0	N2HET[19] Parity Protect 0 = HETPPR_19_DIS : N2HET[19] is not affected by an N2HET parity error. 1 = HETPPR_19_ENA : N2HET[19] is driven to a known state by an N2HET parity error
18	HETPPR_18	R/W	0	N2HET[18] Parity Protect 0 = HETPPR_18_DIS : N2HET[18] is not affected by an N2HET parity error. 1 = HETPPR_18_ENA : N2HET[18] is driven to a known state by an N2HET parity error
17	HETPPR_17	R/W	0	N2HET[17] Parity Protect 0 = HETPPR_17_DIS : N2HET[17] is not affected by an N2HET parity error. 1 = HETPPR_17_ENA : N2HET[17] is driven to a known state by an N2HET parity error
16	HETPPR_16	R/W	0	N2HET[16] Parity Protect 0 = HETPPR_16_DIS : N2HET[16] is not affected by an N2HET parity error. 1 = HETPPR_16_ENA : N2HET[16] is driven to a known state by an N2HET parity error
15	HETPPR_15	R/W	0	N2HET[15] Parity Protect 0 = HETPPR_15_DIS : N2HET[15] is not affected by an N2HET parity error. 1 = HETPPR_15_ENA : N2HET[15] is driven to a known state by an N2HET parity error
14	HETPPR_14	R/W	0	N2HET[14] Parity Protect 0 = HETPPR_14_DIS : N2HET[14] is not affected by an N2HET parity error. 1 = HETPPR_14_ENA : N2HET[14] is driven to a known state by an N2HET parity error

1-29. HETPPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	HETPPR_13	R/W	0	N2HET[13] Parity Protect 0 = HETPPR_13_DIS : N2HET[13] is not affected by an N2HET parity error. 1 = HETPPR_13_ENA : N2HET[13] is driven to a known state by an N2HET parity error
12	HETPPR_12	R/W	0	N2HET[12] Parity Protect 0 = HETPPR_12_DIS : N2HET[12] is not affected by an N2HET parity error. 1 = HETPPR_12_ENA : N2HET[12] is driven to a known state by an N2HET parity error
11	HETPPR_11	R/W	0	N2HET[11] Parity Protect 0 = HETPPR_11_DIS : N2HET[11] is not affected by an N2HET parity error. 1 = HETPPR_11_ENA : N2HET[11] is driven to a known state by an N2HET parity error
10	HETPPR_10	R/W	0	N2HET[10] Parity Protect 0 = HETPPR_10_DIS : N2HET[10] is not affected by an N2HET parity error. 1 = HETPPR_10_ENA : N2HET[10] is driven to a known state by an N2HET parity error
9	HETPPR_9	R/W	0	N2HET[9] Parity Protect 0 = HETPPR_9_DIS : N2HET[9] is not affected by an N2HET parity error. 1 = HETPPR_9_ENA : N2HET[9] is driven to a known state by an N2HET parity error
8	HETPPR_8	R/W	0	N2HET[8] Parity Protect 0 = HETPPR_8_DIS : N2HET[8] is not affected by an N2HET parity error. 1 = HETPPR_8_ENA : N2HET[8] is driven to a known state by an N2HET parity error
7	HETPPR_7	R/W	0	N2HET[7] Parity Protect 0 = HETPPR_7_DIS : N2HET[7] is not affected by an N2HET parity error. 1 = HETPPR_7_ENA : N2HET[7] is driven to a known state by an N2HET parity error
6	HETPPR_6	R/W	0	N2HET[6] Parity Protect 0 = HETPPR_6_DIS : N2HET[6] is not affected by an N2HET parity error. 1 = HETPPR_6_ENA : N2HET[6] is driven to a known state by an N2HET parity error
5	HETPPR_5	R/W	0	N2HET[5] Parity Protect 0 = HETPPR_5_DIS : N2HET[5] is not affected by an N2HET parity error. 1 = HETPPR_5_ENA : N2HET[5] is driven to a known state by an N2HET parity error
4	HETPPR_4	R/W	0	N2HET[4] Parity Protect 0 = HETPPR_4_DIS : N2HET[4] is not affected by an N2HET parity error. 1 = HETPPR_4_ENA : N2HET[4] is driven to a known state by an N2HET parity error

1-29. HETPPR Register Field Descriptions (continued)

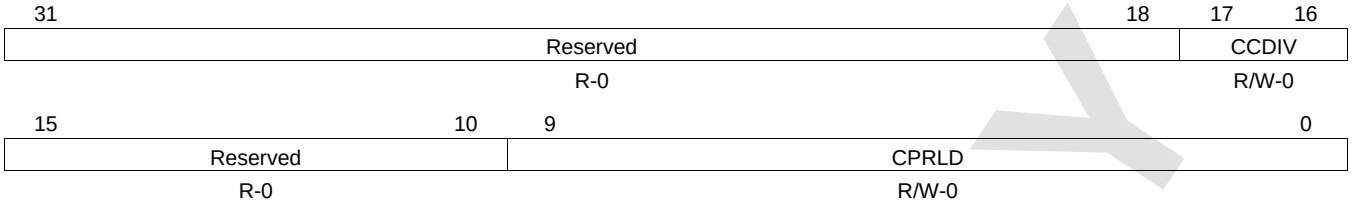
Bit	Field	Type	Reset	Description
3	HETPPR_3	R/W	0	N2HET[3] Parity Protect 0 = HETPPR_3_DIS : N2HET[3] is not affected by an N2HET parity error. 1 = HETPPR_3_ENA : N2HET[3] is driven to a known state by an N2HET parity error
2	HETPPR_2	R/W	0	N2HET[2] Parity Protect 0 = HETPPR_2_DIS : N2HET[2] is not affected by an N2HET parity error. 1 = HETPPR_2_ENA : N2HET[2] is driven to a known state by an N2HET parity error
1	HETPPR_1	R/W	0	N2HET[1] Parity Protect 0 = HETPPR_1_DIS : N2HET[1] is not affected by an N2HET parity error. 1 = HETPPR_1_ENA : N2HET[1] is driven to a known state by an N2HET parity error
0	HETPPR_0	R/W	0	N2HET[0] Parity Protect 0 = HETPPR_0_DIS : N2HET[0] is not affected by an N2HET parity error. 1 = HETPPR_0_ENA : N2HET[0] is driven to a known state by an N2HET parity error

1-30. Known State on Parity Error

HETDIR[n]	HETPDR[n]	HETPSL[n]	Known State on Parity Error
0	x	x	High Impedance
1	0	0	Drive Logic 0
1	0	1	Drive Logic 1
1	1	x	High Impedance

1.1.29 HETSFPRLD Register

1-29. Suppression Filter Preload Register (HETSFPRLD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-31. HETSFPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
18-31	Reserved	R	0	Read returns 0. Writes have no effect.
16-17	CCDIV	R/W	0	Counter Clock Divider: CCDIV determines the ratio between the counter clock and VCLK2. 0 = CCDIV_BY_1 : CCLK = VCLK2 1 = CCDIV_BY_2 : CCLK = VCLK2 / 2 2 = CCDIV_BY_3 : CCLK = VCLK2 / 3 3 = CCDIV_BY_4 : CCLK = VCLK2 / 4
10-15	Reserved	R	0	Read returns 0. Writes have no effect.
0-9	CPRLD	R/W	0	Counter Preload Value: CPRLD contains the preload value for the counter clock.

1.1.30 HETSFENA Register

N2HET1: offset = FFF7 B884h; **N2HET2:** offset = FFF7 B984h

1-30. Suppression Filter Enable Register (HETSFENA)

31	16
HETSFENA	
R/W-0	

15	0
HETSFENA	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-32. HETSFENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETSFENA_31	R/W	0	N2HET[31] Suppression Filter Enable 0 = HETSFENA_31_DIS : N2HET[31] filter is disabled. 1 = HETSFENA_31_ENA : N2HET[31] filter is enabled.
30	HETSFENA_30	R/W	0	N2HET[30] Suppression Filter Enable 0 = HETSFENA_30_DIS : N2HET[30] filter is disabled. 1 = HETSFENA_30_ENA : N2HET[30] filter is enabled.
29	HETSFENA_29	R/W	0	N2HET[29] Suppression Filter Enable 0 = HETSFENA_29_DIS : N2HET[29] filter is disabled. 1 = HETSFENA_29_ENA : N2HET[29] filter is enabled.
28	HETSFENA_28	R/W	0	N2HET[28] Suppression Filter Enable 0 = HETSFENA_28_DIS : N2HET[28] filter is disabled. 1 = HETSFENA_28_ENA : N2HET[28] filter is enabled.
27	HETSFENA_27	R/W	0	N2HET[27] Suppression Filter Enable 0 = HETSFENA_27_DIS : N2HET[27] filter is disabled. 1 = HETSFENA_27_ENA : N2HET[27] filter is enabled.
26	HETSFENA_26	R/W	0	N2HET[26] Suppression Filter Enable 0 = HETSFENA_26_DIS : N2HET[26] filter is disabled. 1 = HETSFENA_26_ENA : N2HET[26] filter is enabled.
25	HETSFENA_25	R/W	0	N2HET[25] Suppression Filter Enable 0 = HETSFENA_25_DIS : N2HET[25] filter is disabled. 1 = HETSFENA_25_ENA : N2HET[25] filter is enabled.
24	HETSFENA_24	R/W	0	N2HET[24] Suppression Filter Enable 0 = HETSFENA_24_DIS : N2HET[24] filter is disabled. 1 = HETSFENA_24_ENA : N2HET[24] filter is enabled.
23	HETSFENA_23	R/W	0	N2HET[23] Suppression Filter Enable 0 = HETSFENA_23_DIS : N2HET[23] filter is disabled. 1 = HETSFENA_23_ENA : N2HET[23] filter is enabled.

1-32. HETSFENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETSFENA_22	R/W	0	N2HET[22] Suppression Filter Enable 0 = HETSFENA_22_DIS : N2HET[22] filter is disabled. 1 = HETSFENA_22_ENA : N2HET[22] filter is enabled.
21	HETSFENA_21	R/W	0	N2HET[21] Suppression Filter Enable 0 = HETSFENA_21_DIS : N2HET[21] filter is disabled. 1 = HETSFENA_21_ENA : N2HET[21] filter is enabled.
20	HETSFENA_20	R/W	0	N2HET[20] Suppression Filter Enable 0 = HETSFENA_20_DIS : N2HET[20] filter is disabled. 1 = HETSFENA_20_ENA : N2HET[20] filter is enabled.
19	HETSFENA_19	R/W	0	N2HET[19] Suppression Filter Enable 0 = HETSFENA_19_DIS : N2HET[19] filter is disabled. 1 = HETSFENA_19_ENA : N2HET[19] filter is enabled.
18	HETSFENA_18	R/W	0	N2HET[18] Suppression Filter Enable 0 = HETSFENA_18_DIS : N2HET[18] filter is disabled. 1 = HETSFENA_18_ENA : N2HET[18] filter is enabled.
17	HETSFENA_17	R/W	0	N2HET[17] Suppression Filter Enable 0 = HETSFENA_17_DIS : N2HET[17] filter is disabled. 1 = HETSFENA_17_ENA : N2HET[17] filter is enabled.
16	HETSFENA_16	R/W	0	N2HET[16] Suppression Filter Enable 0 = HETSFENA_16_DIS : N2HET[16] filter is disabled. 1 = HETSFENA_16_ENA : N2HET[16] filter is enabled.
15	HETSFENA_15	R/W	0	N2HET[15] Suppression Filter Enable 0 = HETSFENA_15_DIS : N2HET[15] filter is disabled. 1 = HETSFENA_15_ENA : N2HET[15] filter is enabled.
14	HETSFENA_14	R/W	0	N2HET[14] Suppression Filter Enable 0 = HETSFENA_14_DIS : N2HET[14] filter is disabled. 1 = HETSFENA_14_ENA : N2HET[14] filter is enabled.
13	HETSFENA_13	R/W	0	N2HET[13] Suppression Filter Enable 0 = HETSFENA_13_DIS : N2HET[13] filter is disabled. 1 = HETSFENA_13_ENA : N2HET[13] filter is enabled.
12	HETSFENA_12	R/W	0	N2HET[12] Suppression Filter Enable 0 = HETSFENA_12_DIS : N2HET[12] filter is disabled. 1 = HETSFENA_12_ENA : N2HET[12] filter is enabled.
11	HETSFENA_11	R/W	0	N2HET[11] Suppression Filter Enable 0 = HETSFENA_11_DIS : N2HET[11] filter is disabled. 1 = HETSFENA_11_ENA : N2HET[11] filter is enabled.

1-32. HETSFENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETSFENA_10	R/W	0	N2HET[10] Suppression Filter Enable 0 = HETSFENA_10_DIS : N2HET[10] filter is disabled. 1 = HETSFENA_10_ENA : N2HET[10] filter is enabled.
9	HETSFENA_9	R/W	0	N2HET[9] Suppression Filter Enable 0 = HETSFENA_9_DIS : N2HET[9] filter is disabled. 1 = HETSFENA_9_ENA : N2HET[9] filter is enabled.
8	HETSFENA_8	R/W	0	N2HET[8] Suppression Filter Enable 0 = HETSFENA_8_DIS : N2HET[8] filter is disabled. 1 = HETSFENA_8_ENA : N2HET[8] filter is enabled.
7	HETSFENA_7	R/W	0	N2HET[7] Suppression Filter Enable 0 = HETSFENA_7_DIS : N2HET[7] filter is disabled. 1 = HETSFENA_7_ENA : N2HET[7] filter is enabled.
6	HETSFENA_6	R/W	0	N2HET[6] Suppression Filter Enable 0 = HETSFENA_6_DIS : N2HET[6] filter is disabled. 1 = HETSFENA_6_ENA : N2HET[6] filter is enabled.
5	HETSFENA_5	R/W	0	N2HET[5] Suppression Filter Enable 0 = HETSFENA_5_DIS : N2HET[5] filter is disabled. 1 = HETSFENA_5_ENA : N2HET[5] filter is enabled.
4	HETSFENA_4	R/W	0	N2HET[4] Suppression Filter Enable 0 = HETSFENA_4_DIS : N2HET[4] filter is disabled. 1 = HETSFENA_4_ENA : N2HET[4] filter is enabled.
3	HETSFENA_3	R/W	0	N2HET[3] Suppression Filter Enable 0 = HETSFENA_3_DIS : N2HET[3] filter is disabled. 1 = HETSFENA_3_ENA : N2HET[3] filter is enabled.
2	HETSFENA_2	R/W	0	N2HET[2] Suppression Filter Enable 0 = HETSFENA_2_DIS : N2HET[2] filter is disabled. 1 = HETSFENA_2_ENA : N2HET[2] filter is enabled.
1	HETSFENA_1	R/W	0	N2HET[1] Suppression Filter Enable 0 = HETSFENA_1_DIS : N2HET[1] filter is disabled. 1 = HETSFENA_1_ENA : N2HET[1] filter is enabled.
0	HETSFENA_0	R/W	0	N2HET[0] Suppression Filter Enable 0 = HETSFENA_0_DIS : N2HET[0] filter is disabled. 1 = HETSFENA_0_ENA : N2HET[0] filter is enabled.

1.1.31 HETLBPSEL Register

These bit fields are valid only when IODFT mode is enabled (HETLBPDIR[19:16] = "1010"). If bit x is set, the HR structures on pins HET[n+1] and HET[n] are connected in a loop back mode. The direction is given by LBPDIR n+1/n and type is selected by LBPTYPE n+1/n. The pin which is not driven by the N2HET pin actions can still be used as normal GIO pin.

1-31. Loop Back Pair Select Register (HETLBPSEL)

31	30	29	28	27	26	25	24
LBPTYPE31/30	LBPTYPE29/28	LBPTYPE27/26	LBPTYPE25/24	LBPTYPE23/22	LBPTYPE21/20	LBPTYPE19/18	LBPTYPE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
LBPTYPE15/14	LBPTYPE13/12	LBPTYPE11/10	LBPTYPE9/8	LBPTYPE7/6	LBPTYPE5/4	LBPTYPE3/2	LBPTYPE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
LBPSEL 31/30	LBPSEL 29/28	LBPSEL 27/26	LBPSEL 25/24	LBPSEL 23/22	LBPSEL 21/20	LBPSEL 19/18	LBPSEL 17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
LBPSEL 15/14	LBPSEL 13/12	LBPSEL 11/10	LBPSEL 9/8	LBPSEL 7/6	LBPSEL 5/4	LBPSEL 3/2	LBPSEL 1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-33. HETLBPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LBPTYPE_31_30	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[31] and N2HET[30]: 0 = LBPTYPE_31_30_DIG : Digital Loopback Selected 1 = LBPTYPE_31_30_ANA : Analog Loopback Selected
30	LBPTYPE_29_28	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[29] and N2HET[28]: 0 = LBPTYPE_29_28_DIG : Digital Loopback Selected 1 = LBPTYPE_29_28_ANA : Analog Loopback Selected
29	LBPTYPE_27_26	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[27] and N2HET[26]: 0 = LBPTYPE_27_26_DIG : Digital Loopback Selected 1 = LBPTYPE_27_26_ANA : Analog Loopback Selected
28	LBPTYPE_25_24	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[25] and N2HET[24]: 0 = LBPTYPE_25_24_DIG : Digital Loopback Selected 1 = LBPTYPE_25_24_ANA : Analog Loopback Selected
27	LBPTYPE_23_22	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[23] and N2HET[22]: 0 = LBPTYPE_23_22_DIG : Digital Loopback Selected 1 = LBPTYPE_23_22_ANA : Analog Loopback Selected
26	LBPTYPE_21_20	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[21] and N2HET[20]: 0 = LBPTYPE_21_20_DIG : Digital Loopback Selected 1 = LBPTYPE_21_20_ANA : Analog Loopback Selected
25	LBPTYPE_19_18	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[19] and N2HET[18]: 0 = LBPTYPE_19_18_DIG : Digital Loopback Selected 1 = LBPTYPE_19_18_ANA : Analog Loopback Selected

1-33. HETLBPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	LBPTYPE_17_16	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[17] and N2HET[16]: 0 = LBPTYPE_17_16_DIG : Digital Loopback Selected 1 = LBPTYPE_17_16_ANA : Analog Loopback Selected
23	LBPTYPE_15_14	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[15] and N2HET[14]: 0 = LBPTYPE_15_14_DIG : Digital Loopback Selected 1 = LBPTYPE_15_14_ANA : Analog Loopback Selected
22	LBPTYPE_13_12	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[13] and N2HET[12]: 0 = LBPTYPE_13_12_DIG : Digital Loopback Selected 1 = LBPTYPE_13_12_ANA : Analog Loopback Selected
21	LBPTYPE_11_10	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[11] and N2HET[10]: 0 = LBPTYPE_11_10_DIG : Digital Loopback Selected 1 = LBPTYPE_11_10_ANA : Analog Loopback Selected
20	LBPTYPE_9_8	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[9] and N2HET[8]: 0 = LBPTYPE_9_8_DIG : Digital Loopback Selected 1 = LBPTYPE_9_8_ANA : Analog Loopback Selected
19	LBPTYPE_7_6	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[7] and N2HET[6]: 0 = LBPTYPE_7_6_DIG : Digital Loopback Selected 1 = LBPTYPE_7_6_ANA : Analog Loopback Selected
18	LBPTYPE_5_4	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[5] and N2HET[4]: 0 = LBPTYPE_5_4_DIG : Digital Loopback Selected 1 = LBPTYPE_5_4_ANA : Analog Loopback Selected
17	LBPTYPE_3_2	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[3] and N2HET[2]: 0 = LBPTYPE_3_2_DIG : Digital Loopback Selected 1 = LBPTYPE_3_2_ANA : Analog Loopback Selected
16	LBPTYPE_1_0	R/W	0	Loop Back Pair Type Select Bits for pins N2HET[1] and N2HET[0]: 0 = LBPTYPE_1_0_DIG : Digital Loopback Selected 1 = LBPTYPE_1_0_ANA : Analog Loopback Selected
15	LBPSEL_31_30	R/W	0	Loop Back Pair Select Bits for pins N2HET[31] and N2HET[30]: 0 = LBPSEL_31_30_DIS : Loopback Disabled 1 = LBPSEL_31_30_ENA : Loopback Enabled
14	LBPSEL_29_28	R/W	0	Loop Back Pair Select Bits for pins N2HET[29] and N2HET[28]: 0 = LBPSEL_29_28_DIS : Loopback Disabled 1 = LBPSEL_29_28_ENA : Loopback Enabled
13	LBPSEL_27_26	R/W	0	Loop Back Pair Select Bits for pins N2HET[27] and N2HET[26]: 0 = LBPSEL_27_26_DIS : Loopback Disabled 1 = LBPSEL_27_26_ENA : Loopback Enabled

1-33. HETLBPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	LBPSEL_25_24	R/W	0	Loop Back Pair Select Bits for pins N2HET[25] and N2HET[24]: 0 = LBPSEL_25_24_DIS : Loopback Disabled 1 = LBPSEL_25_24_ENA : Loopback Enabled
11	LBPSEL_23_22	R/W	0	Loop Back Pair Select Bits for pins N2HET[23] and N2HET[22]: 0 = LBPSEL_23_22_DIS : Loopback Disabled 1 = LBPSEL_23_22_ENA : Loopback Enabled
10	LBPSEL_21_20	R/W	0	Loop Back Pair Select Bits for pins N2HET[21] and N2HET[20]: 0 = LBPSEL_21_20_DIS : Loopback Disabled 1 = LBPSEL_21_20_ENA : Loopback Enabled
9	LBPSEL_19_18	R/W	0	Loop Back Pair Select Bits for pins N2HET[19] and N2HET[18]: 0 = LBPSEL_19_18_DIS : Loopback Disabled 1 = LBPSEL_19_18_ENA : Loopback Enabled
8	LBPSEL_17_16	R/W	0	Loop Back Pair Select Bits for pins N2HET[17] and N2HET[16]: 0 = LBPSEL_17_16_DIS : Loopback Disabled 1 = LBPSEL_17_16_ENA : Loopback Enabled
7	LBPSEL_15_14	R/W	0	Loop Back Pair Select Bits for pins N2HET[15] and N2HET[14]: 0 = LBPSEL_15_14_DIS : Loopback Disabled 1 = LBPSEL_15_14_ENA : Loopback Enabled
6	LBPSEL_13_12	R/W	0	Loop Back Pair Select Bits for pins N2HET[13] and N2HET[12]: 0 = LBPSEL_13_12_DIS : Loopback Disabled 1 = LBPSEL_13_12_ENA : Loopback Enabled
5	LBPSEL_11_10	R/W	0	Loop Back Pair Select Bits for pins N2HET[11] and N2HET[10]: 0 = LBPSEL_11_10_DIS : Loopback Disabled 1 = LBPSEL_11_10_ENA : Loopback Enabled
4	LBPSEL_9_8	R/W	0	Loop Back Pair Select Bits for pins N2HET[9] and N2HET[8]: 0 = LBPSEL_9_8_DIS : Loopback Disabled 1 = LBPSEL_9_8_ENA : Loopback Enabled
3	LBPSEL_7_6	R/W	0	Loop Back Pair Select Bits for pins N2HET[7] and N2HET[6]: 0 = LBPSEL_7_6_DIS : Loopback Disabled 1 = LBPSEL_7_6_ENA : Loopback Enabled
2	LBPSEL_5_4	R/W	0	Loop Back Pair Select Bits for pins N2HET[5] and N2HET[4]: 0 = LBPSEL_5_4_DIS : Loopback Disabled 1 = LBPSEL_5_4_ENA : Loopback Enabled
1	LBPSEL_3_2	R/W	0	Loop Back Pair Select Bits for pins N2HET[3] and N2HET[2]: 0 = LBPSEL_3_2_DIS : Loopback Disabled 1 = LBPSEL_3_2_ENA : Loopback Enabled

1-33. HETLBPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LBPSEL_1_0	R/W	0	Loop Back Pair Select Bits for pins N2HET[1] and N2HET[0]: 0 = LBPSEL_1_0_DIS : Loopback Disabled 1 = LBPSEL_1_0_ENA : Loopback Enabled

1.1.32 HETLBPDIR Register

N2HET1: offset = FFF7 B890h; **N2HET2:** offset = FFF7 B990h

1-32. Loop Back Pair Direction Register (HETLBPDIR)

31						20	19			16
Reserved							IODFTENA			
R-0							R/WP-5h			
15	14	13	12	11	10		9			8
LBPDIR 31/30	LBPDIR 29/28	LBPDIR 27/26	LBPDIR 25/24	LBPDIR 23/22	LBPDIR 21/20		LBPDIR 19/18			LBPDIR 17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0			R/W-0
7	6	5	4	3	2		1			0
LBPDIR 15/14	LBPDIR 13/12	LBPDIR 11/10	LBPDIR 9/8	LBPDIR 7/6	LBPDIR 5/4		LBPDIR 3/2			LBPDIR 1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

1-34. HETLBPDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
20-31	Reserved	R	0	Read returns 0. Writes have no effect.
16-19	IODFTENA	R/WP	0x5	Module IODFT Enable Key. Note that 0x0A is recommended but any value other than 0x5 disables IODFT. - Write in Privilege Mode Only 0x5 = IODFTENA_ON: I/O DFT is enabled. 0xA = IODFTENA_OFF: I/O DFT is disabled
15	LBPDIR_31_30	R/W	0	Loop Back Pair Select Bits for pins N2HET[31] and N2HET[30]: 0 = LBPDIR_31_30_ODD : Pin N2HET[31] is output and N2HET[30] is input 1 = LBPDIR_31_30_EVEN : Pin N2HET[30] is output and N2HET[31] is input
14	LBPDIR_29_28	R/W	0	Loop Back Pair Select Bits for pins N2HET[29] and N2HET[28]: 0 = LBPDIR_29_28_ODD : Pin N2HET[29] is output and N2HET[28] is input 1 = LBPDIR_29_28_EVEN : Pin N2HET[28] is output and N2HET[29] is input
13	LBPDIR_27_26	R/W	0	Loop Back Pair Select Bits for pins N2HET[27] and N2HET[26]: 0 = LBPDIR_27_26_ODD : Pin N2HET[27] is output and N2HET[26] is input 1 = LBPDIR_27_26_EVEN : Pin N2HET[26] is output and N2HET[27] is input
12	LBPDIR_25_24	R/W	0	Loop Back Pair Select Bits for pins N2HET[25] and N2HET[24]: 0 = LBPDIR_25_24_ODD : Pin N2HET[25] is output and N2HET[24] is input 1 = LBPDIR_25_24_EVEN : Pin N2HET[24] is output and N2HET[25] is input
11	LBPDIR_23_22	R/W	0	Loop Back Pair Select Bits for pins N2HET[23] and N2HET[22]: 0 = LBPDIR_23_22_ODD : Pin N2HET[23] is output and N2HET[22] is input 1 = LBPDIR_23_22_EVEN : Pin N2HET[22] is output and N2HET[23] is input
10	LBPDIR_21_20	R/W	0	Loop Back Pair Select Bits for pins N2HET[21] and N2HET[20]: 0 = LBPDIR_21_20_ODD : Pin N2HET[21] is output and N2HET[20] is input 1 = LBPDIR_21_20_EVEN : Pin N2HET[20] is output and N2HET[21] is input
9	LBPDIR_19_18	R/W	0	Loop Back Pair Select Bits for pins N2HET[19] and N2HET[18]: 0 = LBPDIR_19_18_ODD : Pin N2HET[19] is output and N2HET[18] is input 1 = LBPDIR_19_18_EVEN : Pin N2HET[18] is output and N2HET[19] is input

1-34. HETLBPDIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LBPDIR_17_16	R/W	0	Loop Back Pair Select Bits for pins N2HET[17] and N2HET[16]: 0 = LBPDIR_17_16_ODD : Pin N2HET[17] is output and N2HET[16] is input 1 = LBPDIR_17_16_EVEN : Pin N2HET[16] is output and N2HET[17] is input
7	LBPDIR_15_14	R/W	0	Loop Back Pair Select Bits for pins N2HET[15] and N2HET[14]: 0 = LBPDIR_15_14_ODD : Pin N2HET[15] is output and N2HET[14] is input 1 = LBPDIR_15_14_EVEN : Pin N2HET[14] is output and N2HET[15] is input
6	LBPDIR_13_12	R/W	0	Loop Back Pair Select Bits for pins N2HET[13] and N2HET[12]: 0 = LBPDIR_13_12_ODD : Pin N2HET[13] is output and N2HET[12] is input 1 = LBPDIR_13_12_EVEN : Pin N2HET[12] is output and N2HET[13] is input
5	LBPDIR_11_10	R/W	0	Loop Back Pair Select Bits for pins N2HET[11] and N2HET[10]: 0 = LBPDIR_11_10_ODD : Pin N2HET[11] is output and N2HET[10] is input 1 = LBPDIR_11_10_EVEN : Pin N2HET[10] is output and N2HET[11] is input
4	LBPDIR_9_8	R/W	0	Loop Back Pair Select Bits for pins N2HET[9] and N2HET[8]: 0 = LBPDIR_9_8_ODD : Pin N2HET[9] is output and N2HET[8] is input 1 = LBPDIR_9_8_EVEN : Pin N2HET[8] is output and N2HET[9] is input
3	LBPDIR_7_6	R/W	0	Loop Back Pair Select Bits for pins N2HET[7] and N2HET[6]: 0 = LBPDIR_7_6_ODD : Pin N2HET[7] is output and N2HET[6] is input 1 = LBPDIR_7_6_EVEN : Pin N2HET[6] is output and N2HET[7] is input
2	LBPDIR_5_4	R/W	0	Loop Back Pair Select Bits for pins N2HET[5] and N2HET[4]: 0 = LBPDIR_5_4_ODD : Pin N2HET[5] is output and N2HET[4] is input 1 = LBPDIR_5_4_EVEN : Pin N2HET[4] is output and N2HET[5] is input
1	LBPDIR_3_2	R/W	0	Loop Back Pair Select Bits for pins N2HET[3] and N2HET[2]: 0 = LBPDIR_3_2_ODD : Pin N2HET[3] is output and N2HET[2] is input 1 = LBPDIR_3_2_EVEN : Pin N2HET[2] is output and N2HET[3] is input
0	LBPDIR_1_0	R/W	0	Loop Back Pair Select Bits for pins N2HET[1] and N2HET[0]: 0 = LBPDIR_1_0_ODD : Pin N2HET[1] is output and N2HET[0] is input 1 = LBPDIR_1_0_EVEN : Pin N2HET[0] is output and N2HET[1] is input

The loop back direction can be selected independent on the HETDIR register setting.

1.1.33 HETPINDIS Register

N2HET1: offset = FFF7 B894h; **N2HET2:** offset = FFF7 B994h

1-33. N2HET Pin Disable Register (HETPINDIS)

31	16
HETPINDIS	
R/W-0	
15	0
HETPINDIS	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

1-35. HETPINDIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HETPINDIS_31	R/W	0	N2HET[31] Pin Disable 0 = HETPINDIS_31_OFF : N2HET[31] ignores nDIS error input 1 = HETPINDIS_31_ON : N2HET[31] disabled when nDIS input is active.
30	HETPINDIS_30	R/W	0	N2HET[30] Pin Disable 0 = HETPINDIS_30_OFF : N2HET[30] ignores nDIS error input 1 = HETPINDIS_30_ON : N2HET[30] disabled when nDIS input is active.
29	HETPINDIS_29	R/W	0	N2HET[29] Pin Disable 0 = HETPINDIS_29_OFF : N2HET[29] ignores nDIS error input 1 = HETPINDIS_29_ON : N2HET[29] disabled when nDIS input is active.
28	HETPINDIS_28	R/W	0	N2HET[28] Pin Disable 0 = HETPINDIS_28_OFF : N2HET[28] ignores nDIS error input 1 = HETPINDIS_28_ON : N2HET[28] disabled when nDIS input is active.
27	HETPINDIS_27	R/W	0	N2HET[27] Pin Disable 0 = HETPINDIS_27_OFF : N2HET[27] ignores nDIS error input 1 = HETPINDIS_27_ON : N2HET[27] disabled when nDIS input is active.
26	HETPINDIS_26	R/W	0	N2HET[26] Pin Disable 0 = HETPINDIS_26_OFF : N2HET[26] ignores nDIS error input 1 = HETPINDIS_26_ON : N2HET[26] disabled when nDIS input is active.
25	HETPINDIS_25	R/W	0	N2HET[25] Pin Disable 0 = HETPINDIS_25_OFF : N2HET[25] ignores nDIS error input 1 = HETPINDIS_25_ON : N2HET[25] disabled when nDIS input is active.
24	HETPINDIS_24	R/W	0	N2HET[24] Pin Disable 0 = HETPINDIS_24_OFF : N2HET[24] ignores nDIS error input 1 = HETPINDIS_24_ON : N2HET[24] disabled when nDIS input is active.
23	HETPINDIS_23	R/W	0	N2HET[23] Pin Disable 0 = HETPINDIS_23_OFF : N2HET[23] ignores nDIS error input 1 = HETPINDIS_23_ON : N2HET[23] disabled when nDIS input is active.

1-35. HETPINDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	HETPINDIS_22	R/W	0	N2HET[22] Pin Disable 0 = HETPINDIS_22_OFF : N2HET[22] ignores nDIS error input 1 = HETPINDIS_22_ON : N2HET[22] disabled when nDIS input is active.
21	HETPINDIS_21	R/W	0	N2HET[21] Pin Disable 0 = HETPINDIS_21_OFF : N2HET[21] ignores nDIS error input 1 = HETPINDIS_21_ON : N2HET[21] disabled when nDIS input is active.
20	HETPINDIS_20	R/W	0	N2HET[20] Pin Disable 0 = HETPINDIS_20_OFF : N2HET[20] ignores nDIS error input 1 = HETPINDIS_20_ON : N2HET[20] disabled when nDIS input is active.
19	HETPINDIS_19	R/W	0	N2HET[19] Pin Disable 0 = HETPINDIS_19_OFF : N2HET[19] ignores nDIS error input 1 = HETPINDIS_19_ON : N2HET[19] disabled when nDIS input is active.
18	HETPINDIS_18	R/W	0	N2HET[18] Pin Disable 0 = HETPINDIS_18_OFF : N2HET[18] ignores nDIS error input 1 = HETPINDIS_18_ON : N2HET[18] disabled when nDIS input is active.
17	HETPINDIS_17	R/W	0	N2HET[17] Pin Disable 0 = HETPINDIS_17_OFF : N2HET[17] ignores nDIS error input 1 = HETPINDIS_17_ON : N2HET[17] disabled when nDIS input is active.
16	HETPINDIS_16	R/W	0	N2HET[16] Pin Disable 0 = HETPINDIS_16_OFF : N2HET[16] ignores nDIS error input 1 = HETPINDIS_16_ON : N2HET[16] disabled when nDIS input is active.
15	HETPINDIS_15	R/W	0	N2HET[15] Pin Disable 0 = HETPINDIS_15_OFF : N2HET[15] ignores nDIS error input 1 = HETPINDIS_15_ON : N2HET[15] disabled when nDIS input is active.
14	HETPINDIS_14	R/W	0	N2HET[14] Pin Disable 0 = HETPINDIS_14_OFF : N2HET[14] ignores nDIS error input 1 = HETPINDIS_14_ON : N2HET[14] disabled when nDIS input is active.
13	HETPINDIS_13	R/W	0	N2HET[13] Pin Disable 0 = HETPINDIS_13_OFF : N2HET[13] ignores nDIS error input 1 = HETPINDIS_13_ON : N2HET[13] disabled when nDIS input is active.
12	HETPINDIS_12	R/W	0	N2HET[12] Pin Disable 0 = HETPINDIS_12_OFF : N2HET[12] ignores nDIS error input 1 = HETPINDIS_12_ON : N2HET[12] disabled when nDIS input is active.
11	HETPINDIS_11	R/W	0	N2HET[11] Pin Disable 0 = HETPINDIS_11_OFF : N2HET[11] ignores nDIS error input 1 = HETPINDIS_11_ON : N2HET[11] disabled when nDIS input is active.

1-35. HETPINDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HETPINDIS_10	R/W	0	N2HET[10] Pin Disable 0 = HETPINDIS_10_OFF : N2HET[10] ignores nDIS error input 1 = HETPINDIS_10_ON : N2HET[10] disabled when nDIS input is active.
9	HETPINDIS_9	R/W	0	N2HET[9] Pin Disable 0 = HETPINDIS_9_OFF : N2HET[9] ignores nDIS error input 1 = HETPINDIS_9_ON : N2HET[9] disabled when nDIS input is active.
8	HETPINDIS_8	R/W	0	N2HET[8] Pin Disable 0 = HETPINDIS_8_OFF : N2HET[8] ignores nDIS error input 1 = HETPINDIS_8_ON : N2HET[8] disabled when nDIS input is active.
7	HETPINDIS_7	R/W	0	N2HET[7] Pin Disable 0 = HETPINDIS_7_OFF : N2HET[7] ignores nDIS error input 1 = HETPINDIS_7_ON : N2HET[7] disabled when nDIS input is active.
6	HETPINDIS_6	R/W	0	N2HET[6] Pin Disable 0 = HETPINDIS_6_OFF : N2HET[6] ignores nDIS error input 1 = HETPINDIS_6_ON : N2HET[6] disabled when nDIS input is active.
5	HETPINDIS_5	R/W	0	N2HET[5] Pin Disable 0 = HETPINDIS_5_OFF : N2HET[5] ignores nDIS error input 1 = HETPINDIS_5_ON : N2HET[5] disabled when nDIS input is active.
4	HETPINDIS_4	R/W	0	N2HET[4] Pin Disable 0 = HETPINDIS_4_OFF : N2HET[4] ignores nDIS error input 1 = HETPINDIS_4_ON : N2HET[4] disabled when nDIS input is active.
3	HETPINDIS_3	R/W	0	N2HET[3] Pin Disable 0 = HETPINDIS_3_OFF : N2HET[3] ignores nDIS error input 1 = HETPINDIS_3_ON : N2HET[3] disabled when nDIS input is active.
2	HETPINDIS_2	R/W	0	N2HET[2] Pin Disable 0 = HETPINDIS_2_OFF : N2HET[2] ignores nDIS error input 1 = HETPINDIS_2_ON : N2HET[2] disabled when nDIS input is active.
1	HETPINDIS_1	R/W	0	N2HET[1] Pin Disable 0 = HETPINDIS_1_OFF : N2HET[1] ignores nDIS error input 1 = HETPINDIS_1_ON : N2HET[1] disabled when nDIS input is active.
0	HETPINDIS_0	R/W	0	N2HET[0] Pin Disable 0 = HETPINDIS_0_OFF : N2HET[0] ignores nDIS error input 1 = HETPINDIS_0_ON : N2HET[0] disabled when nDIS input is active.

1.1.34 HWAPINSEL Register

1-36. HWAPINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
5-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-4	PINSEL	R/W	2	Pin select register: This register determines which N2HET pin is used by the HWAG as the toothed wheel signal. 0 = HWAPIN0: N2HET[0] is selected. 1 = HWAPIN0: N2HET[1] is selected. 2 = HWAPIN0: N2HET[2] is selected. 3 = HWAPIN0: N2HET[3] is selected. 4 = HWAPIN0: N2HET[4] is selected. 5 = HWAPIN0: N2HET[5] is selected. 6 = HWAPIN0: N2HET[6] is selected. 7 = HWAPIN0: N2HET[7] is selected. 8 = HWAPIN0: N2HET[8] is selected. 9 = HWAPIN0: N2HET[9] is selected. 10 = HWAPIN0: N2HET[10] is selected. 11 = HWAPIN0: N2HET[11] is selected. 12 = HWAPIN0: N2HET[12] is selected. 13 = HWAPIN0: N2HET[13] is selected. 14 = HWAPIN0: N2HET[14] is selected. 15 = HWAPIN0: N2HET[15] is selected. 16 = HWAPIN0: N2HET[16] is selected. 17 = HWAPIN0: N2HET[17] is selected. 18 = HWAPIN0: N2HET[18] is selected. 19 = HWAPIN0: N2HET[19] is selected. 20 = HWAPIN0: N2HET[20] is selected. 21 = HWAPIN0: N2HET[21] is selected. 22 = HWAPIN0: N2HET[22] is selected. 23 = HWAPIN0: N2HET[23] is selected. 24 = HWAPIN0: N2HET[24] is selected. 25 = HWAPIN0: N2HET[25] is selected. 26 = HWAPIN0: N2HET[26] is selected. 27 = HWAPIN0: N2HET[27] is selected. 28 = HWAPIN0: N2HET[28] is selected. 29 = HWAPIN0: N2HET[29] is selected. 30 = HWAPIN0: N2HET[30] is selected. 31 = HWAPIN0: N2HET[31] is selected.

1.1.35 HWAGCR0 Register

1-37. HWAGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
1-7	Reserved	R	0	Read returns 0. Writes have no effect.
0	RESET	R/W	0	Resets the HWAG 0 = HWAG_RESET : HWAG is in reset. 1 = HWAG_ON : HWAG is out of reset.

1.1.36 HWAGCR1 Register

1-38. HWAGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
25-31	Reserved	R	0	Read returns 0. Writes have no effect.
24	ARST	R/W	0	This bit is used to validate the singularity when the hardware criteria is not used. ARST is cleared whenver the ACNT counter is reset. If this bit is not set before the tooth edge during a singularity tooth, the HWAG sets the singularity not found interrupt flag. 0 = ARST_DIS : Reset of ACNT at angle 0 is disabled. 1 = ARST_ENA : Reset of ACNT at angle 0 is enabled
18-23	Reserved	R	0	Read returns 0. Writes have no effect.
17	TED	R/W	0	Tooth Edge :This bit is used to select the edge of the toothed wheel that is considered active: 0 = TED_FALL : Falling edge of the toothed wheel signals is the active edge. 1 = TED_RISE : Rising edge of the toothed wheel signals is the active edge.
16	CRI	R/W	0	Criteria Enable: This bit is used to determine whether the hardware criteria filter is enabled. 0 = CRI_DIS : Criteria Disabled. 1 = CRI_ENA : Criteria Enabled.
9-15	Reserved	R	0	Read returns 0. Writes have no effect.
8	FIL	R/W	0	Filter Input Enable: Enables the toothed wheel input filter. 0 = FIL_DIS : Filter Disabled. 1 = FIL_ENA : Filter Enabled.
1-7	Reserved	R	0	Read returns 0. Writes have no effect.
0	STRT	R/W	0	Start bit: Puts the HWAG online, counting ACNT, TCNT and checking the criteria mechanism. The HWAG will start from the next active edge of the toothed wheel after this bit is set. 0 = HWA_STOP : Stop the HWAG. 1 = HWA_START: Start the HWAG.

1.1.37 HWAINTENAS Register

1-39. HWAINTENAS Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	ANGIOVFL_ENAS	R/W1S	0	Angle Increment Overflow Interrupt Flag 1 = HWAENA_ANGIOVFL_ISENA R: Angle Increment Overflow Interrupt is Enabled 0 = HWAENA_ANGIOVFL_ISDIS R: Angle Increment Overflow Interrupt is Disabled 1 = HWAENA_ANGIOVFL_ENA W: Enables Angle Increment Overflow Interrupt 0 = HWAENA_ANGIOVFL_NA W: Write of 0 Has No Effect.
6	GFLG_ENAS	R/W1S	0	Gap Flag Interrupt Flag 1 = HWAENA_GFLG_ISENA R: Gap Flag Interrupt is Enabled 0 = HWAENA_GFLG_ISDIS R: Gap Flag Interrupt is Disabled 1 = HWAENA_GFLG_ENA W: Enables Gap Flag Interrupt 0 = HWAENA_GFLG_NA W: Write of 0 Has No Effect.
5	BADTH_ENAS	R/W1S	0	Bad Tooth Interrupt Flag 1 = HWAENA_BADTH_ISENA R: Bad Tooth Interrupt is Enabled 0 = HWAENA_BADTH_ISDIS R: Bad Tooth Interrupt is Disabled 1 = HWAENA_BADTH_ENA W: Enables Bad Tooth Interrupt 0 = HWAENA_BADTH_NA W: Write of 0 Has No Effect.
4	PCNTRNG_ENAS	R/W1S	0	PCNT Out of Range Interrupt Flag 1 = HWAENA_PCNTRNG_ISENA R: PCNT Out Of Range Interrupt is Enabled 0 = HWAENA_PCNTRNG_ISDIS R: PCNT Out Of Range Interrupt is Disabled 1 = HWAENA_PCNTRNG_ENA W: Enables PCNT Out Of Range Interrupt 0 = HWAENA_PCNTRNG_NA W: Write of 0 Has No Effect.
3	ACNTOVFL_ENAS	R/W1S	0	ACNT Overflow Interrupt Flag 1 = HWAENA_ACNTOVFL_ISENA R: ACNT Overflow Interrupt is Enabled 0 = HWAENA_ACNTOVFL_ISDIS R: ACNT Overflow Interrupt is Disabled 1 = HWAENA_ACNTOVFL_ENA W: Enables ACNT Overflow Interrupt 0 = HWAENA_ACNTOVFL_NA W: Write of 0 Has No Effect.
2	TH_ENAS	R/W1S	0	Tooth Interrupt Flag 1 = HWAENA_TH_ISENA R: Tooth Interrupt is Enabled 0 = HWAENA_TH_ISDIS R: Tooth Interrupt is Disabled 1 = HWAENA_TH_ENA W: Enables Tooth Interrupt 0 = HWAENA_TH_NA W: Write of 0 Has No Effect.
1	SNF_ENAS	R/W1S	0	Singularity Not Found Interrupt Flag 1 = HWAENA_SNF_ISENA R: Singularity Not Found Interrupt is Enabled 0 = HWAENA_SNF_ISDIS R: Singularity Not Found Interrupt is Disabled 1 = HWAENA_SNF_ENA W: Enables Singularity Not Found Interrupt 0 = HWAENA_SNF_NA W: Write of 0 Has No Effect.

1-39. HWAINTENAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PEROVFL_ENAS	R/W1S	0	Period Overflow Interrupt Flag 1 = HWAENA_PEROVFL_ISENA R: Period Overflow Interrupt is Enabled 0 = HWAENA_PEROVFL_ISDIS R: Period Overflow Interrupt is Disabled 1 = HWAENA_PEROVFL_ENA W: Enables Period Overflow Interrupt 0 = HWAENA_PEROVFL_NA W: Write of 0 Has No Effect.

1.1.38 HWAINTENAC Register

1-40. HWAINTENAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	ANGIOVFL_ENAC	R/W1C	0	Angle Increment Overflow Interrupt Flag 1 = HWAENA_ANGIOVFL_ISENA R: Angle Increment Overflow Interrupt is Enabled 0 = HWAENA_ANGIOVFL_ISDIS R: Angle Increment Overflow Interrupt is Disabled 1 = HWAENA_ANGIOVFL_DIS W: Disables Angle Increment Overflow Interrupt 0 = HWAENA_ANGIOVFL_NA W: Write of 0 Has No Effect.
6	GFLG_ENAC	R/W1C	0	Gap Flag Interrupt Flag 1 = HWAENA_GFLG_ISENA R: Gap Flag Interrupt is Enabled 0 = HWAENA_GFLG_ISDIS R: Gap Flag Interrupt is Disabled 1 = HWAENA_GFLG_DIS W: Disables Gap Flag Interrupt 0 = HWAENA_GFLG_NA W: Write of 0 Has No Effect.
5	BADTH_ENAC	R/W1C	0	Bad Tooth Interrupt Flag 1 = HWAENA_BADTH_ISENA R: Bad Tooth Interrupt is Enabled 0 = HWAENA_BADTH_ISDIS R: Bad Tooth Interrupt is Disabled 1 = HWAENA_BADTH_DIS W: Disables Bad Tooth Interrupt 0 = HWAENA_BADTH_NA W: Write of 0 Has No Effect.
4	PCNTRNG_ENAC	R/W1C	0	PCNT Out of Range Interrupt Flag 1 = HWAENA_PCNTRNG_ISENA R: PCNT Out Of Range Interrupt is Enabled 0 = HWAENA_PCNTRNG_ISDIS R: PCNT Out Of Range Interrupt is Disabled 1 = HWAENA_PCNTRNG_DIS W: Disables PCNT Out Of Range Interrupt 0 = HWAENA_PCNTRNG_NA W: Write of 0 Has No Effect.
3	ACNTOVFL_ENAC	R/W1C	0	ACNT Overflow Interrupt Flag 1 = HWAENA_ACNTOVFL_ISENA R: ACNT Overflow Interrupt is Enabled 0 = HWAENA_ACNTOVFL_ISDIS R: ACNT Overflow Interrupt is Disabled 1 = HWAENA_ACNTOVFL_DIS W: Disables ACNT Overflow Interrupt 0 = HWAENA_ACNTOVFL_NA W: Write of 0 Has No Effect.
2	TH_ENAC	R/W1C	0	Tooth Interrupt Flag 1 = HWAENA_TH_ISENA R: Tooth Interrupt is Enabled 0 = HWAENA_TH_ISDIS R: Tooth Interrupt is Disabled 1 = HWAENA_TH_DIS W: Disables Tooth Interrupt 0 = HWAENA_TH_NA W: Write of 0 Has No Effect.
1	SNF_ENAC	R/W1C	0	Singularity Not Found Interrupt Flag 1 = HWAENA_SNF_ISENA R: Singularity Not Found Interrupt is Enabled 0 = HWAENA_SNF_ISDIS R: Singularity Not Found Interrupt is Disabled 1 = HWAENA_SNF_DIS W: Disables Singularity Not Found Interrupt 0 = HWAENA_SNF_NA W: Write of 0 Has No Effect.

1-40. HWAINTENAC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PEROVFL_ENAC	R/W1C	0	Period Overflow Interrupt Flag 1 = HWAENA_PEROVFL_ISENA R: Period Overflow Interrupt is Enabled 0 = HWAENA_PEROVFL_ISDIS R: Period Overflow Interrupt is Disabled 1 = HWAENA_PEROVFL_DIS W: Disables Period Overflow Interrupt 0 = HWAENA_PEROVFL_NA W: Write of 0 Has No Effect.

1.1.39 HWAPRYS Register

1-41. HWAPRYS Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	ANGIOVFL_PRYS	R/W1S	0	Angle Increment Overflow Interrupt Flag 1 = HWAPRY_ANGIOVFL_LVL1 R: Angle Increment Overflow Interrupt Level is 1 0 = HWAPRY_ANGIOVFL_LVL0 R: Angle Increment Overflow Interrupt Level is 0 1 = HWAPRY_ANGIOVFL_SET W: Sets Angle Increment Overflow Interrupt Level to 1 0 = HWAPRY_ANGIOVFL_NA W: Write of 0 Has No Effect.
6	GFLG_PRYS	R/W1S	0	Gap Flag Interrupt Flag 1 = HWAPRY_GFLG_LVL1 R: Gap Flag Interrupt Level is 1 0 = HWAPRY_GFLG_LVL0 R: Gap Flag Interrupt Level is 0 1 = HWAPRY_GFLG_SET W: Sets Gap Flag Interrupt Level to 1 0 = HWAPRY_GFLG_NA W: Write of 0 Has No Effect.
5	BADTH_PRYS	R/W1S	0	Bad Tooth Interrupt Flag 1 = HWAPRY_BADTH_LVL1 R: Bad Tooth Interrupt Level is 1 0 = HWAPRY_BADTH_LVL0 R: Bad Tooth Interrupt Level is 0 1 = HWAPRY_BADTH_SET W: Sets Bad Tooth Interrupt Level to 1 0 = HWAPRY_BADTH_NA W: Write of 0 Has No Effect.
4	PCNTRNG_PRYS	R/W1S	0	PCNT Out of Range Interrupt Flag 1 = HWAPRY_PCNTRNG_LVL1 R: PCNT Out Of Range Interrupt Level is 1 0 = HWAPRY_PCNTRNG_LVL0 R: PCNT Out Of Range Interrupt Level is 0 1 = HWAPRY_PCNTRNG_SET W: Sets PCNT Out Of Range Interrupt Level to 1 0 = HWAPRY_PCNTRNG_NA W: Write of 0 Has No Effect.
3	ACNTOVFL_PRYS	R/W1S	0	ACNT Overflow Interrupt Flag 1 = HWAPRY_ACNTOVFL_LVL1 R: ACNT Overflow Interrupt Level is 1 0 = HWAPRY_ACNTOVFL_LVL0 R: ACNT Overflow Interrupt Level is 0 1 = HWAPRY_ACNTOVFL_SET W: Sets ACNT Overflow Interrupt Level to 1 0 = HWAPRY_ACNTOVFL_NA W: Write of 0 Has No Effect.
2	TH_PRYS	R/W1S	0	Tooth Interrupt Flag 1 = HWAPRY_TH_LVL1 R: Tooth Interrupt Level is 1 0 = HWAPRY_TH_LVL0 R: Tooth Interrupt Level is 0 1 = HWAPRY_TH_SET W: Sets Tooth Interrupt Level to 1 0 = HWAPRY_TH_NA W: Write of 0 Has No Effect.
1	SNF_PRYS	R/W1S	0	Singularity Not Found Interrupt Flag 1 = HWAPRY_SNF_LVL1 R: Singularity Not Found Interrupt Level is 1 0 = HWAPRY_SNF_LVL0 R: Singularity Not Found Interrupt Level is 0 1 = HWAPRY_SNF_SET W: Sets Singularity Not Found Interrupt Level to 1 0 = HWAPRY_SNF_NA W: Write of 0 Has No Effect.

1-41. HWAPRYS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PEROVFL_PRYS	R/W1S	0	Period Overflow Interrupt Flag 1 = HWAPRY_PEROVFL_LVL1 R: Period Overflow Interrupt Level is 1 0 = HWAPRY_PEROVFL_LVL0 R: Period Overflow Interrupt Level is 0 1 = HWAPRY_PEROVFL_SET W: Sets Period Overflow Interrupt Level to 1 0 = HWAPRY_PEROVFL_NA W: Write of 0 Has No Effect.

1.1.40 HWAPRYC Register

1-42. HWAPRYC Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	ANGIOVFL_PRYC	R/W1C	0	Angle Increment Overflow Interrupt Flag 1 = HWAPRY_ANGIOVFL_LVL1 R: Angle Increment Overflow Interrupt Level is 1 0 = HWAPRY_ANGIOVFL_LVL0 R: Angle Increment Overflow Interrupt Level is 0 1 = HWAPRY_ANGIOVFL_CLR W: Clears Angle Increment Overflow Interrupt Level to 0 0 = HWAPRY_ANGIOVFL_NA W: Write of 0 Has No Effect.
6	GFLG_PRYC	R/W1C	0	Gap Flag Interrupt Flag 1 = HWAPRY_GFLG_LVL1 R: Gap Flag Interrupt Level is 1 0 = HWAPRY_GFLG_LVL0 R: Gap Flag Interrupt Level is 0 1 = HWAPRY_GFLG_CLR W: Clears Gap Flag Interrupt Level to 0 0 = HWAPRY_GFLG_NA W: Write of 0 Has No Effect.
5	BADTH_PRYC	R/W1C	0	Bad Tooth Interrupt Flag 1 = HWAPRY_BADTH_LVL1 R: Bad Tooth Interrupt Level is 1 0 = HWAPRY_BADTH_LVL0 R: Bad Tooth Interrupt Level is 0 1 = HWAPRY_BADTH_CLR W: Clears Bad Tooth Interrupt Level to 0 0 = HWAPRY_BADTH_NA W: Write of 0 Has No Effect.
4	PCNTRNG_PRYC	R/W1C	0	PCNT Out of Range Interrupt Flag 1 = HWAPRY_PCNTRNG_LVL1 R: PCNT Out Of Range Interrupt Level is 1 0 = HWAPRY_PCNTRNG_LVL0 R: PCNT Out Of Range Interrupt Level is 0 1 = HWAPRY_PCNTRNG_CLR W: Clears PCNT Out Of Range Interrupt Level to 0 0 = HWAPRY_PCNTRNG_NA W: Write of 0 Has No Effect.
3	ACNTOVFL_PRYC	R/W1C	0	ACNT Overflow Interrupt Flag 1 = HWAPRY_ACNTOVFL_LVL1 R: ACNT Overflow Interrupt Level is 1 0 = HWAPRY_ACNTOVFL_LVL0 R: ACNT Overflow Interrupt Level is 0 1 = HWAPRY_ACNTOVFL_CLR W: Clears ACNT Overflow Interrupt Level to 0 0 = HWAPRY_ACNTOVFL_NA W: Write of 0 Has No Effect.
2	TH_PRYC	R/W1C	0	Tooth Interrupt Flag 1 = HWAPRY_TH_LVL1 R: Tooth Interrupt Level is 1 0 = HWAPRY_TH_LVL0 R: Tooth Interrupt Level is 0 1 = HWAPRY_TH_CLR W: Clears Tooth Interrupt Level to 0 0 = HWAPRY_TH_NA W: Write of 0 Has No Effect.
1	SNF_PRYC	R/W1C	0	Singularity Not Found Interrupt Flag 1 = HWAPRY_SNF_LVL1 R: Singularity Not Found Interrupt Level is 1 0 = HWAPRY_SNF_LVL0 R: Singularity Not Found Interrupt Level is 0 1 = HWAPRY_SNF_CLR W: Clears Singularity Not Found Interrupt Level to 0 0 = HWAPRY_SNF_NA W: Write of 0 Has No Effect.

1-42. HWAPRYC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PEROVFL_PRYC	R/W1C	0	Period Overflow Interrupt Flag 1 = HWAPRY_PEROVFL_LVL1 R: Period Overflow Interrupt Level is 1 0 = HWAPRY_PEROVFL_LVL0 R: Period Overflow Interrupt Level is 0 1 = HWAPRY_PEROVFL_CLR W: Clears Period Overflow Interrupt Level to 0 0 = HWAPRY_PEROVFL_NA W: Write of 0 Has No Effect.

1.1.41 HWAFLG Register

1-43. HWAFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
7	ANGIOVFL_FLG	R/W1C	0	Angle Increment Overflow Interrupt Flag 1 = HWAFLG_ANGIOVFL_ACT R: Angle Increment Overflow Interrupt Pending 0 = HWAFLG_ANGIOVFL_INACT R: Angle Increment Overflow Interrupt Not Pending 1 = HWAFLG_ANGIOVFL_CLR W: Clears Angle Increment Overflow Interrupt Flag 0 = HWAFLG_ANGIOVFL_NA W: Write of 0 Has No Effect.
6	GFLG_FLG	R/W1C	0	Gap Flag Interrupt Flag 1 = HWAFLG_GFLG_ACT R: Gap Flag Interrupt Pending 0 = HWAFLG_GFLG_INACT R: Gap Flag Interrupt Not Pending 1 = HWAFLG_GFLG_CLR W: Clears Gap Flag Interrupt Flag 0 = HWAFLG_GFLG_NA W: Write of 0 Has No Effect.
5	BADTH_FLG	R/W1C	0	Bad Tooth Interrupt Flag 1 = HWAFLG_BADTH_ACT R: Bad Tooth Interrupt Pending 0 = HWAFLG_BADTH_INACT R: Bad Tooth Interrupt Not Pending 1 = HWAFLG_BADTH_CLR W: Clears Bad Tooth Interrupt Flag 0 = HWAFLG_BADTH_NA W: Write of 0 Has No Effect.
4	PCNTRNG_FLG	R/W1C	0	PCNT Out of Range Interrupt Flag 1 = HWAFLG_PCNTRNG_ACT R: PCNT Out Of Range Interrupt Pending 0 = HWAFLG_PCNTRNG_INACT R: PCNT Out Of Range Interrupt Not Pending 1 = HWAFLG_PCNTRNG_CLR W: Clears PCNT Out Of Range Interrupt Flag 0 = HWAFLG_PCNTRNG_NA W: Write of 0 Has No Effect.
3	ACNTOVFL_FLG	R/W1C	0	ACNT Overflow Interrupt Flag 1 = HWAFLG_ACNTOVFL_ACT R: ACNT Overflow Interrupt Pending 0 = HWAFLG_ACNTOVFL_INACT R: ACNT Overflow Interrupt Not Pending 1 = HWAFLG_ACNTOVFL_CLR W: Clears ACNT Overflow Interrupt Flag 0 = HWAFLG_ACNTOVFL_NA W: Write of 0 Has No Effect.
2	TH_FLG	R/W1C	0	Tooth Interrupt Flag 1 = HWAFLG_TH_ACT R: Tooth Interrupt Pending 0 = HWAFLG_TH_INACT R: Tooth Interrupt Not Pending 1 = HWAFLG_TH_CLR W: Clears Tooth Interrupt Flag 0 = HWAFLG_TH_NA W: Write of 0 Has No Effect.
1	SNF_FLG	R/W1C	0	Singularity Not Found Interrupt Flag 1 = HWAFLG_SNF_ACT R: Singularity Not Found Interrupt Pending 0 = HWAFLG_SNF_INACT R: Singularity Not Found Interrupt Not Pending 1 = HWAFLG_SNF_CLR W: Clears Singularity Not Found Interrupt Flag 0 = HWAFLG_SNF_NA W: Write of 0 Has No Effect.

1-43. HWAFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PEROVFL_FLG	R/W1C	0	Period Overflow Interrupt Flag 1 = HWAFLG_PEROVFL_ACT R: Period Overflow Interrupt Pending 0 = HWAFLG_PEROVFL_INACT R: Period Overflow Interrupt Not Pending 1 = HWAFLG_PEROVFL_CLR W: Clears Period Overflow Interrupt Flag 0 = HWAFLG_PEROVFL_NA W: Write of 0 Has No Effect.

1.1.42 HWAOFF0 Register

1-44. HWAOFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-7	OFFSET1	R	0	Priority Level 0 Interrupt Offset. Reading from this register returns the highest priority interrupt pending on the priority level 0 and clears the corresponding flag in the HWAFLG register, unless the read occurs during emulation mode. Offset values are encoded as follows, values not listed are reserved: 0 = HWAOFF_NONE: There are currently no priority level 1 Interrupts pending. 1 = HWAOFF_PEROVFL: Period Overflow Interrupt Pending 2 = HWAOFF_SNF: Singularity Not Found Interrupt Pending 3 = HWAOFF_TH : Tooth Interrupt Pending 4 = HWAOFF_ACNTOVFL : ACNT Overflow Interrupt Pending 5 = HWAOFF_PCNTRNG : PCNT Out Of Range Interrupt Pending 6 = HWAOFF_BADTH : Bad Tooth Interrupt Pending 7 = HWAOFF_GFLG : Gap Flag Interrupt pending 8 = HWAOFF_ANGIOVFL : Angle Increment Overflow Interrupt Pending

1.1.43 HWAOFF1 Register

1-45. HWAOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-7	OFFSET1	R	0	Priority Level 1 Interrupt Offset. Reading from this register returns the highest priority interrupt pending on the priority level 1 and clears the corresponding flag in the HWAFLG register, unless the read occurs during emulation mode. Offset values are encoded as follows, values not listed are reserved: 0 = HWAOFF_NONE: There are currently no priority level 1 Interrupts pending. 1 = HWAOFF_PEROVFL: Period Overflow Interrupt Pending 2 = HWAOFF_SNF: Singularity Not Found Interrupt Pending 3 = HWAOFF_TH : Tooth Interrupt Pending 4 = HWAOFF_ACNTOVFL : ACNT Overflow Interrupt Pending 5 = HWAOFF_PCNTRNG : PCNT Out Of Range Interrupt Pending 6 = HWAOFF_BADTH : Bad Tooth Interrupt Pending 7 = HWAOFF_GFLG : Gap Flag Interrupt pending 8 = HWAOFF_ANGIOVFL : Angle Increment Overflow Interrupt Pending

1.1.44 HWAACNT Register

1-46. HWAACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
24-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-23	ACNT	R/W	0	Provides the current angle value from the toothed wheel. This value is equal to the step width times the tooth value.

1.1.45 HWAPCNT0 Register

1-47. HWAPCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
24-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-23	PCNT0	R/W	0	Returns the period of the previous tooth.

1.1.46 HWAPCNT1 Register

1-48. HWAPCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
24-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-23	PCNT1	R/W	0	Returns the current period counter value, as measured from the active edge of the last tooth.

1.1.47 HWASTWD Register

1-49. HWASTWD Register Field Descriptions

Bit	Field	Type	Reset	Description
4-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-3	STWD	R/W	0	Step Width: Sets the step width for tick generation. 0 = STWD_4 : Step Width is 4 Ticks Per Period 1 = STWD_8 : Step Width is 8 Ticks Per Period 2 = STWD_16 : Step Width is 16 Ticks Per Period 3 = STWD_32 : Step Width is 32 Ticks Per Period 4 = STWD_64 : Step Width is 64 Ticks Per Period 5 = STWD_128 : Step Width is 128 Ticks Per Period 6 = STWD_256 : Step Width is 256 Ticks Per Period 7 = STWD_512 : Step Width is 512 Ticks Per Period 8 = STWD_1K : Step Width is 1024 Ticks Per Period 9 = STWD_2K: Step Width is 2048 Ticks Per Period 10 = STWD_4K : Step Width is 4096 Ticks Per Period 11 = STWD_8K : Step Width is 8192 Ticks Per Period 12 = STWD_16K : Step Width is 16384 Ticks Per Period 13 = STWD_32K : Step Width is 32768 Ticks Per Period 14 = STWD_64K : Step Width is 65536 Ticks Per Period 15 = STWD_128K : Step Width is 131072 Ticks Per Period

1.1.48 HWATHNUM Register

1-50. HWATHNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-7	THNUM	R/W	0	Number of Teeth: This register must be set to the number of teeth on the toothed wheel - 1. For example, a 60-2 wheel has 58 teeth; for this wheel the THNUM value should be programmed to 58-1=57.

1.1.49 HWATHCNT Register

1-51. HWATHCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
8-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-7	THCNT	R/W	0	Tooth Counter: Provides the current tooth number

1.1.50 HWAFIL0 Register

1-52. HWAFIL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
12-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-11	FIL0	R/W	0	Filter Value 0: Contains the value compared to the tick counter. It allows the tooth signal to be taken into account by the HWAG. Requires filtering to be enabled.

1.1.51 HWAFIL1 Register

1-53. HWAFIL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
12-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-11	FIL1	R/W	0	Filter Value 1: Contains the value to be compared to the tick counter during the singularity tooth. It allows the tooth signal to be taken into account by the HWAG. Requires filtering to be enabled.

1.1.52 HWAANGI Register

1-54. HWAANGI Register Field Descriptions

Bit	Field	Type	Reset	Description
10-31	Reserved	R	0	Read returns 0. Writes have no effect.
0-9	ANGI	R	0	Angle Increment Value: Reads return the current angle increment value.