

Soft-start circuits for LDO linear regulators

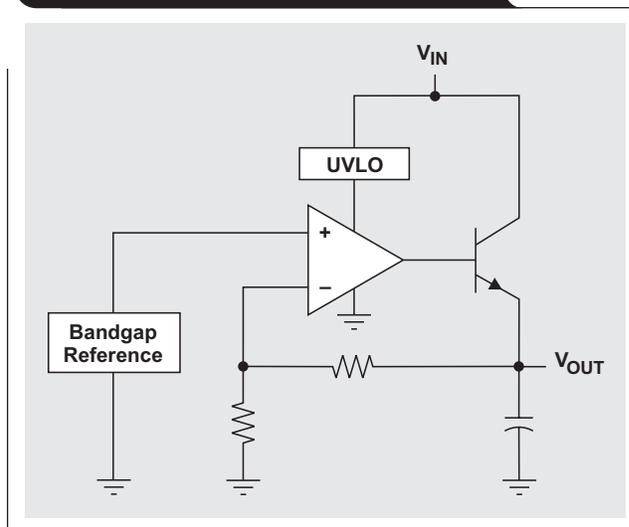
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Applications, Portable Power

Many low-dropout (LDO) linear regulators do not have an integrated “soft-start” function that limits the in-rush current to the device being powered. In fact, as the simplified block diagram in Figure 1 shows, most linear regulators consist of only a reference, an error amplifier, and a pass element. Thus, at startup, the error amplifier senses that the output voltage is low and drives the pass element as hard as possible. The pass element pulls a large in-rush current to charge the output capacitance and/or load current abruptly, after a short delay. The delay is caused by three factors: the time required for the input voltage to rise above the undervoltage lockout circuitry, if any; the time required for the chip’s internal circuitry, particularly the band-gap reference, to power up; and the time required for the regulator to sense its output voltage and turn on the pass element (i.e., the feedback loop bandwidth). The load resistance and the size of the regulator’s output capacitance influence the start-up response. If the regulator starts up into a large capacitive or small resistive load, the in-rush current will be large, approaching the regulator’s current limit in some cases. This article discusses two methods of slew-rate limiting a linear regulator’s output-voltage rise time and, consequently, limiting its in-rush current at startup. The TPS795xx, high-PSRR, low-noise family of regulators, which were designed for approximately 50- μ s start-up times and thus large start-up currents, are used as examples.

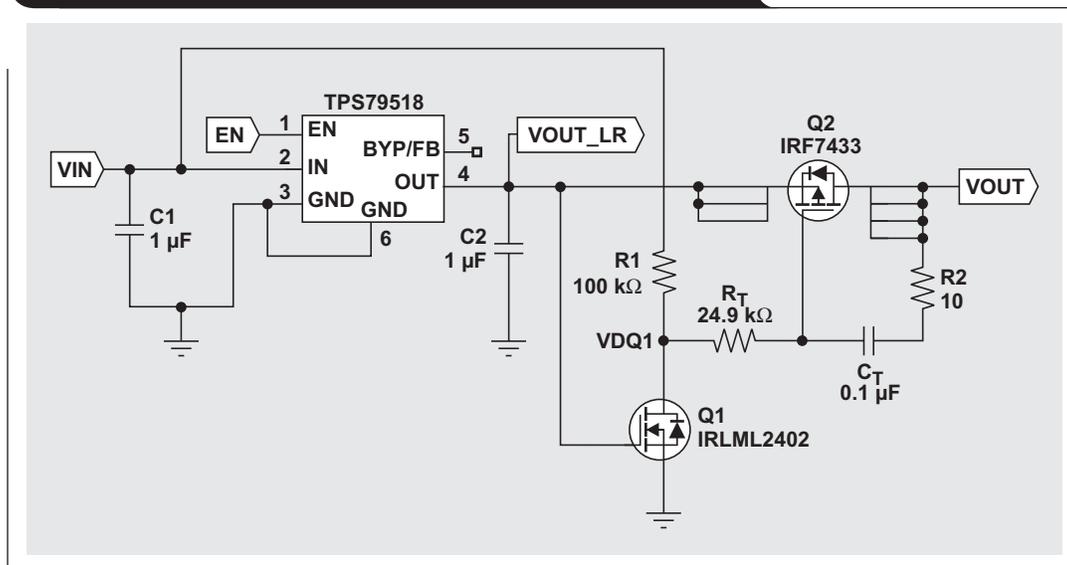
The simplest method uses a PMOS FET switch following the regulator output, in series with the regulator’s load, as shown in Figure 2. Note that the switch must be placed

Figure 1. Simplified block diagram of LDO linear regulator



after the regulator’s minimum required output capacitance (i.e., C₃) to ensure that the regulator remains stable. After the regulator turns on abruptly, FET Q1 operates as a crude supervisor and pulls R_T low. Capacitor C_T, effectively replacing the gate-to-drain capacitance of the FET, then causes the switch to function like an integrator and provides a more linear transition of the drain voltage.

Figure 2. Soft start using a PMOS FET following the output



Careful component selection is critical for proper operation of the circuit. First, Q1 and Q2 must have threshold voltages that are lower than the desired output voltage (i.e., $V_{OUT} > V_{TH1,2}$). Second, Q2's $r_{DS(on)}$ must be small enough so that the drop across it due to the maximum dc load current does not significantly reduce the regulated output voltage. C_T is selected to be much larger than the gate-to-drain capacitance (i.e., $C_T \gg C_{GD} = C_{RSS}$). R_T is chosen according to the equation

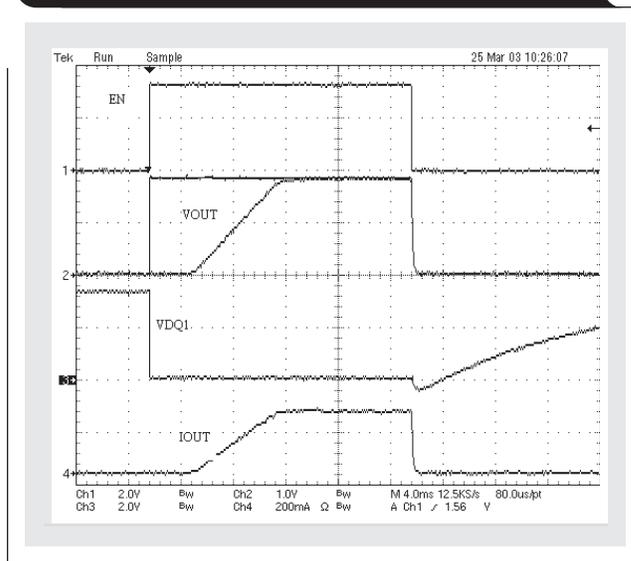
$$R_T = \frac{V_{OUT} - V_{TH}}{C_T \times \frac{V_{OUT}}{t_{Rise}}}$$

where t_{Rise} is the desired rise time (here 5 ms) and V_{TH} is Q2's threshold voltage (here 0.9 V). Resistor R1 is simply a large pull-up resistor. R2 should be selected to be much smaller than R_T .

Figure 3 shows the rise time of the regulator output voltage with and without the additional circuitry for $V_{IN} = 3.3$ V and $I_{OUT} = 300$ mA. The measured rise time is 6.5 ms, slightly larger than the designed 5 ms, but within an acceptable margin considering the variation in Q2's threshold voltage, V_{TH} . The 4-ms delay before startup is due to the RC time constant created by the PMOS FET's gate capacitances and R_T . With such a long start-up delay, the variation of threshold voltage of Q1, and thus the exact turn-on time of the switch, can be neglected.

The advantage of this method is its applicability to any regulator or dc/dc converter. The disadvantage is the difficulty in finding FETs either with low enough $r_{DS(on)}$ not to affect regulation under large load currents or with low enough threshold voltages for low output voltages. Another disadvantage is that this circuit does not work properly if V_{IN} is tied to EN. The IRF7433 has a maximum of 46-milliohm $r_{DS(on)}$ at $V_{GS} = -1.8$ V; so, at 300-mA output current, the output voltage could be 14 mV below the nominal voltage

Figure 3. Results from soft-start circuit using a PMOS FET following the output

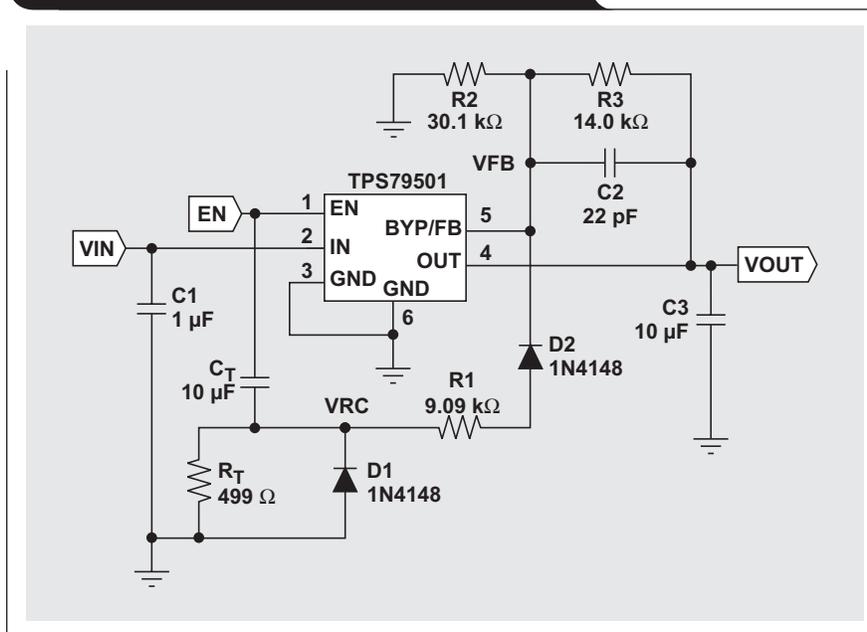


and thus could increase the lower tolerance limit of the regulator solution from -3 to -3.8% . In addition, to prevent large load transients from momentarily turning off the switch and causing the rail voltage to droop, a large output capacitor after the switch is recommended.

The second method uses an RC time constant and diode to shape the voltage that is being fed back from the output to the regulator at startup, as seen in Figure 4.

When the enable signal goes high, node V_{RC} charges to V_{EN} . With proper sizing of R1, the feedback node, V_{FB} , artificially rises above the regulated intended feedback voltage of 1.2 V to V_{FB2} . V_{FB2} is chosen to be at least

Figure 4. Soft-start circuit with RC and diode



200 mV above the intended feedback voltage but less than a diode drop below V_{EN} . Capacitor C_T then discharges through R_T and, as the feedback voltage drops, the pass element slowly turns on and the output voltage slowly rises. Diode D2 keeps R1 and R_T out of the feedback-voltage divider and therefore prevents any degradation in output-voltage tolerance during normal operation. Diode D1 clamps node V_{RC} to a diode drop below ground when EN is taken low.

The following equation is used to determine the appropriate size of R1 to raise node V_{FB} to V_{FB2} :

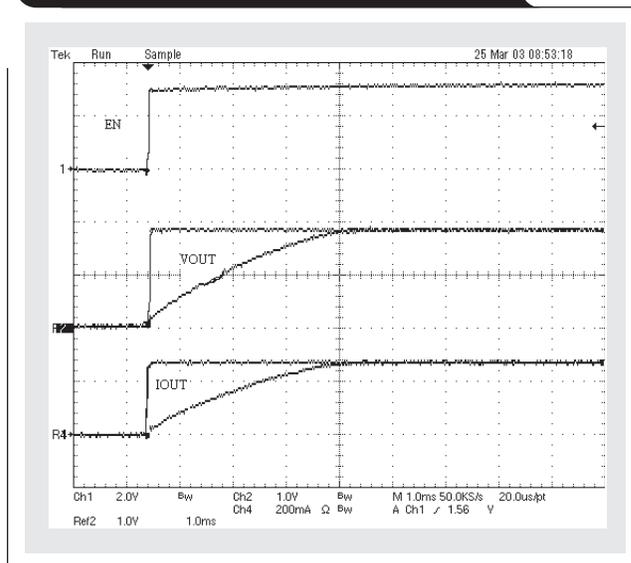
$$R1 = \frac{V_{IN(min)} - 0.6\text{ V} - V_{FB2}}{\frac{V_{FB2}}{R2 \parallel R3}}$$

In this example, V_{FB2} is $1.2\text{ V} + 0.2\text{ V} = 1.4\text{ V}$; and $V_{IN(min)}$ is 3.3 V , so the calculated value of R1 is $9\text{ k}\Omega$. Once R1 is determined, R_T is selected to be much smaller than R1 (roughly a factor of 10 or more) so that it will dominate the RC time constant; and then C_T can be sized to provide the appropriate rise time. In this example, the desired t_{Rise} is 5 ms for $R_T = 499\ \Omega$; and $C_T = 10\ \mu\text{F}$ is required.

Figure 5 shows the rise time of the regulator with and without the additional circuitry for $V_{IN} = 3.3\text{ V}$ and $I_{OUT} = 300\text{ mA}$. The measured rise time is slightly below 4 ms .

The advantages of this method are simplicity, low cost, and isolation from the regulator after startup because of diode D2 and also because the control voltage is not a function of the output voltage. The primary disadvantages are that this circuit requires the use of an adjustable regulator and that it does not work with some regulators. Regulators with extra features, like an integrated SVS or a fast transient-assist circuitry, require the output of the regulator to be biased above ground after it is enabled. Using this soft-start method with such regulators could cause the start-up waveform to have an initial voltage spike before the slow rise to the output voltage.

Figure 5. Results from soft-start circuit using RC and diode



Either method limits the in-rush current, slowing the ramp time of the regulator output. The first method is best suited for higher-voltage rails with looser output-voltage tolerances and fewer transients. The second method provides the best performance, since the additional circuitry is effectively removed after startup and thus does not affect regulation; however, it will not work with all regulators.

Related Web sites

analog.ti.com

www.ti.com/sc/device/TPS79501

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