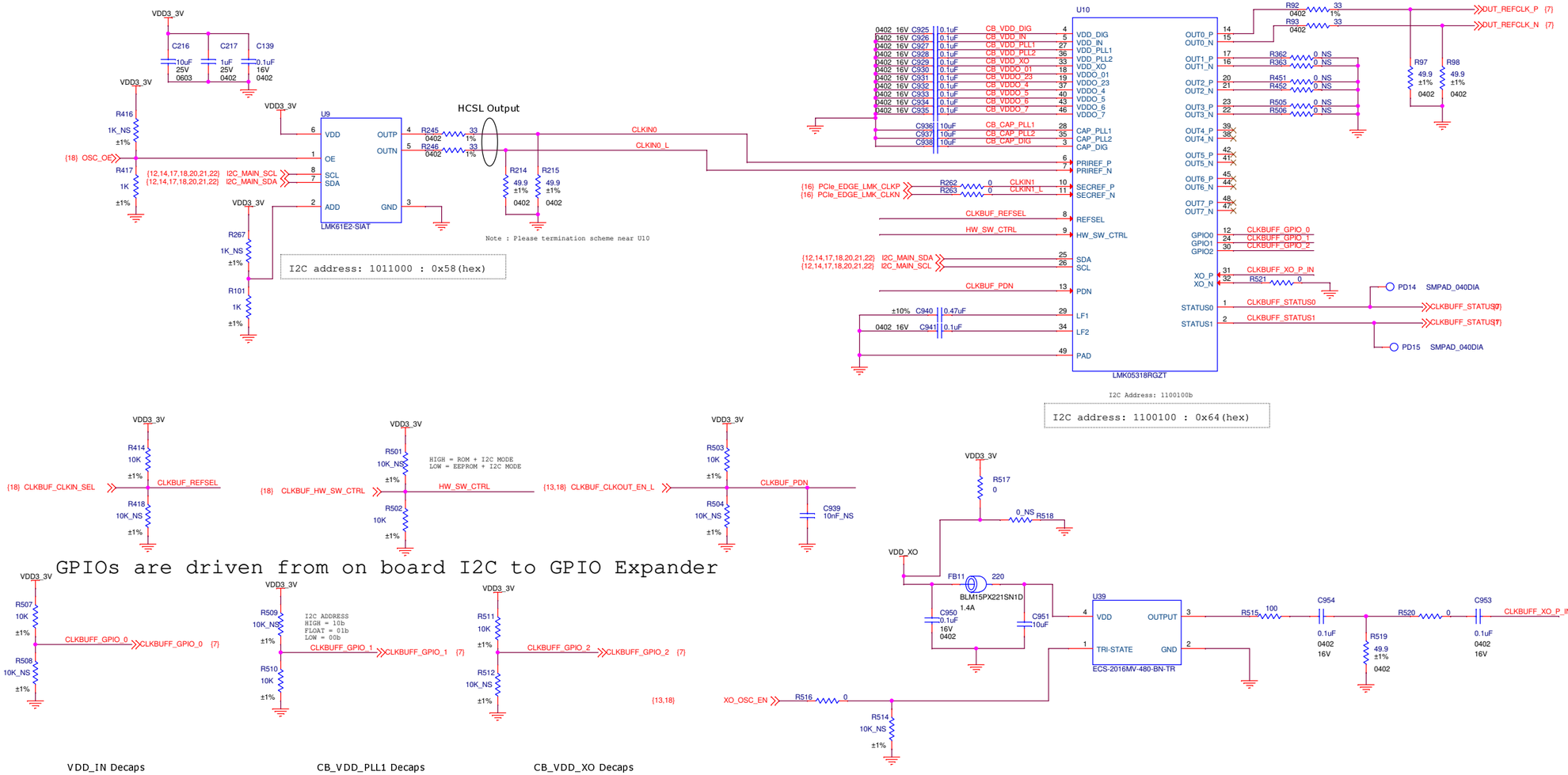
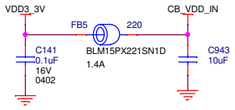
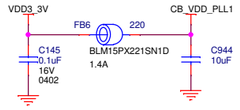
Clock Buffer



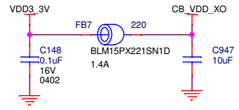
VDD_IN Decaps



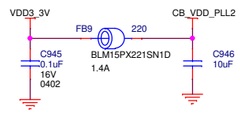
CB_VDD_PLL1 Decaps



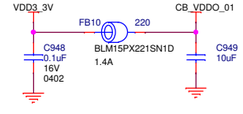
CB_VDD_XO Decaps



CB_VDD_PLL2 Decaps



CB_VDDO_01



VDD_DIG

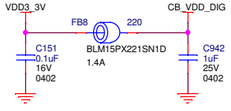


Table 1. Device Start-Up Modes

HW_SW_CTRL INPUT LEVEL (1)	START-UP MODE	MODE DESCRIPTION
0	EEPROM + I²C (Soft pin mode)	Registers are initialized from EEPROM, and I²C interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: I²C Data, I²C Clock (open drain) • **GPIO0/SYNCN**: Output SYNC Input (active low). Pull up externally if not used. • **GPIO1/SCS** (1): I²C Address LSB Select (Low = 00b, Float = 01b, High = 10b) • **GPIO2/SDO/FINC** (2): DPLL DCO Frequency Increment (active high) • **STATUS1/FDEC** (2): DPLL DCO Frequency Decrement (active high), or Status output
Float (V_{IM})	EEPROM + SPI (Soft pin mode)	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: SPI Data In (SDI), SPI Clock (SCK) • **GPIO0/SYNCN**: Output SYNC Input (active low). Pull up externally if not used. • **GPIO1/SCS**: SPI Chip Select (SCS) • **GPIO2/SDO/FINC**: SPI Data Out (SDO)
1	ROM + I²C (Hard pin mode)	Registers are initialized from the ROM page selected by GPIO pins, and I²C interface is enabled. Logic pins: • **SDA/SDI, SCL/SCK**: I²C Data, I²C Clock (open drain) • **GPIO[2:0]** (1): ROM Page Select Inputs (000b to 111b) during POR. • After POR, GPIO2/SDO/FINC and STATUS1/FDEC pins can function the same as for HW_SW_CTRL = 0.

(1) The input levels on these pins are sampled only during POR.
(2) FINC and FDEC pins are only available when DCO mode and GPIO pin control are enabled by registers.