**ADC clock configuration**

Procedure we followed

Step 1: Hardware reset

Step 2: Software reset

Step 3: Configured left ADC



Figure 1: Configuring ADC

Step 4: Configured the PLL



Figure 2: PLL configuration

Step 5: Probed the GPIO1 port



Observation:

GPIO1: dc voltage

WCLK: word clock remains in the same state as even without PLL, 44.1 KHz.

Moreover in the screenshot related to the configuration of PLL, its displayed at the bottom that, “loading this settings into the EVM may cause the USB audio to not work correctly” what does this imply. Kindly revert back.

Step 6:



GPIO1: ≈ 98 MHz

Captured data is depicted below



