How to Generate a Header File

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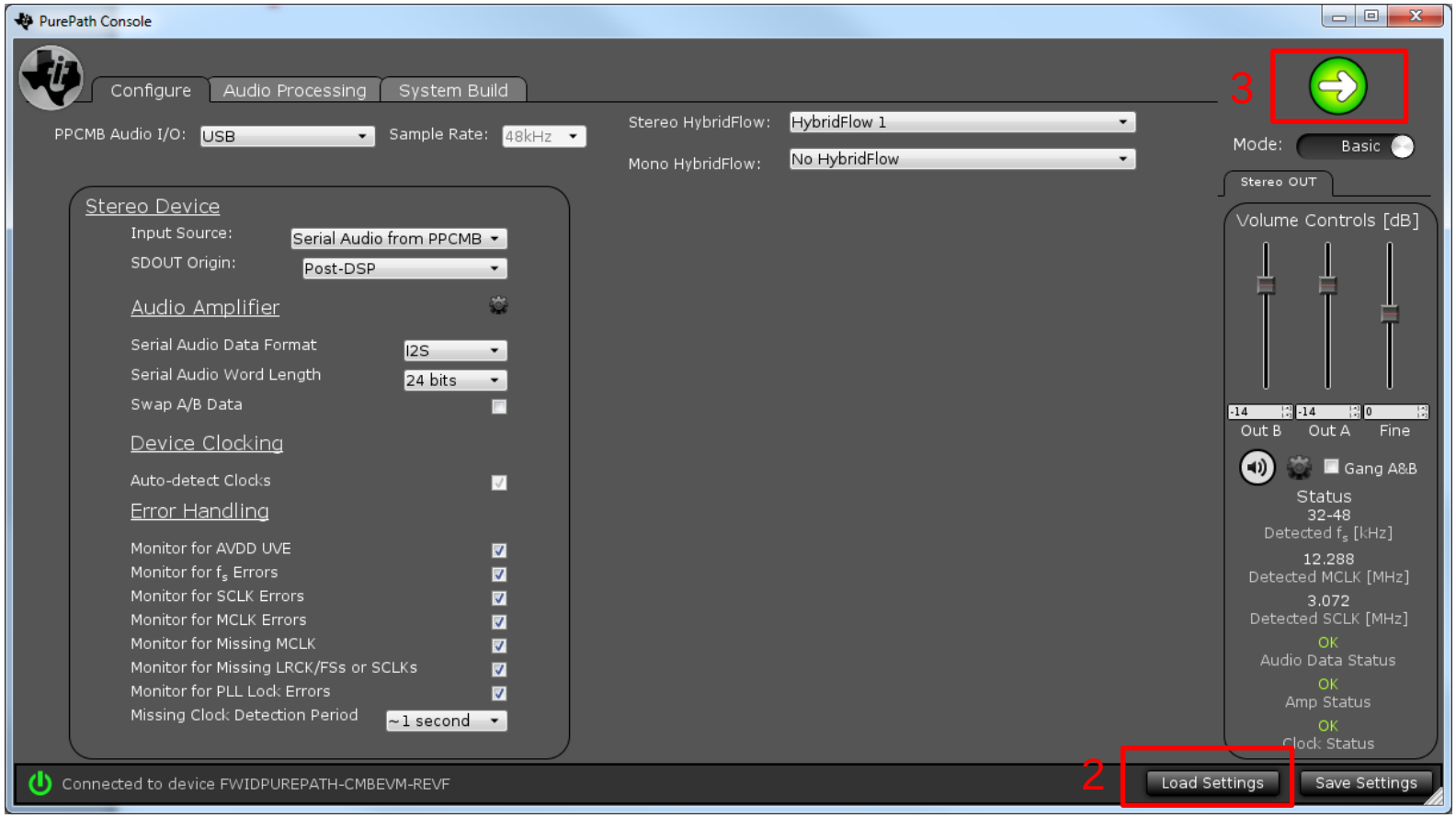
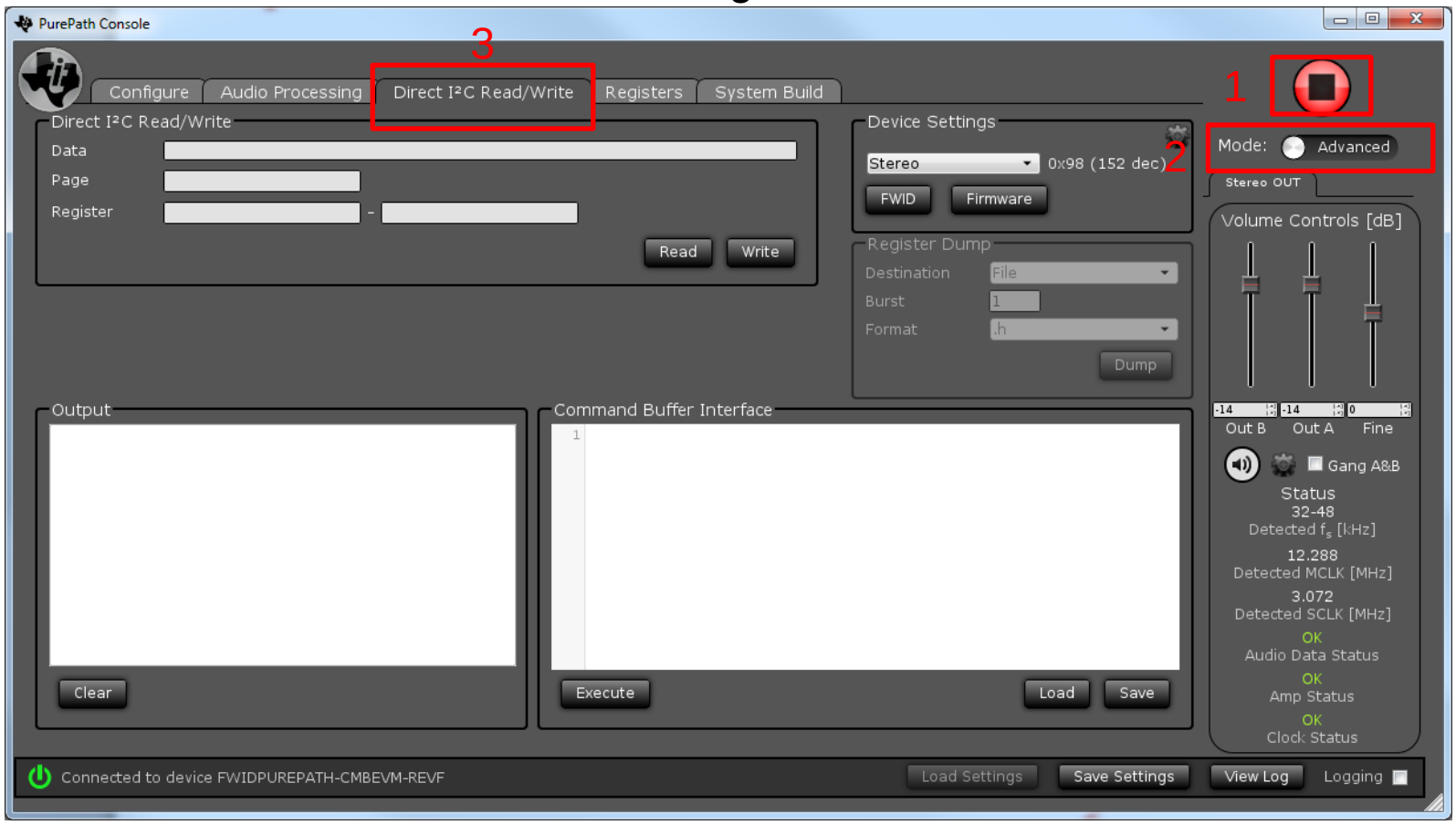
Step 1

1. Connect your PPCMB to a PC.
2. Launch PPC2 and load your tuning file(.xml).
3. Click the download button.



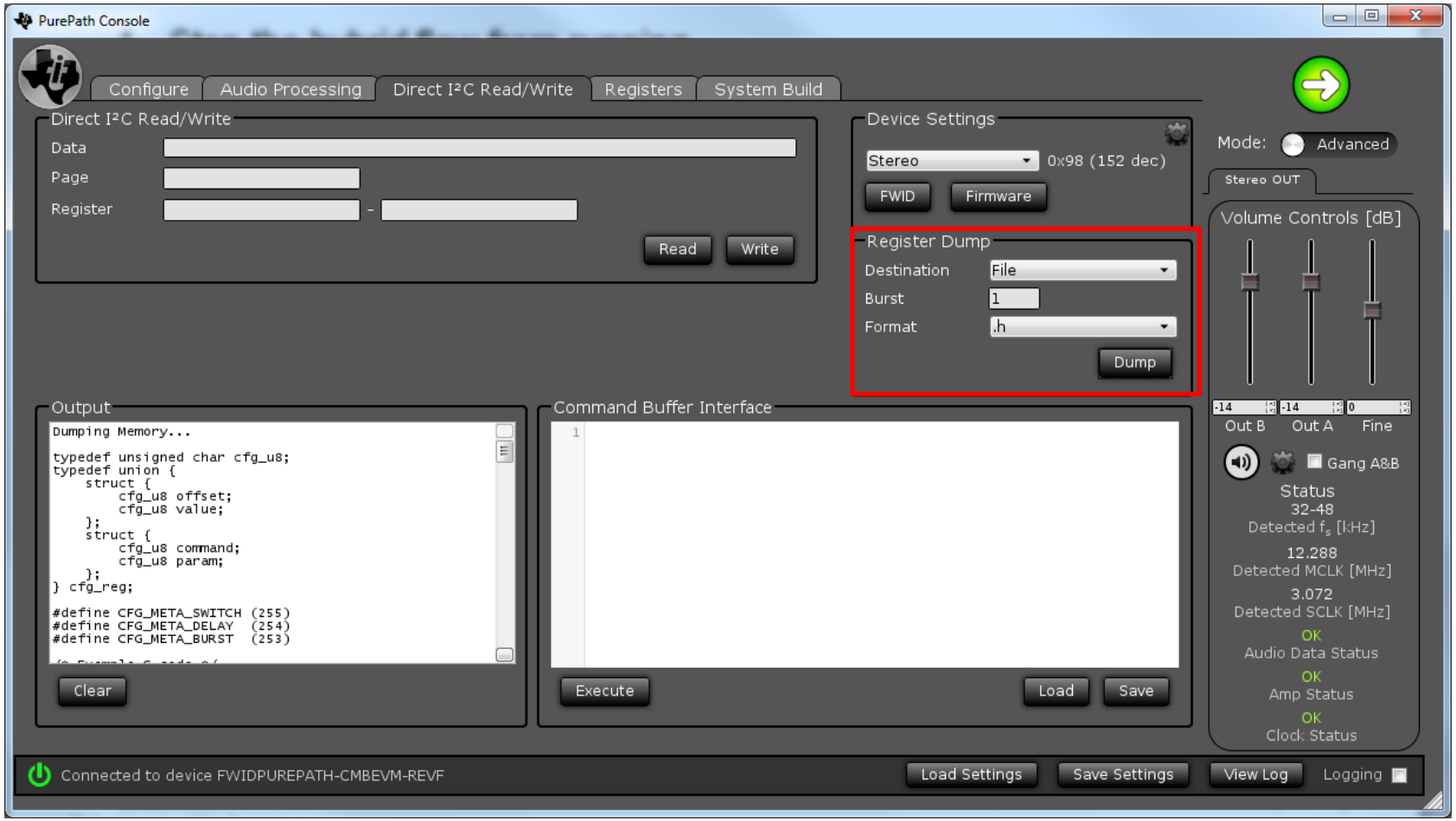
Step 2

1. Stop the HybridFlow from running.
2. Switch to Advanced mode.
3. Go to “Direct I2C Read / Write“ Page.



Step 3

1. Select the right destination, burst length and format in the Register Dump.
2. Click the Dump button to start dumping.



Step 4

1. Fix the P0-R42 value if it is set to 0x00.

HF1_burst1_fix.cfg

```
64 w 98 19 00
65 w 98 1a 80
66 w 98 1b 00
67 w 98 1c 00
68 w 98 1d 00
69 w 98 1e 00
70 w 98 1f 04
71 w 98 20 00
72 w 98 21 00
73 w 98 22 00
74 w 98 23 01
75 w 98 24 00
76 w 98 25 00
77 w 98 26 f3
78 w 98 27 04
79 w 98 28 02
80 w 98 29 00
81 #w 98 2a 00    #Anglog Mute
82 w 98 2a 11
83 w 98 2b 1f
84 w 98 2c 00
85 w 98 2d 00
86 w 98 2e 00
87 w 98 2f 00
```

hf1-burst1_fix.h

```
100     { 0x22, 0x00 },
101     { 0x23, 0x01 },
102     { 0x24, 0x00 },
103     { 0x25, 0x00 },
104     { 0x26, 0xf3 },
105     { 0x27, 0x04 },
106     { 0x28, 0x02 },
107     { 0x29, 0x00 },
108     /*{ 0x2a, 0x00 },  Ananlog Mute */
109     { 0x2a, 0x11 },
110     { 0x2b, 0x1f },
111     { 0x2c, 0x00 },
112     { 0x2d, 0x00 },
113     { 0x2e, 0x00 },
114     { 0x2f, 0x00 },
115     { 0x30, 0x00 },
116     { 0x31, 0x00 },
117     { 0x32, 0x00 },
118     { 0x33, 0x00 },
119     { 0x34, 0x00 },
120     { 0x35, 0x00 },
121     { 0x36, 0x00 },
122     { 0x37, 0x00 },
123     { 0x38, 0x00 },
```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P0-R3 and P0-R42(0x2a)

8.4.2.3 P0-R3

Mute Channel B [4] (R/W)	00000000
This bit issues soft mute request for the Channel B. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - 0 - - - -
Mute	- - - 1 - - - -
Mute Channel A [0] (R/W)	**00000000**
This bit issues soft mute request for the Channel A. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - - - - - 0
Mute	- - - - - - - 1

8.4.2.29 P0-R42

Channel B DAC Data Path [5:4] (R/W)	00000001
These bits control the Channel B audio data path connection.	
Zero data (mute)	- - 0 0 - - - -
Channel B data	- - 0 1 - - - -
Channel A data	- - 1 0 - - - -
Reserved (do not set)	- - 1 1 - - - -
Channel A DAC Data Path [1:0] (R/W)	**00000001**
These bits control the Channel A audio data path connection.	
Zero data (mute)	- - - - - - 0 0
Channel A data	- - - - - - 0 1
Channel B data	- - - - - - 1 0
Reserved (do not set)	- - - - - - 1 1

Register Page & Header File Structure

Register Page Structure

Register Page Structure

Page:	0	1	2-43	44-52	53-61	62-70	71-151	152-186
Func:	Control	Analog Control	Reserved	Coeffient A	Reserved	Coeffient B	Reserved	Instruction
Desc:	General Control and Configuration	Analog Control		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		1024 24-bit instructions, 30 instructions per page, 4 registers per instruction

Coefficient Buffer A & B Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	44	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	44	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C29	44	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	45	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C59	45	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	46	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C89	46	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	47	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C119	47	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	48	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C149	48	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	49	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C179	49	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	50	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C209	50	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	51	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C239	51	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	52	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C255	52	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Header / CFG File Structure

Content	Comment
	Put TAS5754M into standby mode and mute the device.
Page 0 -1	General control and analog control
Page 44 - 52	Coefficient A (C-RAM)
Page 62 - 70	Coefficient B (C-RAM)
Page 152 - 169	Instruction (I-RAM)
	Post-Initialization: Enable adaptive mode. Wake up and unmute the device.

C-RAM Access

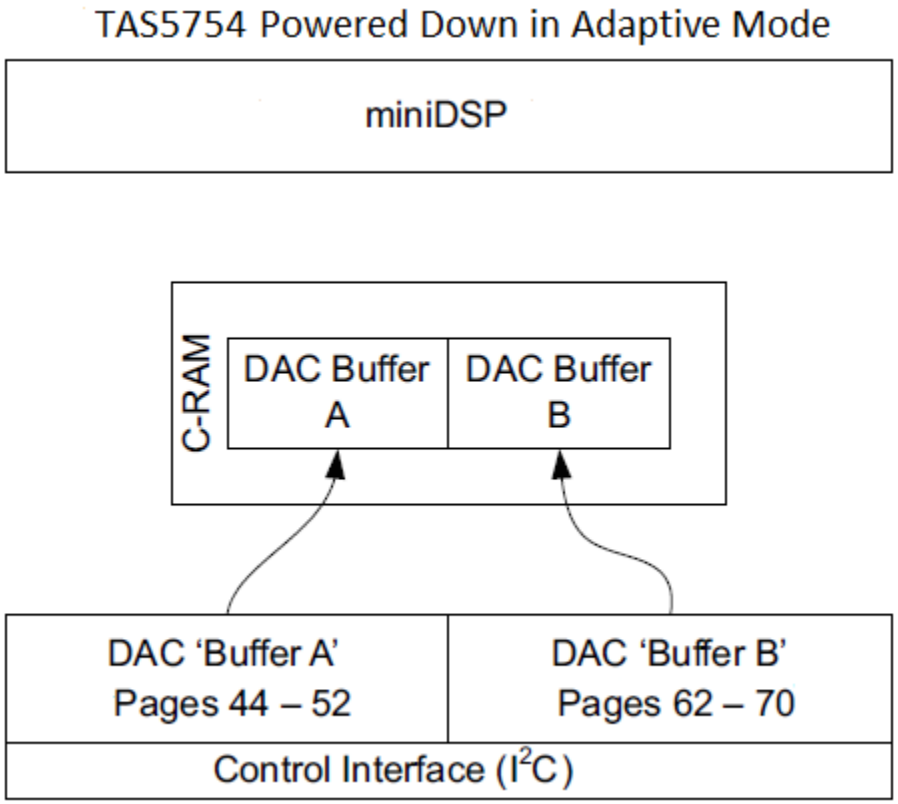
C-RAM Access

C-RAM Access Table – Adaptive

Status	miniDSP C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up (p44_r1_b1 = 0)	Buffer A only	Buffer B only
Powered Up (p44_r1_b1 = 1)	Buffer B only	Buffer A only

p44_r1_b1 is short for Page 44 / Register 1, Bit 1

C-RAM Access at Power-Down Mode



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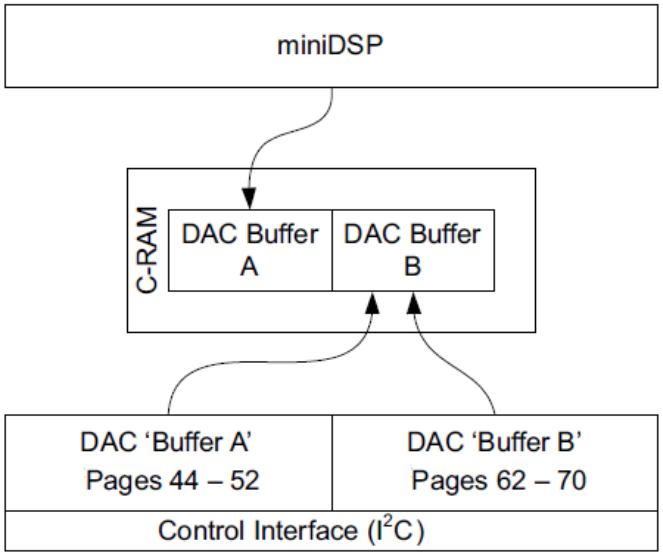
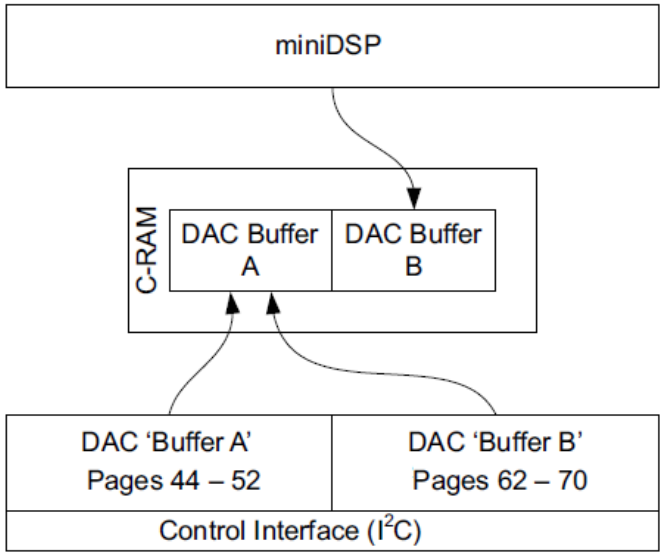
C-RAM Access at Power-Up Mode

TAS5754 Powered Up in Adaptive Mode (p44_r1_b1 = 0)



TAS5754 Powered Up in Adaptive Mode (p44_r1_b1 = 1)



Page 44 / Register 1 (Hex 0x01)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	0x01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Reset Value							0		0

ACRS	**Active CRAM Selection (Read Only)** This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I2C) 0: CRAM A is active and being used by the DSP 1: CRAM B is active and being used by the DSP
ACSW	**Switch Active CRAM** This bit is used to request switching roles of the two buffers, i.e. switching the active buffer role between CRAM A and CRAM B. This bit is cleared automatically when the switching process completed. Default value: 0 0: No switching requested or switching completed 1: Switching is being requested

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C-RAM Access (Adaptive Mode) Example