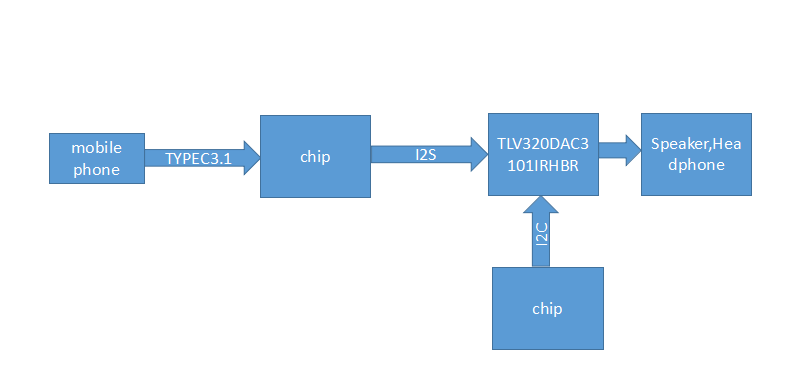
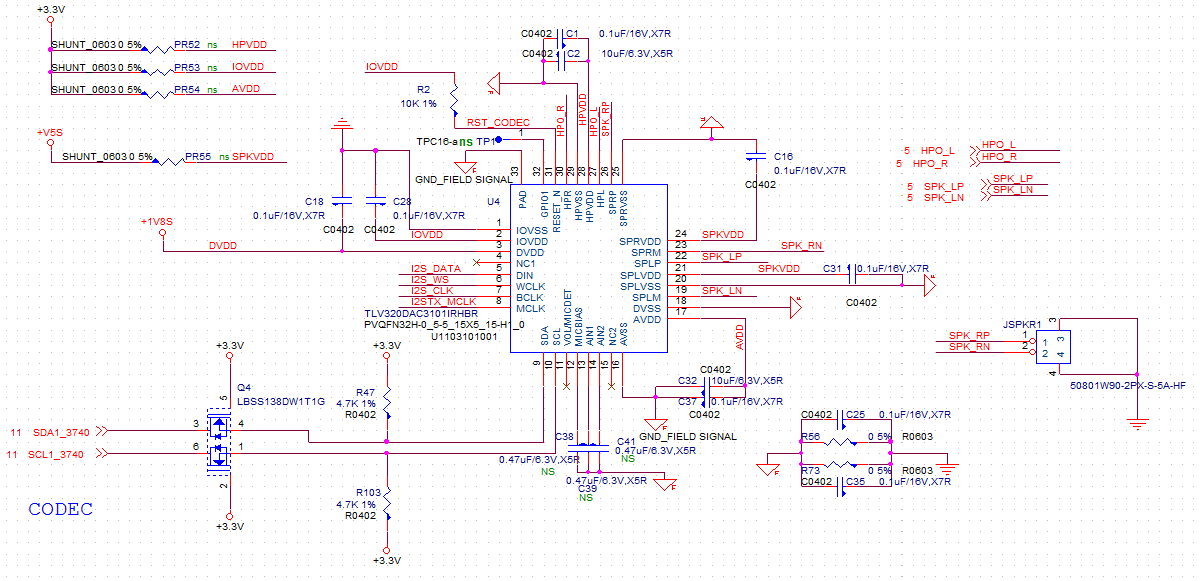
**Block diagram:**



**Sch:**



**I2C Initialization code**:

//page 0  
{ 0x00,Audio\_I2C\_W, 0x00 },//  
{ 0x01,Audio\_I2C\_W, 0x01 },//s/w reset  
{ 0x04,Audio\_I2C\_W, 0x07 },//PLL\_clkin = BCLK,codec\_clkin = PLL\_CLK  
{ 0x05,Audio\_I2C\_W, 0x94 },  
{ 0x06,Audio\_I2C\_W, 0x07 },  
{ 0x07,Audio\_I2C\_W, 0x00 },  
{ 0x08,Audio\_I2C\_W, 0x00 },  
{ 0x1B,Audio\_I2C\_W, 0x30 },//mode is i2s,wordlength is 16  
{ 0x1C,Audio\_I2C\_W, 0x00 },//Data-Slot Offset Programmability   
{ 0x1D,Audio\_I2C\_W, 0x00 },  
{ 0x1E,Audio\_I2C\_W, 0x00 },  
{ 0x0B,Audio\_I2C\_W, 0x82 },//NDAC is powered up and set to 2  
{ 0x0C,Audio\_I2C\_W, 0x87 },//MDAC is powered up and set to 7  
{ 0x0D,Audio\_I2C\_W, 0x00 },//DOSR = 128, DOSR(9:8) = 0  
{ 0x0E,Audio\_I2C\_W, 0x80 },//DOSR(7:0) = 128  
{ 0x74,Audio\_I2C\_W, 0x00 },//DAC => volume control thru pin disable   
{ 0x44,Audio\_I2C\_W, 0x00 },//DAC => drc disable, th and hy  
// { 0x41,Audio\_I2C\_W, 0x0A },// DAC => 0 db gain left  
// { 0x42,Audio\_I2C\_W, 0x0A },//DAC => 0 db gain right  
//page 1  
{ 0x00,Audio\_I2C\_W, 0x01 },  
{ 0x21,Audio\_I2C\_W, 0x4E },  
{ 0x1F,Audio\_I2C\_W, 0x06 }, //0xC6  
{ 0x23,Audio\_I2C\_W, 0x44 },  
{ 0x28,Audio\_I2C\_W, 0x06 },//Garlin\_2019092001-- 0x0E },  
{ 0x29,Audio\_I2C\_W, 0x06 },//Garlin\_2019092001-- 0x0E },  
{ 0x24,Audio\_I2C\_W, 0x00 },  
{ 0x25,Audio\_I2C\_W, 0x00 },  
{ 0x2E,Audio\_I2C\_W, 0x0B },  
// { 0x30,Audio\_I2C\_W, 0x40 },  
// { 0x31,Audio\_I2C\_W, 0x40 },  
//page 0  
{ 0x00,Audio\_I2C\_W, 0x00 },  
{ 0x3C,Audio\_I2C\_W, 0x17 }, // DAC Processing Block Selection  PRB\_P23  
//page 8  
{ 0x00,Audio\_I2C\_W, 0x08 },  
{ 0x01,Audio\_I2C\_W, 0x04 },  
//page 0  
{ 0x00,Audio\_I2C\_W, 0x00 },  
{ 0x3F,Audio\_I2C\_W, 0XD6 }, //Garlin\_2019093003-- 0xFE },  
{ 0x40,Audio\_I2C\_W, 0x00 },  
//page 1  
{ 0x00,Audio\_I2C\_W, 0x01 },  
{ 0x23,Audio\_I2C\_W, 0x08 },//44  
{ 0x23,Audio\_I2C\_W, 0x00 },//44  
{ 0x26,Audio\_I2C\_W, 0x00 }, //0xA1  
{ 0x27,Audio\_I2C\_W, 0x00 }, //0XA1  
{ 0x23,Audio\_I2C\_W, 0x40 },//44  
{ 0x23,Audio\_I2C\_W, 0x44 },//44  
{ 0x26,Audio\_I2C\_W, 0x00 }, //0xA1  
{ 0x27,Audio\_I2C\_W, 0x00 }, //0XA1  
{ 0x2A,Audio\_I2C\_W, 0x15 },//Garlin\_2019092001-- 0x0B },  
{ 0x2B,Audio\_I2C\_W, 0x15 },//Garlin\_2019092001-- 0x0B },  
//page 1  
{ 0x00,Audio\_I2C\_W, 0x01 },  
{ 0x2A,Audio\_I2C\_W, 0x0C },  
{ 0x2B,Audio\_I2C\_W, 0x0C },  
{ 0x20,Audio\_I2C\_W, 0xC6 },  
// { 0x24,Audio\_I2C\_W, 0x30 },  
// { 0x25,Audio\_I2C\_W, 0x30 },  
// { 0x31,Audio\_I2C\_W, 0x00 },