Agenda

- Background
- Layout considerations
- System board requirements
- Add-in card designs
- Signal validations
- Summary
Bus Topology Evolution

- **PCI common clock**
  - Meet setup/hold timing
  - Multi-drop parallel I/O

- **AGP source synchronous**
  - Single strobe, multiple data
  - Match all data to strobes

- **PCI Express serial differential**
  - Embedded clock
  - Point-to-point, match per data pair only
  - Longer route, creative device placement

**PCI Express pt-to-pt routing is straightforward**
Serial Differential Signal

- **Diff pairs**
- **AC coupled**
- **Lane-to-lane de-skew**
- **Polarity inversion**
- **On-chip equalization (de-emphasis)**
- **On-chip terminations**

**System board**

**TX Spec**

- 0.7 UI
- 800 mV

**RX Spec**

- 0.4 UI
- 175 mV

**Interconnect Loss** < 13.2 dB

**Jitter** < 0.3 UI

**TX Eye** shown without de-emphasis

UI = Unit Interval = 400ps
PCI Express Routing

- Trace length matching between pairs is not required
  - Embedded clock simplifies routing rules

- Longer motherboard traces
  - 12+ inches possible

- TX pairs usually route on top layer
  - AC coupling caps on TX traces on system board

AC Coupling Caps
PCI Express x16 Connector
Trace Serpentines Not Required
Interconnect Budget

- Loss and jitter are key parameters
- Target impedance not as critical
- Maintain differential pair symmetry
- Design tradeoffs: loss vs. trace length, etc.

Recommended Solution Space:
- System board traces:
  - Up to 12 inches
- Add-in card traces:
  - Up to 3.5 inches
- Chip-to-chip routes:
  - System board traces:
    - Up to 15 inches

Manage loss and jitter to meet budget
Stackup Design

- No new PCB technology required
- Standard 4-layer stackup 0.062” thick PCB
- Microstrip ½ oz Cu plated
  - OR -
- Stripline 1 oz Cu (6+ layers)

Follow simple layout rules & design tradeoffs

Nominal 4-layer Stackup Geometries

Follow simple layout rules & design tradeoffs

T = ~62 mils
Trace Geometry & Impedance

- Wide pair-to-pair spacing ⇒ minimize crosstalk
  - “Close” intra-pair spacing
- Same geometry for interleaved/non-interleaved
- Example impedance targets:
  - Single-end $Z_0$ of 60 Ω ±15%
  - Differential Impedance of ~100 Ω ±20%

Non-interleaved topology example

Interleaved topology example
FR4 Loss Considerations

- Stackup: FR4 material
  - Narrow traces $\Rightarrow$ loss $\uparrow$
  - Copper roughness $\Rightarrow$ loss $\uparrow$
  - Dielectrics with more resin material $\Rightarrow$ loss $\uparrow$

- Non-homogeneous dielectrics
  - Localized Zo variation due to material weave $\Rightarrow$ loss $\uparrow$

- Wide differential impedance variation on $\mu$strip traces
  - Etching and plating process $\Rightarrow$ loss $\uparrow$
Trace Length

- Longer trace length ⇒ loss ↑
  - ~0.25 to 0.35 dB inherent loss per inch for FR4 microstrip traces at 1.25GHz
- Manage trace lengths to minimize loss
  - Example: 12” board, 3.5” add-in card lengths

Example VNA measurements for differential microstrip trace insertion loss

Example: 20-inch line, 1.25GHz, -5.23dB
Trace Symmetry & Matching

- No matching needed pair-to-pair
- Match each differential pair per segment
  - Match overall length $\leq$ 5 mils (recommended)
  - Symmetric routing for each pair

Match near mismatch

Preferred matching

$\leq$ 45 mils

Alternative matching
Bends and Small Serpentines

- Avoid tight bends
  - No 90° bends; impact to loss and jitter budgets
- Keep angles $\geq 135^\circ$ ($\alpha$)
- Maintain adequate air gap
  - $A \geq 4x$ the trace width
- Lengths of $B$, $C \geq 1.5x$ the width of the trace
- Serpentines length is at least $3w$ for jog
Package Pin Field Breakout

- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends

Diagram:
- Side-by-side: Best
- Adjacent w/ small serpentine: OK
- Adjacent w/ bend: Fair
- Diagonal routing: Fair
Reference Plane

- Full GND plane reference recommended
- Stitching vias required for layer transition
- Keep clearance from plane voids
- Avoid plane splits
- Avoid trace over anti-pad

Layout considerations

Plane Void

Long trace routes

Gnd stitching via
AC Coupling Caps

- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement best

- Cap size: 0.1uF best
- Same sizes for both D+/D-
- Cap location:
  - Along Tx pairs on system board
  - Along Tx pairs on add-in card
Test Points & Vias

- Minimize via usage
  - Up to 0.25 dB loss per via
  - Use via pad size ≤ 25 mil, hole size ≤ 14 mil; standard anti-pad size of 35 mil
- Put test points or LAI pads in series (if used)
  - No stubs
  - Place symmetrically
  - Provide GND pads for single-ended probing

![Diagram of LAI, Probe, and GND pads]
Reference Clock

- Clocks have no phase relationships
  - Length matching for clocks is *NOT* required!
- Deliver diff clock to each device and connector
  - Use same trace geometries as other diff pairs
- **Clock driver requirements:**
  - 100MHz with SSC support (e.g. CK410)
  - System board (source) termination only
  - Rise/fall slew rate requirements need to be met

![Diagram of Reference Clock System Board Requirements](image)

- **System board requirements**
- **Clock Driver Requirements**
  - 100MHz with SSC support (e.g. CK410)
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### System Board Requirements

- **L1**
- **L1'**
- **L2**
- **L2'**
- **L3**
- **L3'**
- **L4**
- **L4'**
- **L5**
- **L5'**

- **Rs**
- **Rt**

- **22 - 33Ω ±5%**
- **0.5” max**
- **0 – 0.2”**
- **49.9Ω ±1%**
- **0.5” – 3.5”**
- **1” – 14”**
- **PCI Express Connector**
- **PCI Express Card**
Connector Layout

- Connector with standard PTH
  - Connector sizes: x1, x4, x8, x16
  - Pinout optimized for differential routing & crosstalk reduction
  - Polarity inversion allowed

- Loss & crosstalk part of system board budget

Improved PTH connector for PCI Express
Power Rails

- Increased current capability for x16 connector
  - Additional +12V pin; 1.1 Amp per pin capability
- Helpful grouping of power supply pins
  - Eases power delivery routing
- ATX power supply connector
  - 2x12 (recommended)

### Power Rail Specifications

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>x16 Connector Spec</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>+3.3V</strong></td>
<td>± 9% (max) 3.0 A (max)</td>
</tr>
<tr>
<td>Voltage Tolerance</td>
<td>Current</td>
</tr>
<tr>
<td><strong>+12V</strong></td>
<td>± 8% (max) 5.5A (max)</td>
</tr>
<tr>
<td>Voltage Tolerance</td>
<td>Current</td>
</tr>
<tr>
<td><strong>+3.3Vaux</strong></td>
<td>± 9% (max) 375 mA (max)</td>
</tr>
<tr>
<td>Voltage Tolerance: Wake Non-Wake</td>
<td>Current</td>
</tr>
</tbody>
</table>
PCI Express introduces a spec for **75W cards**

- Available for x16 connectors
- Allows for performance graphics cards
- 75W can be fully drawn thru x16 connector
- Note: ≤ 25W at initial power-up
  (75W after configuration as a high power device)

**Up to 25W allowed** for x1,x4,x8 cards

<table>
<thead>
<tr>
<th>Connector Size</th>
<th>Power Consumption Allowances</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>x4/x8</td>
</tr>
<tr>
<td>Standard height</td>
<td>10 W (^1) (max)</td>
</tr>
<tr>
<td>Low profile card</td>
<td>10 W (max)</td>
</tr>
</tbody>
</table>

1. Max at initial power-up only.

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PCI Express spec support for 75W cards
Power Delivery - 75W Support

- Ensure +3.3V & +12V tolerances at add-in card
- Max of 2%~3% MB +12V voltage drop (e.g. 360mV)
  - Typical power supply = ± 5% drop
  - Balance trace width vs. length
  - Example: 100 mils min trace width, = 12” length for +12V with 1oz Cu
- Proper power decoupling
  - Max current slew rate of 0.1A/µs
  - Suppress high freq coupling noise
  - Tune capacitor type/location to board needs

Example uATX +12V layout
2x12 Power Supply Connector
Thermal & Acoustic Management

- Platforms need to deliver cool air to x16 slot
  - Use side panel vents, ducting
  - 75W card recommendation: $\leq 55^\circ C$ air temp at graphics card fan intake
  - Use larger fans for better acoustics
Card Edge Fingers

- Remove ref plane under edge finger pads
  ✓ Better impedance match

- PRSNT1#, PRSNT2# Pins
  ✓ 1mm shorter: last-mate, first break Hot-Plug support
  ✓ Multiple PRSNT2# pins (x4,x8,x16 cards)
  ✓ Cards must strap PRSNT1# with furthest PRSNT2# signal
  ✓ *System board Hot-Plug support optional*
Card Retention

- Card allows for chassis & system board-based retention
  - Fixed card height & keep outs
  - “Hockey-stick” near edge fingers
- PCI-SIG* design guideline for retention solution
  - Clip for system board, card “hockey-stick”
  - Supports up to 350g for 75W cards
- OEMs free to innovate independent solutions

Hockey-Stick Retention Mechanism

Requires two, 80-mil diameter holes
Card Physical Dimensions

**End bracket**

Top edge keep out and fixed height to enable chassis level retention solutions

“Hockey-stick” to allow for new retention solutions

Fixed height for I/O cards
(allowance for low profile compliance)
Gfx Thermal & Acoustic

- Limit heat re-circulated thru Gfx card heat sink
  - Use shroud to separate fan intake and heat sink exhaust
  - Place fan intake near air source - direct away the exhaust
  - Reduce fan noise and low speed chatter
  - Use diode and/or thermister for fan speed control

![Diagram showing airflow and components]

- cool air source (e.g. from chassis vent)
Lab Signal Measurements

- PCI Express devices generate compliance pattern per spec
- Use compliance boards for signal validation
  - Compliance Base Board (CBB) for add-in card measurements
  - Compliance Load Board (CLB) for system board measurements
- Measure eye diagrams with real time scope
  - 6+ GHz analog bandwidth
  - 20+ Gs sampling bandwidth
  - Scope vendor should have eye diagram signal analysis SW tool
Acquiring & Interpreting Results

- **Probe locations**
  - Tx Signals: measure at 50Ω loads
  - Rx Signals: measure at package input pins

- **Scope post-processing software**
  - Create transition bit eye
  - Create de-emphasized eye

- **Determine:**
  - Max jitter
  - Min eye voltage margin (high/low)
  - Max AC common mode voltage

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**Validate eye diagrams using real time scope**
Summary

- PCI Express point-to-point layout is straightforward
- Manage loss and jitter from PCB to meet interconnect budget
- Follow basic layout rules and design tradeoffs to implement typical topologies
- Improved connector & add-in card features - support for 75 Watt cards
- Validate compliance eye diagrams using compliance boards and real time scope
Collateral

- For additional and updated information on PCI Express Architecture, visit
  
  http://www.pcisig.com
Thank you for attending the 2004 PCI-SIG Asia-Pacific Developers Conference.

For more information please go to www.pcisig.com