Maximizing GSPS ADC SFDR Performance: Sources of Spurs and Methods of Mitigation

Marjorie Plisch

Applications Engineer, Signal Path Solutions
Outline

• Overview of the issue
• Sources of spurs
• Methods of mitigation
• Summary and recommendations
AN OVERVIEW OF THE ISSUE
Problem statement

How to minimize spurs in the GSPS ADC family in order to maximize SFDR performance?
ADC Sampling Rate and Architecture

- The absolute rate of what “low” or “high” is, changes as process technology advances.
- Higher sampling rate architectures imply lower resolutions.
- Certain techniques may be applied to the basic flash architecture in order to improve its performance.
Ultra high-speed architecture design (2)

- Basic Flash Architecture
  - Can achieve high sampling rates with low conversion latency
  - Basic design requires $2^N$ comparators and latches
  - Drawbacks are high power consumption, die area

- What techniques can make a 12-bit 3.6 GSPS ADC practically realizable?
  - Folding and interpolating to improve power consumption, reduce area

Flash ADC Implementation

# GSPS ADC Functional Blocks

<table>
<thead>
<tr>
<th>Block</th>
<th>Description</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Track-and-hold</td>
<td>Track and hold analog input signal</td>
<td>Improve performance at low Fin</td>
<td>Can reduce max sampling rate</td>
</tr>
<tr>
<td>Folding</td>
<td>Fold transfer function into sub-ranges</td>
<td>Reduce number of latches to improve power, area</td>
<td>Introduces distortion</td>
</tr>
<tr>
<td>Interpolating</td>
<td>Interpolate conversion between series of amplifiers</td>
<td>Reduce number of amplifiers to improve power, area</td>
<td>Introduces distortion</td>
</tr>
<tr>
<td>Interleaving</td>
<td>Time-interleave multiple ADC cores</td>
<td>Achieve higher sampling rates</td>
<td>Introduce distortion from mismatch factors</td>
</tr>
<tr>
<td>Calibrating</td>
<td>Trim bias currents in linear amplifiers</td>
<td>Reduces distortion</td>
<td>Time off-line to calibrate</td>
</tr>
</tbody>
</table>

For more details on the GSPS ADC architecture, see “A 1.8V 1.0Gsps 10b Self-Calibrating Unified-Folding-Interpolating ADC with 9.1 ENOB at Nyquist Frequency” by R. Taft, et al. ISSCC 2009 / Session 4 / High-speed Data Converters.
SOURCES OF SPURS
Harmonic Distortion in an Amplifier

• What are the harmonic distortion terms for an amplifier? First, let us consider the non-linear system:

\[ v_o(t) = a_1v_{in}(t) + a_2v_{in}^2(t) + a_3v_{in}^3(t) + a_4v_{in}^4(t) + a_5v_{in}^5(t) + \ldots \]

• For differential circuits, the even harmonics are ideally zero and \( H_3 \gg H_5 \), so we can approximate:

\[ v_o(t) \approx a_1v_{in}(t) + a_3v_{in}^3(t) \]

• For a sinusoidal input: \( v_{in}(t) = A\cos(\omega t) \)

\[ v_o(t) = a_1A\cos(\omega t) + a_3A^3\cos^3(\omega t) \]

\[ = [a_1A + \frac{3a_3A^3}{4}]\cos(\omega t) + \frac{a_3A^3}{4}\cos(3\omega t) \]

\[ HD_1 \quad \quad \quad HD_3 \]

• If we define: \( v_o(t) \equiv HD_1\cos(\omega t) + HD_3\cos(3\omega t) \)

\[ HD_1 = a_1A \quad \text{and} \quad HD_3 = \frac{a_3A^3}{4} \]

**Example:**
For a classic non-linear amplifier, if the input level, \( A \), is decreased by 1dB, then \( HD_3 \) decreases by 3dB since \( HD_1 \) is proportional to \( A \) and \( HD_3 \) is proportional to \( A^3 \).
Harmonic Distortion due to Non-Linearity

- Harmonic distortion contribution from all sources sum at ADC output
- Distortion location is easy to predict, but amplitude is not

<table>
<thead>
<tr>
<th>Source of Distortion</th>
<th>Harmonics Produced</th>
<th>Rolls off with</th>
<th>Relationship to input power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Track-and-hold</td>
<td>Lower order harmonics</td>
<td>Analog input bandwidth</td>
<td>Classic relationship</td>
</tr>
<tr>
<td>Amplifiers in interpolating, folding architecture</td>
<td>Higher order harmonics</td>
<td>Folding-interpolating factor</td>
<td>Non-linear relationship</td>
</tr>
</tbody>
</table>
E.g.: Harmonic Distortion

**ADC12D800RF**
*(Folding-interpolating)*

**ADS5400**
*(Pipeline)*

Blue = original data  
Red = data with harmonics removed

- **Fundamental**
- **H₂**
- **H₃**
- **Noise Floor**
E.g.: ADC12D1600RF Harmonic Levels

- $H_3$ is generally the highest level harmonic
- Lower index harmonics from the track-and-hold roll off with input bandwidth
- Higher index harmonics from the folding-interpolating architecture remain present and have highly non-linear level
- A reduction in the input level is not strongly related to the harmonics level
ADC Interleaving Basics

- Multiple ADC cores sample signal to increase total sampling rate
- ADC cores sample at same divided frequency but different phase offset
- Digital outputs are re-aligned in time
- Input buffer typically drives cores
Non-Ideal Interleaving

• Offset Errors
  – Mismatched ADC core voltage offset

• Amplitude Errors
  – ADC core gain error
  – ADC reference voltage error

• Phase Errors
  – Input routing delay
  – Input BW difference
  – Clock phase error
  – ADC sampling instant
Non-Ideal Interleaving

- **Offset Error**
  - Different voltage offset at ADC input between different cores

- Alternating up/down in transient waveform

- Creates signal independent spurs in spectrum at $F_s*n/N$ for $n=1,2,…,N-1$ where $N$ is # of interleaved cores

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**Example N=4**

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**Example N=2**

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Non-Ideal Interleaving

- Amplitude and Phase errors
  - Gain difference between different cores
  - BW differences or transmission length differences result in phase difference
- Creates N-1 input signal dependent images from 0 to Fs/2 in a repetitive, mirror-image pattern where N is # of interleaved cores
- Also creates harmonic distortion images

\[
\begin{align*}
\text{Input Signal} & \quad \rightarrow \quad \text{Input Images} \\
\text{H2 Images} & \quad \rightarrow \quad \text{H2 Images}
\end{align*}
\]

Example N=4
E.g.: ADC12D1800RF DES Mode
Interleaving Spurs

4x Interleaving Spurs

Harmonic 2: -72.707 dBFS
Harmonic 3: -66.398 dBFS
Harmonic 4: -79.406 dBFS
Harmonic 5: -75.408 dBFS
Harmonic 6: -74.733 dBFS
# Interleaving by Product

<table>
<thead>
<tr>
<th>Product</th>
<th>Number of sub-converters in Non-DES Mode</th>
<th>Number of sub-converters in DES Mode</th>
<th>Non-DES Mode Offset Spur Locations</th>
<th>DES Mode Offset Spur Locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC10D1x00</td>
<td>2</td>
<td>4</td>
<td>DC, Fs/2</td>
<td>DC, Fs/4, Fs/2</td>
</tr>
<tr>
<td>ADC12D1x00</td>
<td>2</td>
<td>4</td>
<td>DC, Fs/2</td>
<td>DC, Fs/4, Fs/2</td>
</tr>
<tr>
<td>ADC12Dx00RF</td>
<td>1</td>
<td>2</td>
<td>DC</td>
<td>DC, Fs/2</td>
</tr>
<tr>
<td>ADC12Dxx00RF</td>
<td>2</td>
<td>4</td>
<td>DC, Fs/2</td>
<td>DC, Fs/4, Fs/2</td>
</tr>
</tbody>
</table>

- Dual-channel mode is “Non-DES Mode”; interleaved mode is “DES Mode.”
- The ADC12D800/500RF offer the possibility of one sub-converter per bank in Non-DES Mode.
E.g.: ADC12D1000RF Harmonic Distortion Interleaved

- Note the symmetrical appearance of the spurs around Fs/4 due to the 2x interleaving

FFT Details:
- ADC12D1800RF
- Non-DES Mode
- 2x interleaving
- NDM DDR clock
- Ain = 124.47MHz at -1dBFS
• Although there are 4 3rd order inter-modulation distortion products, only the 2 near-in ones are typically considered for an ADC: $2f_2 - f_1$ and $2f_1 - f_2$.

• The amplitude of the fundamentals, $f_1$ and $f_2$, should be set:
  – At, but not above -7dBFS
  – As close to each other as possible, preferably <0.1dB

• The difference between $f_1$ and $f_2$ in the diagram is exaggerated to show which is chosen to measure IMD$_3$.

\[ IMD_3 = \min(f_1, f_2) - \max(f_2 - f_1, f_1 - f_2) \]
E.g. ADC12D1800RF IMD$_3$
## DCLK Spur

<table>
<thead>
<tr>
<th>Product</th>
<th>NDM SDR DCLK (MHz)</th>
<th>NDM DDR DCLK (MHz)</th>
<th>Demux SDR DCLK (MHz)</th>
<th>Demux DDR DCLK (MHz)</th>
<th>DES Mode Spur Locations</th>
<th>Non-DES Mode Spur Locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC10D1500</td>
<td>N/A</td>
<td>500</td>
<td>N/A</td>
<td>250</td>
<td>N/A</td>
<td>Fs/4</td>
</tr>
<tr>
<td>ADC12D1800</td>
<td>N/A</td>
<td>900</td>
<td>N/A</td>
<td>450</td>
<td>N/A</td>
<td>Fs/4</td>
</tr>
<tr>
<td>ADC12D800RF</td>
<td>800</td>
<td>400</td>
<td>400</td>
<td>N/A</td>
<td>Fs/2</td>
<td>Fs/2</td>
</tr>
<tr>
<td>ADC12D1800RF</td>
<td>N/A</td>
<td>900</td>
<td>N/A</td>
<td>450</td>
<td>Fs/4</td>
<td>N/A</td>
</tr>
</tbody>
</table>

• Depending upon the mode, the Data Clock (DCLK) can couple back into the analog circuitry to appear in the output.
## Sub-converter Clock Spur

<table>
<thead>
<tr>
<th>Product</th>
<th>Fclk (MHz)</th>
<th>Sub-converters / Channel</th>
<th>Sub-converter Clock (MHz)</th>
<th>DES Mode Spur Location</th>
<th>Non-DES Mode Spur Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC1xDxxxxx</td>
<td>Fclk</td>
<td>N</td>
<td>Fclk / N</td>
<td>Fs / (2*N)</td>
<td>Fs / N</td>
</tr>
<tr>
<td>ADC12D1800RF</td>
<td>1800</td>
<td>2</td>
<td>900</td>
<td>Fs / 4</td>
<td>Fs / 2</td>
</tr>
<tr>
<td>ADC12D500RF</td>
<td>500</td>
<td>1</td>
<td>500</td>
<td>Fs / 2</td>
<td>Fs = DC</td>
</tr>
</tbody>
</table>

ADC12D1800RF, DES Mode, No Fin

Fs/4 = -75dBFS

[Diagram of sub-converter clock spur]
Spur Source Summary and Conclusions

• Spur sources
  – Non-linearities from the track-and-hold
  – Non-linearities from the folding-interpolating architecture
  – Interleaving images from gain mismatch and timing skew
  – Fixed frequency spurs: DCLK, offset mismatch in interleaving, sub-converter clock

• Conclusions
  – Testing with single tone inputs is the traditional method for assessing the non-linear performance of an ADC, but…
  – It may not be adequate or relevant for most real world applications
  – The next section illustrates how some non-linearities discussed in this section are either mitigated or reduced based on input signal type
METHODS OF MITIGATION
Calibration

- Calibration is the primary way to address spurs due to non-linearities in the conversion process.

- A foreground calibration addresses the following:
  - (1) trim the analog input resistance
  - (2) trim amplifier bias currents

- Minimize full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance.
Before-and-After Calibration

ADC12D1800RF Fin = 997.47MHz Non-DESI Mode

Without Calibration
ENOB = 6.62

With Calibration
ENOB = 8.85
Dithering to Improve Harmonics

- Adding dither or band-limited noise improves harmonic performance

E.g. ADC12D1800RF   Ain=-13dBFS

<table>
<thead>
<tr>
<th>Harmonic</th>
<th>No Dither (dBc)</th>
<th>With Dither (dBc)</th>
<th>Improvement (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H2</td>
<td>-65</td>
<td>-70</td>
<td>5</td>
</tr>
<tr>
<td>H3</td>
<td>-64</td>
<td>-74</td>
<td>10</td>
</tr>
<tr>
<td>H4</td>
<td>-77</td>
<td>-77</td>
<td>0</td>
</tr>
<tr>
<td>H5</td>
<td>-70</td>
<td>-75</td>
<td>5</td>
</tr>
<tr>
<td>H6</td>
<td>-67</td>
<td>-77</td>
<td>10</td>
</tr>
<tr>
<td>H7</td>
<td>-66</td>
<td>-78</td>
<td>12</td>
</tr>
</tbody>
</table>
Wideband Input Signals behave like dither

- In an application with wideband input signals, each signal will act as “dither” on the others and improve its harmonics.

- Noise Power Ratio (NPR) can be used to measure how quiet one unused channel in a wideband system remains in the presence of occupied channels.

\[
NPR = 10 \times \log_{10} \left( \frac{P_{Ni}}{P_{No}} \right)
\]
Frequency Planning

- Frequency planning can be used to make sure lower order harmonics do not interfere with the desired signal.

- The **ADC Harmonic Calculator** can be found at the link below.

- Please note that this tool does not yet include the effects of interleaved harmonics.

http://www.ti.com/lstpd/ti/analog/dataconverters/tools.page
Analog Correction of Interleaving Spurs

- Example: Using the DES Timing Adjust on the ADC12D1800RF to adjust the level of the interleaving spur at Fs/2-Fin.

- At its relative minimum, the power in the spur is due to gain mismatch between the I/Q-channel.

<table>
<thead>
<tr>
<th>GSPS ADC Feature</th>
<th>DES Mode Spur Addressed</th>
<th>Spur Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/Q-ch Offset Adjust</td>
<td>Fs/2</td>
<td>I/Q-ch offset mismatch</td>
</tr>
<tr>
<td>I/Q-ch FSR Adjust</td>
<td>Fs/2 - Fin</td>
<td>I/Q-ch gain mismatch</td>
</tr>
<tr>
<td>Duty Cycle Correct</td>
<td>Fs/2 - Fin</td>
<td>I/Q-ch timing skew</td>
</tr>
<tr>
<td>DES Timing Adjust</td>
<td>Fs/2 - Fin</td>
<td>I/Q-ch timing skew</td>
</tr>
</tbody>
</table>
Digital Correction of Interleaving Spurs

- Interleave correction reduces spectrum offset spurs and images
- Dithering does not affect the level of interleaving spurs
- Correction in analog/digital domain
  - For resolution > 8 bits, achieving the level of matching required in the analog domain is extremely difficult
- Digital correction: *estimate* the errors and *correct* the data with coefficients
- Estimation
  - Detection in time-domain or frequency domain
  - Convergence
- Calibration time
  - Foreground: Calibration interrupts normal operation
  - Background: Calibration runs continuously
Reducing Fixed Frequency Spurs

• Fixed frequency spurs occur from the DCLK, offset mismatch, and sub-converter clock

• Example solutions include DCLK Mode choice, system architecture choices, and ADC selection

<table>
<thead>
<tr>
<th>Example</th>
<th>Spur Source</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>A spectrum analyzer uses the ADC12D800RF interleaved and cannot tolerate a strong spur in the middle of the spectrum</td>
<td>• DCLK running in Demux SDR Mode causes a spur at Fs/4</td>
<td>• Choose instead the Non-Demux SDR DCLK, which moves the spur to Fs/2</td>
</tr>
<tr>
<td>A wideband communications application uses the ADC12D1800RF interleaved to achieve high sampling bandwidth</td>
<td>• DCLK produces spur at Fs/8 or Fs/4</td>
<td>• Adjust the sampling clock so that the fixed-frequency spurs land on channel boundaries</td>
</tr>
<tr>
<td>A long-range tactical radar with Fs = 750Msps cannot tolerate interleave images</td>
<td>• Most members of the GSPS ADC family have interleaved channels, which produce image spurs</td>
<td>• Use the ADC12D800RF, which has only 1 converter per channel</td>
</tr>
</tbody>
</table>
SUMMARY AND RECOMMENDATIONS
Summary and conclusions

- In order to achieve high-resolution, high-sampling rate ADCs, certain techniques were chosen which also generate spurious content.

- Spurs in the GSPS ADC family come from non-linearities, interleaving, and system clocks.

- Techniques to address these spurs include ADC features such as calibration, dithering, and frequency planning.

- Input signals that consist of multiple wideband signals or single tones act like dithering and reduce the impact of non-linearities.
## Solutions Recommendation

<table>
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<tr>
<th>Spur</th>
<th>Dominant Source</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower order harmonics</td>
<td>Non-linearity in track-and-hold</td>
<td>• Calibration</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Frequency planning</td>
</tr>
<tr>
<td>Higher order harmonics</td>
<td>Folding-interpolating architecture</td>
<td>• Calibration</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Dithering</td>
</tr>
<tr>
<td>IMD₃</td>
<td>Non-linearity in track-and-hold, folding-interpolating architecture</td>
<td></td>
</tr>
<tr>
<td>DC, Fs/4, Fs/2</td>
<td>Sub-converter offset mismatch in interleaving architecture</td>
<td>• ADC selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• ADC features</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Digital correction</td>
</tr>
<tr>
<td>Fs/2 – Fin, Fs/4 ± Fin</td>
<td>Sub-converter gain mismatch and timing skew in interleaving architecture</td>
<td></td>
</tr>
<tr>
<td>Fs/8, Fs/4, Fs/2</td>
<td>Coupling from DCLK</td>
<td>• DCLK selection</td>
</tr>
<tr>
<td>DC, Fs/2</td>
<td>Coupling from sub-converter clock</td>
<td>• ADC selection</td>
</tr>
</tbody>
</table>
Questions?

• Thank you for attending!
• Any questions?