## Introduction

The Kintex UltraScale FPGA KCU105 is a development board created by Xilinx. It is aimed to prototype mediumto-high volume applications. The KCU105 uses Ethernet and dual USB-to-UART capabilities to interface with a host computer and set up the FPGA. Texas instruments have created a platform where the KCU105 can interface with TI's latest and most popular high speed data converters Evaluation Modules (EVM) as if it were connected to a TI development board. The platform also allows users to operate the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) software to capture data from an Analog-to-Digital converter (ADC) as well as generate data for a Digital-to-Analog convert (DAC).

# Functionality

The KCU105 has a standard FMC connector that proves an interface between FMC-based development boards and all TI JESD204B ADC and DAC EVMs. To acquire data, receive data, and do register read and writes using a host PC, the FPGA transmits and receives data across three Serial Peripheral Interface (SPI) busses using dedicated pins on the FMC. For communicating, the KCU105 uses Ethernet for connecting to a host PC through a local network and dual USB-to UART bridge interface. The KCU105 also has an industry-standard JTAG connection for configuring the FPGA over USB.

### **Hardware Configuration**

Refer to Xilinx KCU105 for configuration. Refer to specific TI's ADC/DAC EVM for configuration.

### Software Start Up

- Instructions for HSDC Pro v4.42 or greater. (Same as TSW14J10EVM)

Download the latest version of HSDC Pro GUI to a local directory on a host PC. This can be found on the TI website by entering "HIGH SPEED DATA CONVERTER PRO GUI INSTALLER" in the search parameter window at <u>www.ti.com</u>......

- USB interface and Drivers

Connecting Ethernet, UART, and JTAG connector. Ensure Silicon Labs drivers are installed. Configuring a terminal applications (Tera Term, Hyperterm, Putty) to communicate with the COM port assigned to Silicon Labs interface.

- Download instructions for Xilinx Vivado design tool.

https://www.xilinx.com/products/design-tools/vivado.html

#### **Downloading Firmware example**

Instruction on downloading firmware to KCU105, give KCU105 GPIO LED status .....

The user GPIO LEDs on the evaluation boards are used to provide additional visual status indications. The LEDs are assigned as follows:

- 0 Rx SYNC, ON = SYNCB deasserted by Rx core
- 1 Tx SYNC, ON = SYNCB deasserted by Tx core
- 2 RX Reset done, ON = RX reset complete
- 3 DRP CLK, Flashing = CLK Active
- 4 DXI CLK, Flashing = CLK Active
- 5 TX/RX CORECLK, Flashing = CLK Active
- 6 GT REFCLK, Flashing = CLK Active
- 7 TX EMPTY, ON = There is no data available for the TX core from AXI DMA

## DAC and ADC GUI configuration File changes when using a Xilinx development platform

The configuration files that come with the TI ADC and DAC EVM GUIs are setup to operate with the Altera-based TI TSW14J56EVM. There are configuration files created for other Xilinx developments boards like the Virtex VC707 or Zync ZC706. With the latest firmware, some GUI can be configured as if it was connected to the TSW14J56EVM. Depending on the case, the ADC/DAC may be configured with the GUI, Xilinx configuration files, or a couple of changes to the settings of the LMK04828 registers. See example sections.

The firmware for the Xilinx Development Platforms use a separate clock input for REFCLK and Core clock to give maximum flexibility and support all line rates and subclasses with a single programmable design. The Xilinx IP used in the firmware can be driven by a single clock in many circumstances (see the clocking section of the Xilinx IP product guide for more details).

	MaxLr(Gbps)	1.2	1.6	1.9	2	2.4	3.2	3.9	4	4.9	6.5	7.9	8.1	8.2	9.8	12.5
	MinLr(Gbps)	1	1.201	1.601	1.901	2.001	2.401	3.201	3.901	4.001	4.901	6.501	7.901	8.101	8.201	9.801
xMult																
2		Υ	Υ													
10		Υ	Y	Y	Y	γ	Υ	Υ	Υ	Υ	Y	Y	Y	Υ		
20					Y	Y	Υ	γ	γ	γ	Y	γ	Y	γ	Υ	Y
40									Υ	Υ	Υ	Υ	Y	Υ	Y	γ

THE REFCLK and Core clk are determined by the following line rate conditions:

#### Figure 2 Valid xMult line rate ranges.

Line rate switching is supported across the entire speed range supported by transceivers. The ratio of REFCLK to line rate multipliers is also programmable. The line rate is determined by.... The multiplier is programmed in HSDC PRO by the ini files.

Note: REFCLK = line rate/ xMult

Example:

A line rate of 5.0G is in the range between 4.901Gbps and 6.5Gbps and is supported by the xMults values of 10,20, and 40. Therefore, the possible values for REFCLK are:

5.0G/10 = 500MHz, 5.0G/20 = 250MHz, 5.0G/40 = 125MHz

# ADS42JB69/49 EVM startup with Xilinx KCU105



- 1. Connect the ADC to FMC HPC connector J22 on the KCU105.
- 2. Connect the power cables to the KCU105.
- 3. Connect two USB micro B cables between the KCU105 and a host computer with Vivado loaded: one between the USB to JTAG interface J1, and the other between the dual USB-UART port J4.
- 4. Connect a micro USB cable between ADC and computer.
- 5. Open a serial port connection with any sort of serial terminal software, e.g. TeraTerm, Hercules, etc.
- 6. Initialize a serial port communication to Silicon Labs Dual CP210x USB to UART Bridge: **Enhanced** COM Port. Set the baud rate of this serial connection to **115200**, and leave all other defaults as set.
- Open another serial port connection and connect to Silicon Labs Dual CP210x USB to UART Bridge: Standard COM Port. Ensure the baud rate of this serial connection is 9600, leaving all other defaults as set.

(If you do not see these COM ports, open the Device Manager and install the proper drivers)

- 8. Connect an Ethernet cord from the KCU105 to a local network (same as the host computer)
- 9. Power up the KCU105 board. There should be information scrolling on the Enhanced COM port.

# Next:

- 1. Connect the power cable to the ADS42JB49 EVM and open the ADS42JBXX GUI. (This guide uses the updated GUI for the ADS42JBXX)
- 2. Go to the ADS42JBXX tab and click on "Device Reset" in the top left corner.
- 3. Go to the LMK0428 tab and click on "RESET" in the top left corner.
- Go to the "Low Level View" tab and click on "Load Config". Select the proper configuration file. In this case we are using an ADS42JB69 in a 421 mode at a sampling rate of 250MHz: ADS42JB69\_EVM\_LMF421\_250M.cfg

# Note: The configuration file can be used for both the ADS42JB69 and ADS42JB49

Block Diagram	ADS42JBxx	LMK04828	ow Level View	US	B Status 🔵	Reconnect FTD
Register Map				Milita Data	Tr	ansfer Read to Wri
Block / Register N	lame	🗛 🏘 Choose or En	nter Path of File			
LMK04828 x000		0 Save	in: 📜 New Config I	Files 🔹	G 👂 😕 🗔	•
x002		0	Name	*	Dat	te modified
x003		0	D 4D5421849	EVM LMF222 150M KC705.cfg	9/1	8/2015 8:33 AM
x004		0 Recent Places		EVM_EMF222_150M_RC705.ctg		5/2015 6:59 AM
x005		0	AD3423043	EVM_LMF421_250M_cfg		4/2014 2:00 PM
x006		9	AUS42JB09	_EVIVI_LIVIF421_250IVI.CIg	2/1	4/2014 2:00 PM
x00C		0 Desktop				
x00E x100						
x100 x101		0				
x103						
x103		0 Libraries				
x105		0				
x106		0				
×107		n Computer				
Register Descrip	tion					
		Network	•	Ш		
		Network	File name:	ADS42JB69_EVM_LMF421_250M.cfg	+	ОК
			Save as type:	Custom Pattern (*.cfg)	-	Cancel

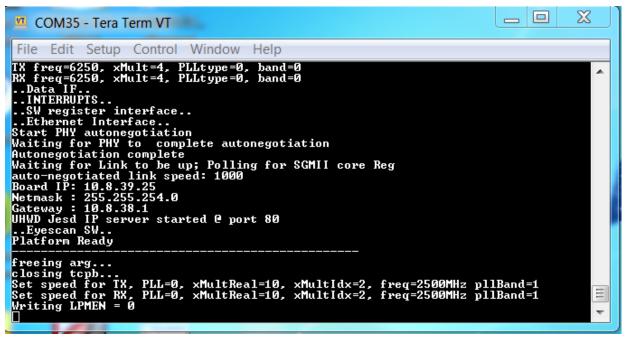
To program the FPGA, do the following steps:

- 1. Open Xilinx Vivado 2016.1 design tool
- 2. Double click on "Open Hardware Manager".
- 3. Click on "Open Target" (located on the green bar), and select "Open New Target" (You can also go to Tools -> Open New Target)
- 4. Click on "Next" twice. Select the Hardware Target, and click "Next" again.
- 5. Click on "Finish".
- 6. Click on "Program device" (located on the green bar). Select xcku040\_0. (You can also go to Tools -> Program device)
- 7. Select the proper bit stream file. In this case, the firmware for the KCU105 is: "KCU105\_TI\_DHCP.bit."
- 8. Click on "Program."
- 9. A new window will open showing the status of the programming. Once this reaches 100%, the FPGA is programmed.

# (Make sure the calibration passes and that there are no errors)

Vivado 2016.1		Contraction of the local division of the loc						
<u>File E</u> dit F <u>l</u> ow <u>T</u> ools <u>W</u> indow Lay	out <u>V</u> iew <u>H</u> elp						Q- Search	h commands
) 🕼 🖉 🗎 🐘 🗙 🐝 🎯 😑	efault Layout	👻 🎉 🔖 🎉 🖎 Dashboard 🕶 🗳						
Hardware Manager - localhost/xilinx_t	tcf/Digilent/21025:	1893722						
Hardware	_ 🗆 🖻 ×	S MIG - MIG_1 ×						00
२ 🔀 🖨 🛐 📭 🕨 🕨 🔳		Properties	* 🗆	Calibration/Margins				*
Name	Status	Name: MIG 1	A	Mode	Pattern		Clock Edge	
localhost (1)	Connected	MIG_1		Read	<ul> <li>Simpl</li> </ul>	٥	Rising	
xilinx_tcf/Digilent/2102518937		MicroBlaze status: PASS	=	Write	Comp		Falling	
xcku040_0 (3) SysMon (System Monitor)	Programmed	DQS gate status: RUNNING			Comp	lex	-aning	
- 3 hw axi 1 (AXI)		Message: No errors		Name	Left Margin (ps)	Center Point (ps)	Right Margin (p	s)
MIG_1 (MIG)	CAL PASS			Rank 0				
		Status	* 🗆	😝 🕀 Byte 0				
		Calibration Stage	Status	PS Nibble 0 Nibble 1		218 243	329 322	218 243
				Byte 1		243	322	243
		1 - DQS Gate	PASS A	Nibble 0		234	335	234
III	- F	2 - DQS Gate Sanity Check 3 - Write Leveling	PASS PASS	Nibble 1		228	305	232
		4 - Read Per-Bit Deskew	PASS	Byte 2		220	505	2.52
ardware Device Properties	? = 🗆 🖻 ×	4 - Kead Per-Bit Deskew 5 - Read Per-Bit DBI Deskew	SKIP	Nibble 0		213	270	218
		6 - Read DQS Centering (Simple)	PASS	Nibble 1		218	286	218
		7 - Read Sanity Check	PASS =	Byte 3				
xcku040_0			PASS	Nibble 0		234	286	239
		8 - Write DQS to DQ Deskew 9 - Write DQS to DM/DBI Deskew	PASS	Nibble 1		229	279	229
Name: xcku040_0		10 - Write DOS to DO (Simple)	PASS	Byte 4				
Part: xcku040		11 - Write DQS to DQ (Simple)	PASS	Nibble 0		218	288	223
ID code: 03822093	-	12 - Read DQS Centering DBI (Simple)	SKIP	Nibble 1		218	258	223
	=	13 - Write Latency Calibration	PASS	Byte 5				
IR length: 6		14 - Write Read Sanity Check 0	PASS	Nibble 0		229	264	234
Status: Programmed		15 - Read DQS Centering (Complex)	PASS	Nibble 1		229	259	229
		16 - Write Read Sanity Check 1	PASS	Byte 6				
Programming file: <a>ire/KCU105_TI_DH</a>	CP_Hugh_Aug	16 - Write Read Sanity Check 1 17 - Read VREF Training	SKIP	Nibble 0		218	283	218
	*	17 - Read VREF Fraining 18 - Write Read Sanity Check 2	SKIP	Mibble 1		219	291	210
III.	•		PASS	Table Chart (Rank 0) - Lef	t Aligned Chart (Rank 0) - Cente	r Aligned		
eneral Properties		19 - Write DOS to DO (Complex)	PASS					
Console		U.						2 - 0 6
program_hw_devices [linder	I det hu dettio	eel 01						
		0:10 ; elapsed = 00:00:10 . Memory (MB):	peak = 854.465 ; gain	= 0.000				
WARNING: [Labtools 27-3089								
		(JTAG device index = 0) is programmed wit						
INFO: [Labtools 27-2302] I	Device xcku040	(JTAG device index = 0) is programmed wit	h a design that has 1	MIG core(s).				
•			111					)
Type a Tcl command here								
🗏 Tcl Console 🔎 Messages 🛭 🗞	Serial I/O Links	Serial I/O Scans						
le								

The board IP address will be available on the Standard COM port.



#### Next, the VADJ8 voltage must be set to 1.8V. This is set in the Enhanced COM port terminal.

- 1. Navigate to the Enhanced COM port window. Return to the main menu by entering "0" in the terminal.
- 2. Select "Adjust FPGA Mezzanine Card (FMC) settings" by entering "4"
- 3. "Set FMC VADJ to 1.8V" by entering "4"
- 4. Return to the main menu by entering "0"
- 5. To check this voltage, select "Get the Power Systems Voltages" by entering "2"
- 6. Enter "7" to "Get VADJ1D8 voltage." The voltage should appear above the menu.
- 7. Return to main menu by entering "0"

# It is recommended that the FPGA is reprogrammed and the VADJ1D8 voltage reset every time after programming the ADC.

Open the latest version of HSDC Pro GUI v4.201 (under Texas Instruments, High Speed Data Converter Pro\_KC105) by right clicking on the icon and **running as administrator**.

In the Select Board popup, check "Connect to KCU105." The IP address: Port can either be selected from the drop down menu or entered manually separated by a colon, i.e. IP Address: Port. Both the IP Address and Port number can be found in the Standard COM port terminal.

🚺 High	n Speed	Data Con	verter Pro	v4.201	100				
File I	ínstrum	ent Optio	ns Data	Capture Options T	est Options Device GUI	Options <b>Help</b>			
₩Ţ	ÈXAS NSTRU	MENTS		<b>.</b>	ADC		₽ <b>₽</b> 	DAC	
Test S	elect AD Capture election		0 16383		00 10000 12500 15000 17	00 20000 22500 250	00 27500 30000 32500 35000	) 37500 40000 42500 4500	2 + 2 + 2 + 2 + 2 + 2 + 2 + 2 +
Sin	igle Tor			Real FFT 💌	Select Board	Transmitt B	<i>ب</i> ر کړ	l Averages I	RBW 7629.39 Hz
SNR	Value 67.36	Unit ү 🔺 dBFs	10.0-						,⊉ +
SFDR THD	48.27 46.67	dBFs dBFs	0.0-	Spur	Select The Serial numb	er of the Device	-		٩
SINAD	46.61	dBFs	-10.0-			Serial Numbers			Q
ENOB Fund.	7.45	Bits dBFs	-20.0-			Sertal Numbers			
Next Spur	-73.79	dBFs =							
HD2 HD3	-48.27 -53.77	dBFs dBFs	-30.0-	12					
HD4	-57.17	dBFs	-40.0-	-					
HD5 NSD/Hz	-62.74 -148.32	dBFs dBFs/H:	-50.0-						
M1	dBFs -109.50	Hz 0.00E+(	요 -60.0-				•		
M2	-117.24	1.00E+€	-				Address - Port Number		
Delta Test Pa	7.74 rameter	1.00E+( *	-70.0-		Connect to KC	U10 10.8.39.25:80	•		
Auto C	Calculation	n of	-80.0-						
	ent Freque Window (		-90.0-	-	— ок		Cancel –		
	2768	•	-100.0-	-					
	tput Data 250M	Rate	-110.0-						
		Frequency							
39.95	5513916	ОМ	-120.0-						
			-130.0-	-	25M	50M	75M	100M	125M
				-		Frequen			.2011
			•						×
		Firmy	vare Ver=		TSW1400 E	oard = " "		Interface Type = " "	
Device i	info detai	ls			11/3/2016 10:44:53 AM	Build - 06/21/2016	NOT CONNECTED		exas Instruments

Select the ADC tab, and then select "ADS42JB69\_LMF\_421" using the device drop-down arrow. Make sure the Analysis Window (samples) is no greater than 32,768 (due to the limit of the internal FPGA memory used for this capture). Next enter **250M** in the ADC Output Data Rate window.

The GUI will display the new lane rate (2.5G) and JESD reference clock required by the capture platform FPGA (250M). Click on "OK".

Connect an analog input signal to the SMA connect (J1)

Click on "Capture"

# Capture of HSDC Pro using a bandpass filter and a tone of 170MHz @+15.5 dB

🚺 High Speed Data Cor	verter Pro v4.201			
File Instrument Optio	ns Data Capture Options T	Test Options Device GUI Options Help		
TEXAS INSTRUMENTS	100 × 100 ×	ADC	DAC	
ADS42JB49_LMF_421	8 8 0 − 0 2500 5000 75 Real FFT ▼		0 27500 30000 32500 35000 37500 40000 hannel1) 1/1 Averages	42500 45000 47500 50000 RBW 7629.39 Hz
SNR         71.71         dBFs           SFDR         85.91         dBFs           THD         84.65         dBFs           SINAD         71.50         dBFs	10.0 -		+(79.994M)	2 + (1) (2)
ENOB 11.59 Bits Fund. 1.07 dBFs Next Spur -94.26 dBFs HD2 -85.91 dBFs HD3 -91.16 dBFs	-20.0 - -30.0 -			
HD4 -104.37 dBFs HD5 -102.42 dBFs NSD/Hz -152.67 dBFs/H: dBFs Hz M1 -113.85 0.00E+t	-40.0 - -50.0 - - - - - - - - - - - - - - - - - - -			
M2         -111.77         1.00E+€           Delta         2.08         1.00E+€         ▼           Test Parameters         ✓         Auto Calculation of	-70.0		2	
Coherent Frequencies Analysis Window (samples) 32768 ADC Output Data Rate	-90.0 -		4	a saa dada a sababa
250M ADC Input Target Frequency 39.955139160M	-110.0 - 74 h h y 1 2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	normalization of the second	n adala da <mark>banan kalan kanan kan</mark>	A Mahala Laatabata
	•	25M 50M Frequency	75M 100N (Hz)	I 125M ▶
	e Version = "0.6"	KCU105 Board = 1020088	Interface Type = KCU	
Waiting for user input		11/3/2016 12:47:27 PM Build - 06/21/2016	CONNECTED Idle	🐺 Texas Instruments

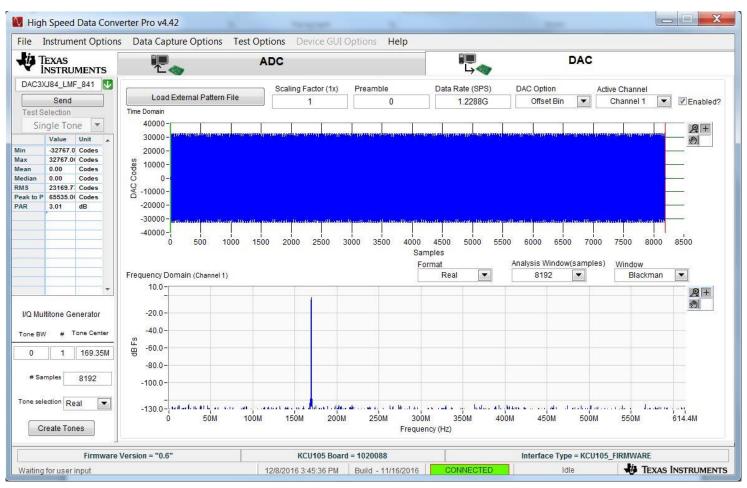
# DAC38J84 EVM with Xilinx KCU105 Development Board Set up Example

This section provides an example of using a DAC38J84 using a KCU105. The KCU105 Configuration will be the same as the ADS42J69 for the DAC38J84. With the updated firmware, users can use the DAC38J84 GUI as if it was connected to a TI's TSW14J56. This example will a mode of the DAC38J84 and what needs to be modified.

The setup will be a 841 mode configured as shown:

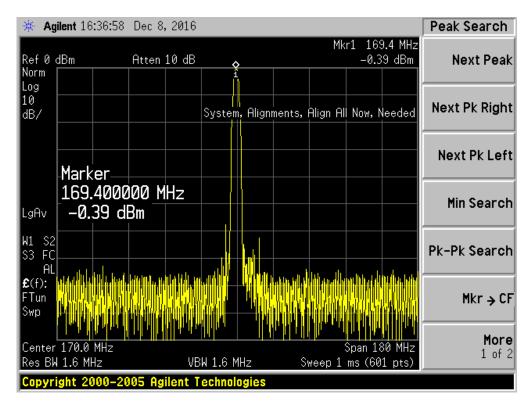
e Debug	Settings Help						
		DA	C3XJ8X GUI	/1.1			
uick Start	DAC3XJ8X Controls	LMK04828 Controls	Low Level View	Che	CK ALARMS	USB Status 🌔	Reconnect USB ?
St	tep 1 - Choose Clock Mode St	ep 2 - Choose DAC Configura	tion	Step 3 - Stats!			
		Device	Number of SerDes Lanes	DAC Output Rate		JESD204B Mode (L	.MFS)
	EVM Clocking Mode	DAC38J84 💌	8	2457.6	MSPS	8411	
		The second se	nterpolation	FPGA Clock 307.2	MHz	SerDes Linerate	
		1220.0 <b>•</b> MSPS	2	507.2	WITZ	12200	Mbps
	Step 4 - Program E Programming Of 1. Program LMK0 toggle DAC RE program DAC3 2. Reset DAC JES 3. Trigger SYSRE	der: 14828, SETB Pin, XJ8X D Core DAC RESE	XJ8X JESD (		Trigger LMK04 SYSREF	828	
	Quick Start Message						

- 1. Press button 1. Program LMK04828 and DAC3XJ8X
- 2. After completion, open HSDC Pro and connect as in the previous example
- 3. Press on the DAC tab, and select from the dropdown DAX3XJ84\_LMF\_841
- 4. Add the Data Rate and change the DAC option to 2's Complement.
- 5. Set the number of samples to at least **8192**
- 6. Create a tone. The GUI should be configured as followed:



HSDC Pro GUI with Single tone of 169.35MHz

- 7. Press Send and the current lane rate (12.288GHz) and FPGA Clock (307.2MHz) should match the numbers on the DAC38J84 GUI
- 8. Go back to the DAC38J84 GUI and press 2. Reset DAC JESD Core and 3. Trigger Button.
- 9. Connect an SMA cable to a Spectrum Analyzer and verify the DAC output



In this example, we will use the same mode, but a different configuration that shows the limitation of the KCU105 1. Configure the DAC as shown:

le Debug	Settings Help						
		DAC	C3XJ8X GUI	v1.1			
Quick Start	DAC3XJ8X Control	Is LMK04828 Controls	Low Level View	Che	K ALARMS	USB Status	Reconnect USB
Ste	ep 1 - Choose Clock Mode EVIM Clocking Mode Onboard	DAC38J84  DAC Data Input Rate	lumber of SerDes Lanes	Step 3 - Stats! DAC Output Rate 1474.56 FPGA Clock 92.16	MSPS	JESD204B Mode (L 8411 SerDes Linerate 3686.4	MFS)
	Step 4 - Program	Order: 1 Program   N	1K04828 2. Rese	tDAC 3	Trigger LMK04	1828	
	1. Program LN toggle DAC program DA 2. Reset DAC 3. Trigger SYS	RESETB Pin, and DAC3: AC3XJ8X JESD Core DAC RESET	XJ8X JESD		SYSREF		
	Quick Start Messag	e					
	Quick Start Messag	e					

- 2. The DAC GUI by default will be configured to generate a FPGA reference clock as line rate/40. Since the linerate is shown to be 3.6G the valid xMult line rate is only supported by x10 and x20 (refer to Figure 1).
- 3. In order to support this mode, the settings of the LMK04828 registers needs to be changed. Update the DCLK Divider to 16 in the DAC GUI as shown:

		DAC	3XJ8X GUI	v1.1		
uick Start DAC3	XJ8X Controls	MK04828 Controls	Low Level View	Check AL	ARMS USB Status	Reconnect USB ?
PLL1 Configuration	PLL2 Configura	ation SYSREF ar	d SYNC Clock (	Dutputs		
CLKout 0 and 1 FPGA Clock & SYSREF	CLKout 2 and 3 DAC Clock & SYSREF	CLKout 4 and 5 Not Used	CLKout 6 and 7 SMP Clock Outputs	CLKout 8 and 9 Extra FMC Clocks	CLKout 10 and 11 Not Used	CLKout 12 and 13 Extra FMC Clocks
Group Powerdown 💌 Output Drive Level 💌 Input Drive Level 💌	Group Powerdown 🕅 Output Drive Level 👽 Input Drive Level 👽	Group Powerdown 🕼 Output Drive Level 📄 Input Drive Level 📄	Group Powerdown 🗹 Output Drive Level 🗖 Input Drive Level 🗖	Group Powerdown 📝 Output Drive Level 🕅 Input Drive Level 🕅	Group Powerdown V Output Drive Level Input Drive Level	Group Powerdown 📝 Output Drive Level 🕅 Input Drive Level 🕅
DCLK Divider	DCLK Divider	DCLK Divider				
16 💌	2 💌	8	24	16 💌	8	8
DCLK Source	DCLK Source	DCLK Source				
Divider + DCC + HS	Divider + DCC + HS 💌	Divider 💌	Divider 💌	Divider 💌	Divider 💌	Divider 💌
DCLK Type Invert 📃	DCLK Type Invert	DCLK Type Invert 🕅	DCLK Type Invert 🕅	DCLK Type Invert 📃	DCLK Type Invert 💌	DCLK Type Invert 🔄
LVDS 💌	LVPECL 2000 mV	Powerdown 💌	Powerdown 💌	LVDS 💌	Powerdown 💌	LVDS
SDCLK Source	SDCLK Source	SDCLK Source				
SYSREF -	SYSREF -	Device Clock 💌	SYSREF -	Device Clock	Device Clock	SYSREF -
SDCLK Type Invert	SDCLK Type Invert	SDCLK Type Invert				
LVDS	LCPECL	Powerdown	Powerdown 💌	LVDS	Powerdown	Powerdown
SDCLK EN/DIS State	SDCLK EN/DIS State	SDCLK EN/DIS State				
Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	Active/Active
SDCLKout PD	SDCLKout PD	SDCLKout PD				
DCLKout_DDLY_PD	DCLKout_DDLY_PD	DCLKout_DDLY_PD	DCLKout_DDLY_PD	DCLKout_DDLY_PD	DCLKout_DDLY_PD	DCLKout_DDLY_PD
DCLKout_HSg_PD	DCLKout_HSg_PD	DCLKout_HSg_PD	DCLKout_HSg_PD	DCLKout_HSg_PD	DCLKout_HSg_PD	DCLKout_HSg_PD
DCLKout_ADLYg_PD	DCLKout_ADLYg_PD 🗸	DCLKout_ADLYg_PD 🗸	DCLKout_ADLYg_PD	DCLKout_ADLYg_PD	DCLKout_ADLYg_PD 📝	DCLKout_ADLYg_PD
DCLKout_ADLY_PD 📝	DCLKout_ADLY_PD	DCLKout_ADLY_PD	DCLKout_ADLY_PD	DCLKout_ADLY_PD	DCLKout_ADLY_PD	DCLKout_ADLY_PD

4. Follow the previous procedure to configure HSDC Pro and produce a tone. NOTE: The FPGA clock will not match on the HSDC PRO GUI and the DAC38J84 GUI.

# ADC12J4000EVM with Xilinx KCU105 Development Board Set up Example

The following is an example of using the Xilinx Ultrascale KCU105 development platform to collect data from an ADC12J400 in bypass mode, as shown in Figure 1 below.



- 1. Follow the procedure for connecting and establishing communication the KCU105.
- 2. Connect the ADC12J400 to the FMC HPC connector to J22 on the KCU105.
- 3. Power up the ADC12J400 and open the ADC12J4000 GUI. Choose On-board as clock, set Fs = 4000MSPS, and set decimation and serial data mode to bypass mode; DDR. Then click Program Clocks and ADC as shown:

49 ADC12J4000EVM GUI A										
File Debug	File Debug Settings Help									
	ADC12J4000EVM GUI A									
EVM Contr	JESD204B	DDC	NCO Configuration	Low Level View	5	USB State	us 🥥 Reconnect FTDI ?			
On- #2a. On-board Fs = 40 #2b. External F: 1000 #3. Decimation Bypass Program	#1. Clock Source       #1. Clock Source         On-board       ▼         #2a. On-board FS Selection       This tab is used to control the EVM to program the clocks, basic mode of the ADC, and read the temperature. Once the EVM is programmed, the other tabs allow the user to configure the ADC.         #2a. On-board FS Selection       1. User Inputs - How to program the EVM clocks and ADC:         #2b. External FS Selection       #1. Clock Source - the DEVCLK to the ADC may be supplied by the on-board PLL/VCO or externally by the user. If the on-board clock is selected, chose the FS at #2a. If the external clock is selected, enter the Fs at #2b.         #2b. External FS Selection       #2a. On-board FS Selection - The PLL/VCO will be programmed to provide any of the available sampling clock frequencies to the									
ADC Temp 0 deg LM95233 Lo 0 deg	rees C cal Temp rees C emperatures									
Operation Succes	sful.	1/12/201	1 11:44:30 AM B	uild: CON	NECTED	Idle	🔅 Texas Instruments			

- 4. Continue follow the steps for loading firmware in the Vivado design tool and open HSDC Pro
- 5. Select "ADC12J4000\_BYPASS" using the device drop down arrow. Make sure the Analysis Window is no greater than 32,768.
- 6. Enter 4G in the ADC Output Data Rate window. Click on "Capture" and the new line rate (8G) and JESD reference clock (200M) should show.
- 7. The captured result as shown:

