

Single Event Effects Characterization of Texas Instruments ADC12D1600CCMLS, 12 bit, 3.2 GSPS Analog-to-Digital Converter with Static and Dynamic Inputs

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Abstract—Texas Instruments’ ADC12D1600CCMLS is a dual channel, 12b Analog-to-Digital Converter that can support conversion rates up to 1.6 gigasamples per second (GSPS). The two channels can be seamlessly interleaved for conversion rates up to 3.2 GSPS. The device was put through heavy ion testing and was monitored for Single Event Latch-up, Single Event Functional Interrupt and Single Event Upset (SEU). Testing was done at two different ion energies and the impact of ion energy on SEU response is evaluated. SEU testing was performed with both static and dynamic inputs and the SEU signatures of each are compared.

Index Terms—analog-to-digital converter, heavy ion testing, single event effects,

I. INTRODUCTION

HIGH speed Analog-to-Digital Converters (ADC) are typically run with high input frequencies that can be in the second or third Nyquist zones. Test methods have been demonstrated for performing Single Event Upset (SEU) analysis on ADCs using dynamic inputs [1][2] with high input frequencies up through the second Nyquist zone. The test method described in [1] was modified and used to characterize Texas Instruments ADC12D1600CCMLS, 12b, dual channel 1.6 gigasample per second (GSPS) ADC, which also can operate as a single channel 3.2 GSPS ADC [3]. An improved method of capturing the data was employed so that code error signatures could be better analyzed. SEU testing was also performed with static inputs and the differences in the response between dynamic and static inputs are compared.

In addition to SEU testing of the digital output, SEU testing of the ADC output clock, Single Event Latch-up (SEL) and Single Event Latch-up testing were performed and the results are presented here. The testing was performed at two different ion energies (4.5 and 10 MeV/nuc.) to determine if the ion energy and range penetration into the silicon would have any impact on any of the Single Event Effects (SEE).

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II. PRODUCT TESTED

Texas Instruments’ ADC12D1600CCMLS is a dual channel 12 bit ADC that can support data conversion rates of 1.6 GSPS and input bandwidths to 4 GHz (Fig. 1) [3]. The two channels can be interleaved resulting in a single channel 3.2 GSPS ADC. It is built on a folding architecture for low power consumption (1.9 W per channel), high data conversion rates and high input bandwidth [4].

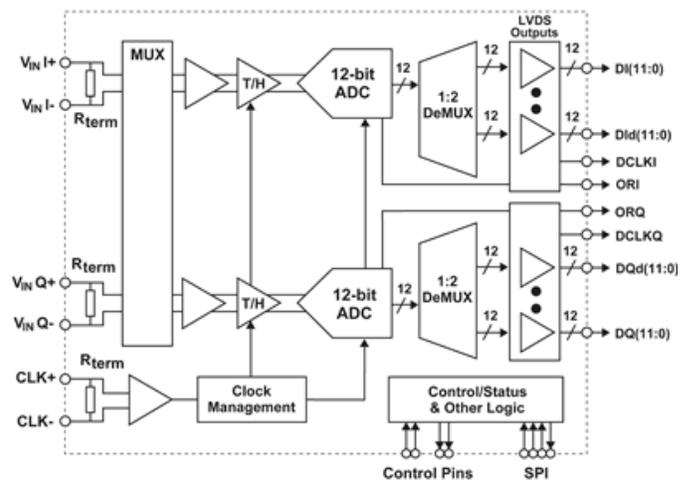


Fig. 1 Block diagram of the ADC12D1600

It employs four 1.9V dc power supplies (1.8V to 2.0V normal operating supply voltage range). In a typical application, these 4 power supplies would be powered from a single regulator on the same supply bus.

The ADC12D1600CCMLS has two control mode options, to set up the various configurations of the part, such as input edge sampling mode, full scale range, offset, gain, output clock settings and demuxing options. In “non-extended control mode” (non-ECM), the set up configuration is done through the control pins and the serial interface is disabled. If the part is powered up in non-ECM, it will come up in a known state based on the control pin settings. In “extended control mode” (ECM) most control pins are disabled and the part is configured through a serial interface (SPI). If the part

is powered up in ECM mode, it will come up in a random unknown state and it is necessary to write to all the registers to put the part in a known, stable state. As an alternative, the part can be started up in non-ECM to a known, default state and then switched over to ECM where adjustments in the part configuration can be made through the SPI. The contents of the control registers may be written out to verify they are correct.

As shown in Fig. 1, the two independently operating 12 bit ADC's, called I and Q, convert the input synchronously using a single input clock. Each of these converters has a 1:2 demultiplexer that feeds two LVDS output buses, called DI and DI_d and DQ and DQ_d for I and Q channel respectively. The DI_d and DQ_d outputs are delayed by one clock cycle with respect to the DI and DQ outputs. Thus the digital outputs from the two ADCs are available on 4 separate Low Voltage Differential Signal (LVDS) 12-bit buses (current and previous sample for each channel clocked out at ½ the sampling rate). Each channel has an output clock (DCLKI and DCLKQ in Fig.1) that runs at ¼ the input clock frequency, so that the output is in double data rate (DDR) format, with data presented on both the rising and falling edges of the DCLK outputs. The 1:2 demux option is switchable and may be turned off, in which case the output will be 1:1 on a single LVDS bus per channel, in which case, the output clock will be ½ the input clock.

Each channel (I and Q) has a differential input that supports frequencies up to 4 GHz, with a 3 dB insertion loss (full power input bandwidth) in the range of 2.4 to 2.7 GHz. The full scale range of the inputs is selectable from 600 to 1000 mV in 32767 steps.

The ADC12D1600CCMLS has an on chip temperature diode for monitoring the junction temperature of the part.

The ADC12D1600CCMLS is the latest part in the evolution of the ultrahigh speed ADC product family, which started with the ADC08D1000WGFQMLV (5962F0520601VZC) from National Semiconductor and continued under Texas Instruments after its acquisition of National in 2011. This family of ADCs uses the same basic folding architecture with calibration and is on the Texas Instrument's CMOS9X 180 nm CMOS process. All earlier versions of this space product family are SEFI immune and the ADC08D1520WGFQMLV (5962F0721401VZC) and ADC10D1000CCMLS are SEFI immune [5]. The process uses an epi layer on a low resistivity, highly doped substrate and has a 6 layer metal stack. From the top surface of the die, through the metal stack and active area of the silicon is less than 15 μm.

The earlier 10 bit ADC10D1000CCMLS was designed with intent of evolving into a 12 bit part while still using much of the 10 bit infrastructure. The 12 bit part uses the same basic layout and die size as the 10 bit part. They both use the same package, with the same footprint and number of columns. They have the same pinout except for the functions of a few control pins, and that for the 10 bit part the two lowest LSB output pins are inactive. It is possible to swap out the 10 and 12 bit parts on a board.

The ADC12D1600CCMLS comes in a 376 column grid

array ceramic package and is manufactured per the Class V flow of MIL-PRF-38535 [6].

III. TEST METHOD

Heavy ion testing was performed per JESD57 [7] with ASTM 1192 [8] and ESA/SCC 21500 [9] used as references. The test techniques, systems and software previously used for testing the 10b ADC10D1000CCMLS [6] were reused for testing the ADC12D1600QML-SP.

A. Test Board and Set Up

The device under test (DUT) was soldered to Texas Instruments ADC1xD1xxxRB Gigasample Reference Board (Fig. 2) [10]. This is a universal board for testing the 10b and 12b versions of the ADC1xD1xxx family of ADCs. The board contains an FPGA for interfacing with the DUT and data capture. The clock for the FPGA is driven by the DLCKI output clock from the ADC. The board also has on board power supplies and oscillator and PLL for powering and driving the DUT, but with a switchable option for an external power supply and clock. The onboard clock is 1.5 GHz. The board can communicate with a computer through a USB port. Texas Instrument's WaveVision5 software is used to drive the board, program the DUT and capture and analyze the output data [11]. The board is powered with a 7.5 V supply.

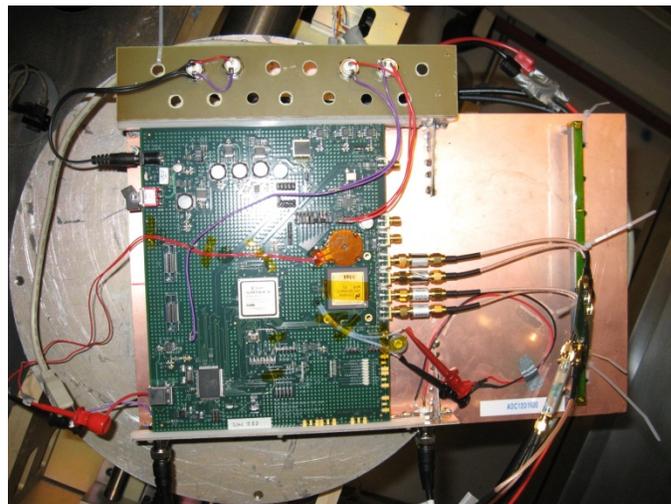


Fig. 2 DUT connected to ADC1xD1xxxRB Gigasample Reference Board inside the vacuum chamber.

The DUT was powered by a remote power supply in the control room of the test facility. Due to the long power cables and high current draw of the DUT, there was a significant voltage drop through the cabling. The supply voltage to the DUT was monitored at the board level. The supply current to the DUT was constantly monitored in the control room, using an HP 3468A multimeter.

A Rhode & Schwarz SMA 100 A signal generator was used to provide the analog signal to the DUT. The signal was passed through a 5% band pass filter and then split for each channel. For each channel, a Texas Instruments SC01806-09 balun board was used to provide a differential signal to the

ADC1xD1xxRB board and the analog inputs of the DUT.

To heat the DUT, a resistive spiral heater was glued to the test board. A thermistor was epoxied to the board to monitor the board temperature. The heater and thermistor were controlled by a LakeShore 332 temperature controller.

B. FPGA Image

For all heavy ion testing, all 12 bits of the ADC12D1600 were active and connected to the FPGA. However, the FPGA had an image for a 10b part and ignored the two least significant bits (LSB) when doing a data capture. This allowed for reuse of the code error software from the testing of the ADC10D1000CCMLS for Single Event Upset (SEU) testing. Because background the noise at the cyclotron test facilities is so high and board connections are less than ideal, it is not possible to resolve the two least significant bits while doing heavy ion testing. The 2 LSBs represent less than 1 mV of change in the input voltage, which is lost in the noise of the environment. In this paper, the code error data will be presented as for a 10b output with an output range of 0 to 1023 and an LSB will be that of a 10b output.

C. SEL Test Set Up

The supply current to the DUT was constantly monitored through the testing with the HP 3468A multimeter which has a resolution of 10 μ A. The current draw by the DUT was between 1.79 and 2.15 A, depending upon the operating conditions of the part. Even in a steady state operating condition, the supply current could vary several 100 mV over a few minute time span. A sudden change in the supply current of more than 2% would be considered an SEL.

Specific, worst case testing was performed with the supply voltage at maximum voltage (2 V) and junction temperature of 125°C at the highest Linear Energy Transfer (LET) tested. The fluence for each ion run was 1×10^7 ions/cm². The board and DUT were heated using the resistive heater glued to the test board. The junction temperature of the DUT was monitored using the on chip temperature diode and the WaveVision5 software. The clock was supplied by the internal supply on the DUT board and was 1.5 GHz.

D. SEFI Test Set Up

All testing was performed with the DUT in “Extended Control Mode”. The configuration of the DUT is programmed through the serial interface and the settings are held in registers. The operation of the DUT was continuously monitored during the testing. Any change in the operation of the part, calibration or input range would be considered a SEFI.

Except for the SEL specific tests, all testing was performed the minimum operating supply voltage (1.8 V), which is worst case for SEFI.

At the highest LET tested, specific SEFI checks were run. The contents of the configuration registers were read before and after an ion run and compared. Also, a Fast Furrier Transform (FFT) was run and the product performance parameters, such as SNR and ENOB, were calculated before and after an ion run and compared. The DUT would be considered to have a SEFI if any of the registers changed or

the ENOB changed by more than 0.2 bit, which is within the repeatability of the test. The fluence for each ion run was 1×10^7 ions/cm². The clock was supplied by the internal supply on the DUT board and was 1.5 GHz. The inputs were either 1.034896 or 999.986 MHz.

E. Output Clock SEU Test Set Up

The DCLKI output was monitored with a differential probe connected to a Tektronix DPO7354 Digital Phospor Oscilloscope. The scope trigger was set on “width” mode so that if the falling edge of the clock was outside the expected time window, an error would be counted and the clock output would be captured (Fig. 3). Testing was performed with the 10 MeV/nuc. beam with the input clock at 1 GHz and the output clocks at 250 MHz. The trigger window limits were set at 1.9 and 2.5 ns.

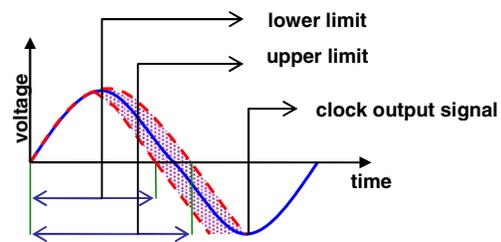


Fig. 3 Scope trigger setting for monitoring the DCLKI clock output. If the falling edge of the clock is not within the limits, an error is recorded and the output clock waveform is captured.

F. Output Code SEU Test Set Up

The beat frequency and code error test method described in [1] was used for this testing with a modification on how the data was captured. As in [1], the FPGA on the DUT board was programmed with code error detection software. For each channel (I or Q), the output was compared to the previous output. For instance, on the I channel, the DI output was compared to the previous DI_d output. If the output codes differed by more than a preset LSB value, an error would be registered (Fig. 4). The modification to [1] is that whenever an error was detected, 8 other codes around that error would be recorded. This allows detection of a case where the code is stuck at one value or hits the rails for more than one clock cycle.

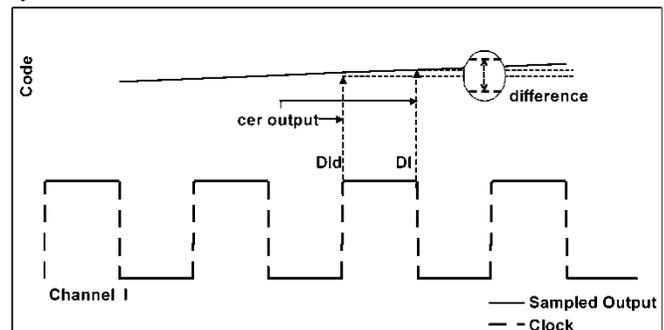


Fig. 4 The CER detection software programmed into the FPGA compares the current output code to the previous output code and registers an event if that difference is greater than a programmable limit. A timestamp plus 9 output codes around the error are recorded.

In order to detect small errors in the output code, a proper beat frequency must be chosen. The beat frequency (and resultant output of the ADC) is the difference between the clock and input frequencies (Fig. 5). This allows the input of the ADC to be run at high frequencies, while the outputs are at a much lower frequency for monitoring and capturing output code errors.

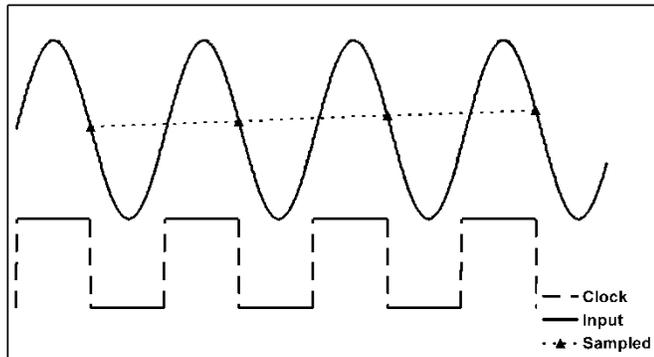


Fig. 5 Beat frequency. With the clock frequency set at 1 GHz, and the input frequency slightly lower at 999.896 MHz, the sampled points on the input curve will result in an output of 104 kHz.

The input clock frequency was 1035 MHz for testing with the 4.5 MeV/nuc. beam and 1000 MHz for testing with the 10 MeV/nuc. beam. Testing was done with both dynamic inputs and static inputs. For the dynamic testing, the input frequency was set so that the output beat frequency was 104 kHz. The error limits were set at ± 23 LSB. For testing with static inputs, the output of the frequency generator was turned off. The common mode circuitry of the ADC12D1600 pulled the inputs up to midrange, so the expected output code was midrange (511 LSB). With static inputs, the noise of the system was less, allowing for tighter limits to be set for the output code errors (± 5 LSB) and the detection of smaller errors.

G. Test Facility, Dates and Sample Size

Testing was performed at the BASE Facility 88-inch cyclotron at Lawrence Berkeley National Laboratory [12], using the 4.5 MeV/nuc. beam on August 10, 2012 and the 10 MeV/nuc. beam on September 11, 2012.

Two DUTs were tested at each LET. SEU cross section data presented is per channel, averaging the data from the two channels and the two DUTs.

IV. RESULTS

During “room” temperature testing the DUT junction temperature ranged from 78°C to 87°C, as measured by the on chip temperature diode. The DUT consumes 4 W of power. Since testing was done in a vacuum and the board was isolated with little heat sinking, the thermal dissipation of the test system was poor, resulting in the high junction temperature.

A. SEL and SEFI Test Results

No incidences of SEL or SEFI were detected to the highest LET tested: 120 MeV-cm²/mg. The DUT would continue to

operate as programmed until the configuration was manually changed. On the SEFI specific tests, no changes were seen in the performance of the DUT as measured by ENOB (Table I) and the control register readout was the same before and after each ion run.

TABLE I
SEL AND SEFI TEST RESULTS

Date	DUT	Run	LETeff (MeV-cm ² /mg)	Junction Temp (°C)	Supply Current			ENOB		Pass/Fail	
					Pre	Post	Delta	Pre	Post		
Aug 10	261	1	99.7	82	1.97479	1.97525	0.00046	8.6	8.6		
		2	121.76	82	1.97525	1.97586	0.00061				
		3	121.76	126	2.14299	2.14373	0.00074			Pass	
		4	99.7	126	2.14506	2.14455	-0.00051			Pass	
	251	13	99.7	85	2.01882	2.02193	0.00311	8.3	8.3	Pass	
		14	121.76	85	2.02228	2.02350	0.00122	8.3	8.2	Pass	
		15	121.76	125	2.19689	2.19776	0.00087			Pass	
		16	99.7	125	2.19810	2.19821	0.00011				
	Sep 11	251	16	58.8	89				8.4	8.4	Pass
			17	117.6	89	1.803	1.804	0.001	8.4	8.4	Pass
		263	18	100	125	1.95551	1.98880	0.03329	8.4	8.3	Pass
			39	58.8	89				8.6	8.6	
		40	40	58.8	127	2.15290	2.15923	0.00633	8.6	8.6	Pass
			41	117.6	127	2.15200	2.15180	-0.00020	8.6	8.6	

B. Output Code Upset Event Length

The code error software recorded an error whenever one reading was different than the previous reading by more than the set limit. For an SEU event, there would be at least two errors recorded, one for when the output code was out of the expected value and one for when the output code returned to the correct reading. For some events, multiple errors could be recorded if the output oscillated. The test data were analyzed so that the number of events and lengths of events were determined.

Most events lasted for only one clock cycle (1 ns with a 1 GHz input clock) but there were a few events lasted as long as 48 clock cycles (Fig. 6). There was a dependence upon LET and the number of events that were longer than one clock cycle (Fig. 7). At the highest LET tested (117.56 MeV-cm²/mg) 22% of the events were longer than one clock cycle, while it was only 7% for the lowest LET tested (1.65 MeV-cm²/mg). Less than 1% of the events were greater than 6 clock cycles.

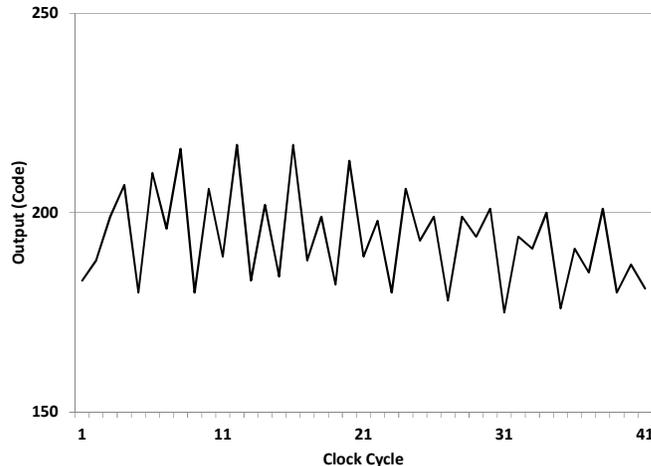


Fig. 6 Example of an event lasting more than one clock cycle from a Bismuth ion run with the 4.5 MeV/nuc. beam for an LET of 99.7 MeV-cm²/mg. Less than 1% of the all events were greater than 6 clock cycles.

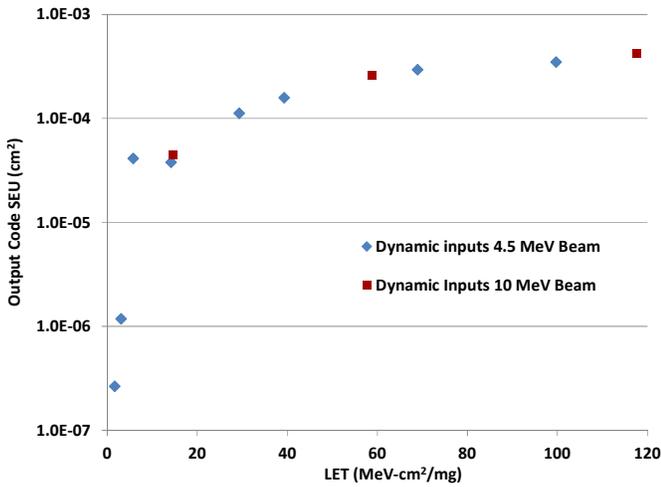


Fig. 7 Percentage of events lasting just one clock cycle. Less than 1% of the events lasted more than 6 clock cycles.

C. Output Code Error Magnitude

An output code error could be either positive or negative. The magnitude of the error ranged from the error limit (23 LSB when testing with dynamic inputs) to a full scale swing (Fig. 8). Less than half of the errors were greater than 100 LSB and the population of the larger magnitude errors was dependent upon the LET of the ion.

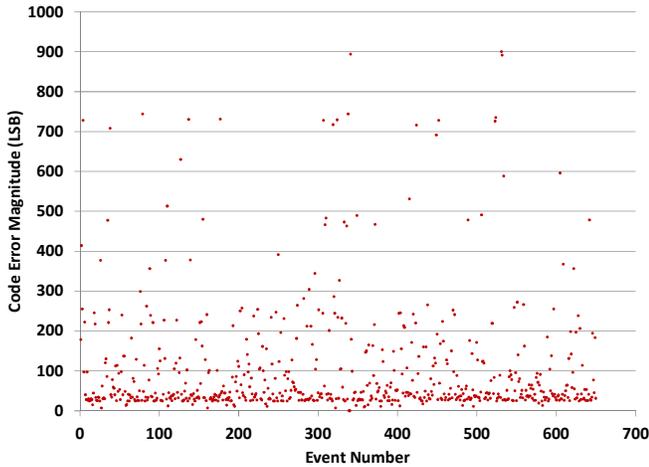


Fig. 8 Magnitude of the output code error for each event for a Xenon ion run with the 10 MeV/nuc. beam for an LET of 58.8 MeV-cm²/mg. Data are for both the I and Q channels.

D. Test results of 4.5 vs. 10 MeV/nuc Beam Energies

No differences were seen in SEU durations (Fig. 7), code error magnitudes or SEU cross sections (Fig. 9) between the testing with the 4.5 MeV/nuc. and 10 MeV/nuc. beam energies.

E. Dynamic vs. Static Inputs

With static inputs, the inputs were pulled up to midrange so that the output was a static code of 511 ± 4 LSB. Because of this, the maximum magnitude of the output errors was 511.

When testing with static inputs, the code error limits could be tightened to ± 5 LSB because with a static output, clock

jitter was no longer a factor and with the analog signals turned off there was less overall noise in the system. This allowed for code errors between 6 and 23 LSB to be detected that were not detected when testing was done with dynamic inputs.

To determine if having a static input instead of a dynamic input had an impact on the testing, the code error SEU rate for testing with static inputs was recalculated using a code error limit of 23, the same as used for the dynamic inputs. The error cross section with dynamic inputs was 2 to 3 times higher than with static inputs (Fig. 10).

With static inputs, approximately 80% of the output code errors were less than 23 LSB, so that lowering the error limit from 23 LSB to 5 LSB captured about 5 times more errors (Fig. 10).

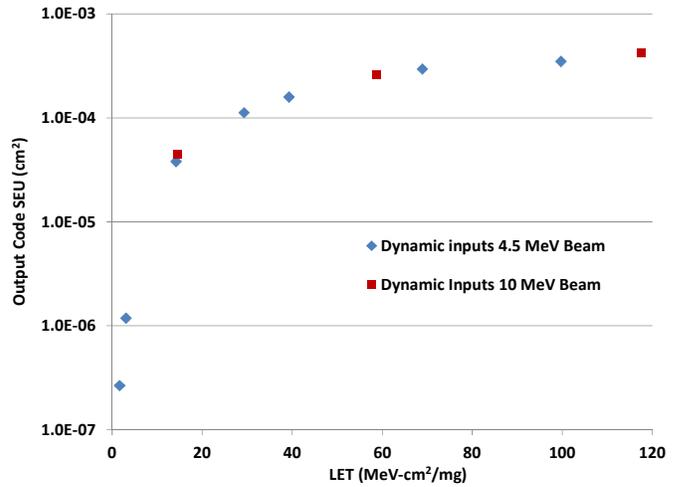


Fig. 9 Output code SEU cross section per channel vs. LET for testing with dynamic outputs.

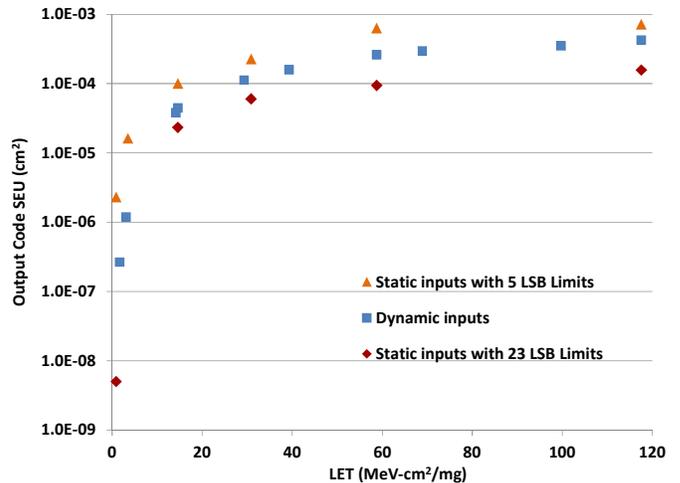


Fig. 10 Output code SEU cross sections for static inputs with error limits set at 5 and 23 LSB. The limit for the dynamic inputs was 23 LSB (errors with magnitude greater than 23 LSB were captured).

F. Output Clock SEU Test Results

Two types of output clock SEUs were detected. In some cases, there was a minor widening or narrowing of the clock pulse, which could be considered single event induced jitter

(Fig. 11) and in other cases, a full clock pulse would be affected and it would take another clock pulse for the clock to recover (Fig. 12). In all cases the clock output would recover within two clock cycles.

The output clock has a relatively low SEU cross section that is approximately two orders of magnitude lower than that of the ADC output (Fig. 13).

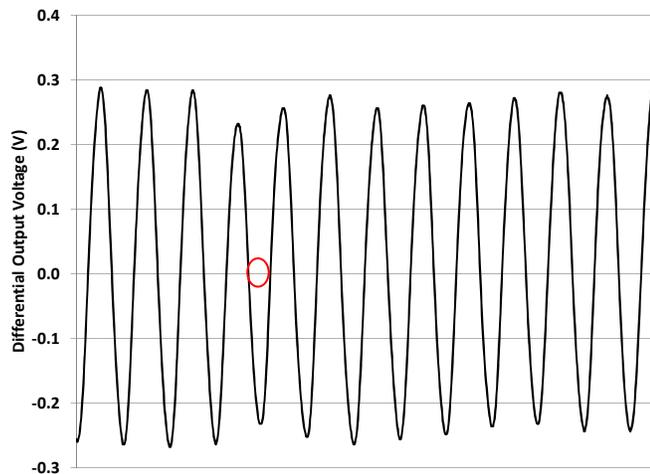


Fig. 11 Differential output clock (DLCKI) signal with pulse narrowing from an ion strike. The scope trigger point is circled. Since clock pulse narrowed, the falling edge of the clock was not within the expected trigger point, and an error was counted. The clock period recovered and the clock remained in phase.

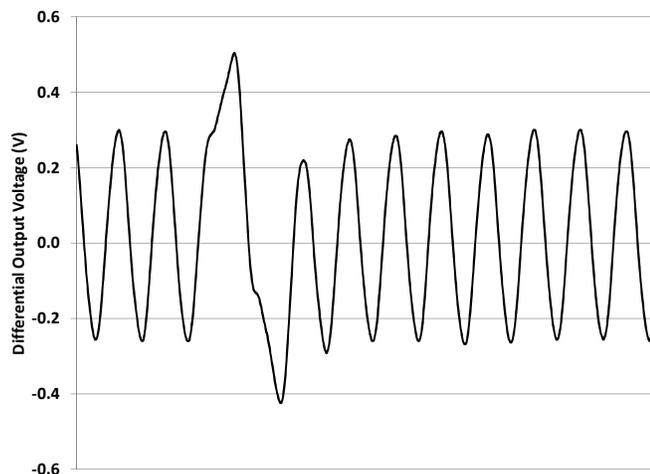


Fig. 12 Differential output clock (DLCKI) SEU that disrupted the clock for two cycles.

V. CONCLUSIONS

Texas Instruments' ADC12D1600CCMLS is SEL and SEFI immune. The output clock has a relatively low SEU cross section compared to the ADC output, indicating that clock upsets are not a significant contribution to the ADC output SEU Cross section.

No difference was detected in the SEL, SEFI and ADC output SEUs when either the 4.5 or 10 MeV/nuc beam was used, indicating that the 4.5 MeV/nuc beam has sufficient range penetration for the process used on this product.

Using dynamic inputs instead of static inputs for an ADC can impact the test results. Under the same test conditions, with the same limits, more output code errors were seen with dynamic inputs. However, testing with static limits allows tighter error limits to be set and smaller magnitude code errors can be counted. This is important, as a majority of the code errors are of lower magnitude.

Heavy ion testing of ultrahigh speed products remains a challenge due to the background noise and the less than optimum operating conditions required to do testing. Sometimes it is necessary to test the part under different conditions to get a better picture of the products heavy ion response.

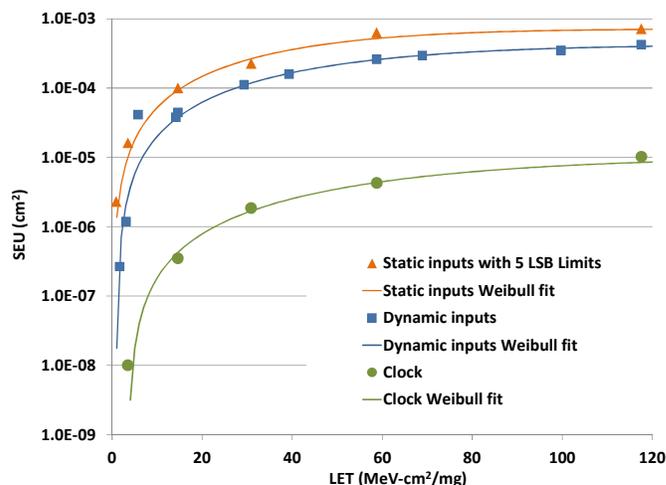


Fig. 13 SEU cross sections of the output code with static inputs with the error limit set at 5 LSB, the output code with the dynamic inputs with the error limit set at 23 LSB and the output clock. The Weibull fit parameters are shown in Table II.

TABLE II
WEIBULL FIT PARAMETERS FOR THE SEU CROSS SECTIONS

	A	Lo	W	s
Output code static inputs	4.21E-04	0.89	60	1.6
Output code dynamic inputs	7.15E-04	0	50	1.6
Clock	1.02E-05	3.49	80	1.6

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