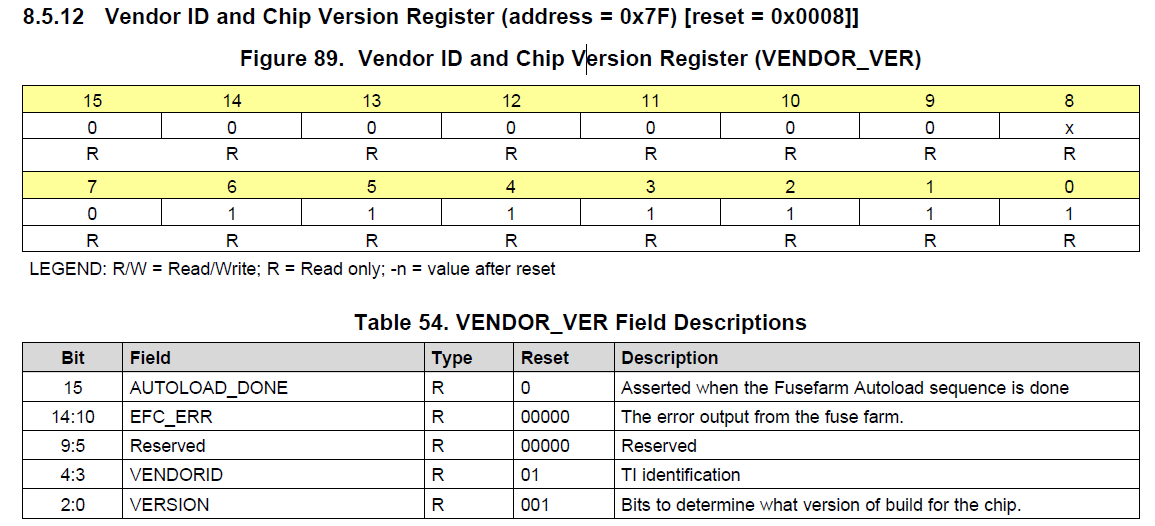
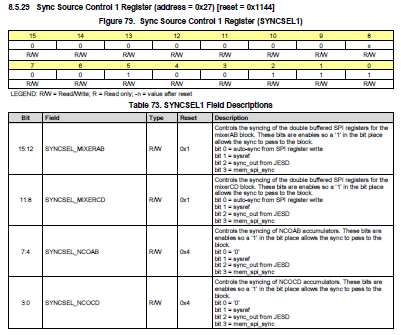
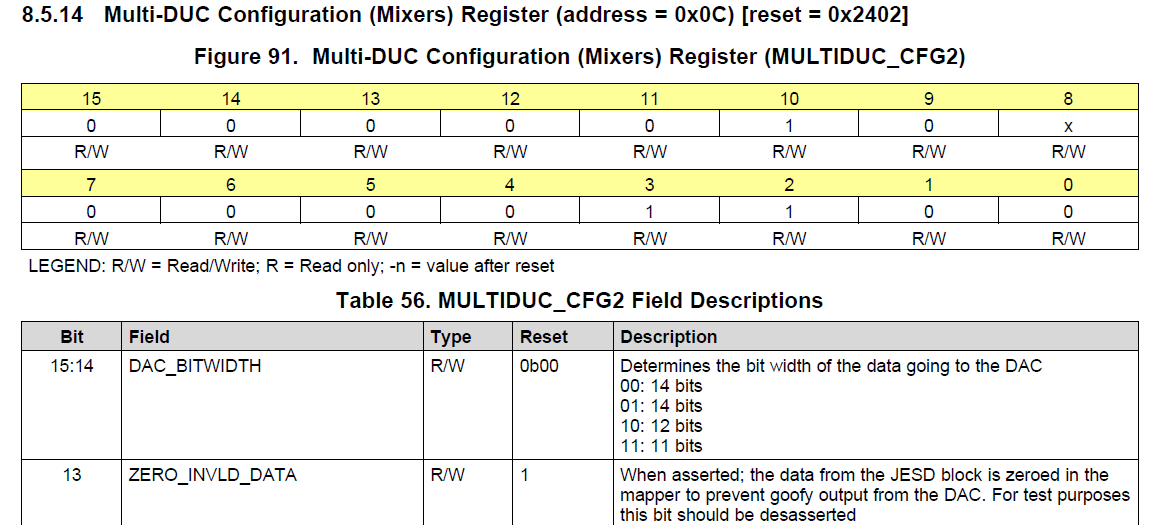
1. After power is applied and external reset is pulsed from low to high, verify bits [15:10] are 100000. If not, the fuse farm did not load. This has to occur before moving on.



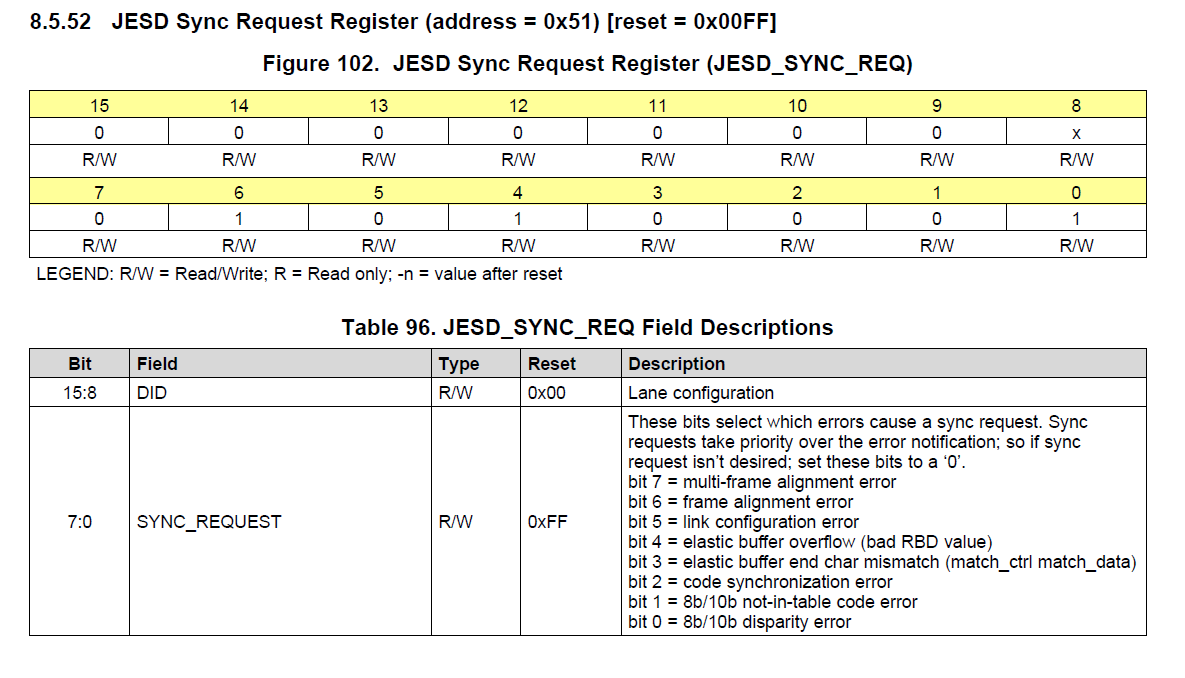
1. To check for SYSREF, run the DAC in NCO only mode and synchronize the NCO blocks to SYSREF. If SYSREF is present, the NCO will be unstable. Set address 0x27 in page 1 and 2 to 0x2828 to use SYSREF as the SYNC source. If SYSREF is present, the DAC output will now be many tones as the NCO will be constantly reset by the SYSREF signal. If SYSREF is now disabled, the DAC output will be a stable NCO tone.



1. If SYSREF is DC coupled, it must have a CM voltage of 0.5V and at least a 100mV swing.
2. To verify if ILA data is wrong, set bit 13 of register 0xC in page 1 and page 2 to enable the ILA check sequence. With this bit set to a “1”, if the DAC has no output, setting this bit to a “0” turns off the ILA checker, and if there was a problem with only the ILA data, and all other registers are configured properly, the DAC will then start sending an output.

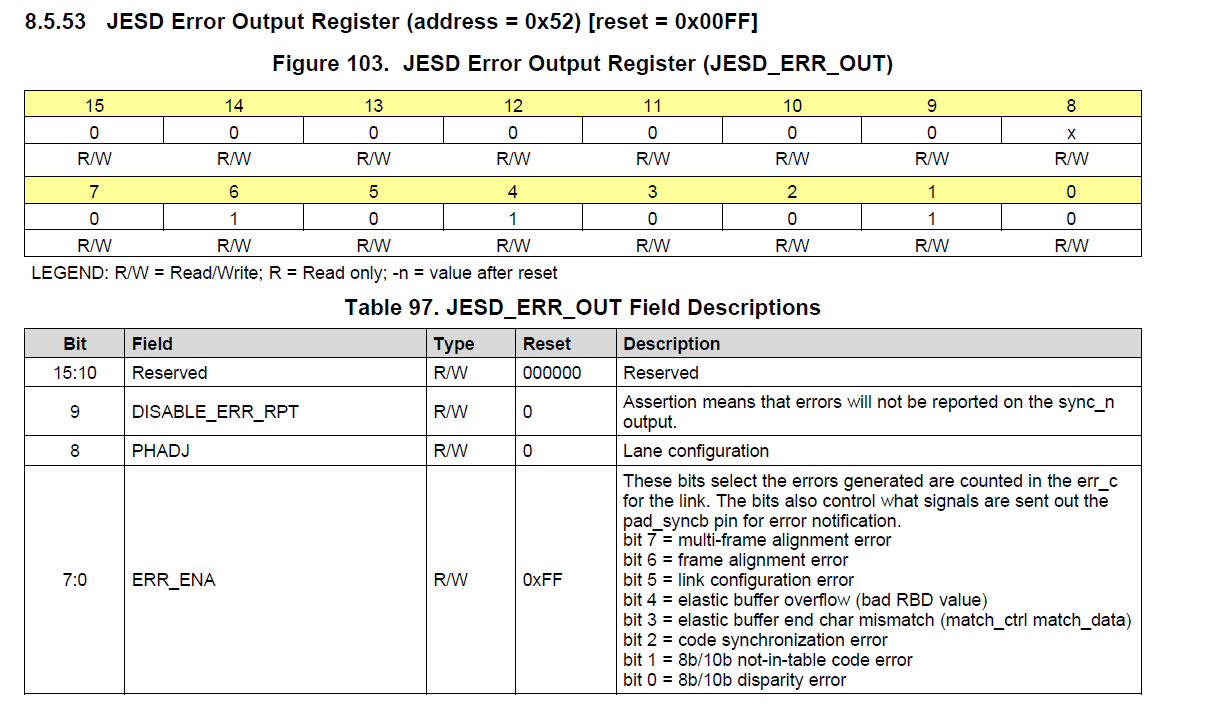


1. Lanes must be enables and assigned to the proper order.
2. Must do the proper reset sequence after the configuration file has been loaded.
3. SYSREF starts SYNC going low after JESD block is released from init state.
4. The following register determines which error will cause SYNC to de-assert (go low):

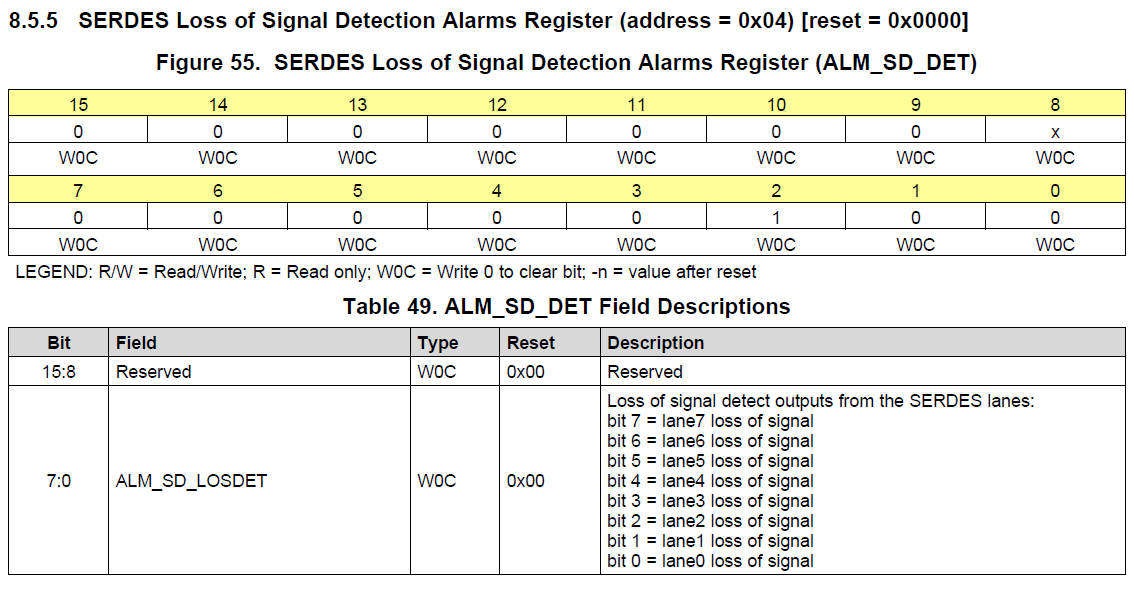


The default value used by TI is 0x001F.

1. This register reports JESD errors. GUI default is 0xFF. If bit 9 is set to 0, if any of the errors occur, a short SYNC pulse will occur.



Sdafsdf



If any lane reports a loss of signal, the device will pull SYNC low. These map directly to the input pins.

If JTAG is not used, TRSTN must be tied low.