Operational Amplifier Stability

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The Culprits

Capacitive Loads!

Reference Buffers!

Cable/Shield Drive!

MOSFET Gate Drive!

High Feedback Network Impedance!

Transimpedance Amplifiers!

High-Source Impedance or Low-Power Circuits!

Attenuators!
Just Plain Trouble!

Inverting Input Filter??

Output Filter??

Oscillator

Vin
Rg 10k

Cin 1u

Rf 100k

OPA

Vout

R1 10k

C1 10u

C5 100n

V1 5

R2 49k

Oscillator

VG1

0.00

10.00m

10.00m

0.00

Vfb

-37.08m

62.12m

Vo

-1.00

1.16

Time (s)

1.95m 2.23m 2.50m

VG1

0.00

10.00m

Vfb

-37.08m

62.12m

Vo

-1.00

1.16
Recognize Amplifier Stability Issues on the Bench

- **Required Tools:**
  - Oscilloscope
  - Step Generator

- **Other Useful Tools:**
  - Gain / Phase Analyzer
  - Network / Spectrum Analyzer
Recognize Amplifier Stability Issues

- Oscilloscope - Transient Domain Analysis:
  - Oscillations or Ringing
  - Overshoots
  - Unstable DC Voltages
  - High Distortion
Recognize Amplifier Stability Issues

- **Gain / Phase Analyzer - Frequency Domain:** Peaking, Unexpected Gains, Rapid Phase Shifts
Quick Op-Amp Theory and Bode Plot Review
Poles and Bode Plots

- **Pole Location** = $f_P$
- **Magnitude** = -20dB/Decade Slope
  - Slope begins at $f_P$ and continues down as frequency increases
  - Actual Function = -3dB down @ $f_P$
- **Phase** = -45°/Decade Slope through $f_P$
  - Decade Above $f_P$ Phase = -84.3°
  - Decade Below $f_P$ Phase = -5.7°
Zeros and Bode Plots

- **Zero Location** = \( f_Z \)
- **Magnitude** = +20dB/Decade Slope
  - Slope begins at \( f_Z \) and continues up as frequency increases
  - Actual Function = +3dB up @ \( f_Z \)
- **Phase** = +45°/Decade Slope through \( f_Z \)
  - Decade Above \( f_Z \) Phase = +84.3°
  - Decade Below \( f_Z \) Phase = 5.7°
Capacitor Intuitive Model

DC $X_C$

- OPEN

DC $< X_C < \text{Hi-f}$

- frequency controlled resistor
- $X_C = \frac{1}{(2\pi fC)}$

Hi-f $X_C$

- SHORT
Inductor Intuitive Model

DC $X_L$

SHORT

DC $< X_L <$ Hi-f

frequency controlled resistor

$X_L = 2\pi fL$

Hi-f $X_L$

OPEN
Op-Amp Intuitive Model

\[ K(f) \times \frac{V_{\text{out}}}{V_{\text{in}}} = V_{\text{diff}} \]

\[ R_{\text{in}} \]

\[ V_{\text{out}} \]

\[ V_{\text{diff}} \]

\[ V_{\text{in}} \]

\[ x1 \]

\[ R_0 \]

\[ \text{OPEN-LOOP GAIN/ PHASE vs FREQUENCY} \]

\[ \text{Frequency (Hz)} \]

\[ \text{Open-Loop Gain (dB)} \]
Op-Amp Loop Gain Model

\[
\begin{align*}
V_{\text{OUT}} / V_{\text{IN}} &= Acl = Aol / (1 + Aol \beta) \\
\text{If } Aol &> > 1 \text{ then } Acl \approx 1 / \beta \\
Aol &\text{: Open Loop Gain} \\
\beta &\text{: Feedback Factor} \\
Acl &\text{: Closed Loop Gain}
\end{align*}
\]
Amplifier Stability Criteria

\[ \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A_{\text{OL}}}{1 + A_{\text{OL}}\beta} \]

**If:** \( A_{\text{OL}}\beta = -1 \)

**Then:** \( \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A_{\text{OL}}}{0} \rightarrow \infty \)

If \( \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \infty \rightarrow \) Unbounded Gain

Any small changes in \( V_{\text{IN}} \) will result in large changes in \( V_{\text{OUT}} \) which will feed back to \( V_{\text{IN}} \) and result in even larger changes in \( V_{\text{OUT}} \rightarrow \text{OSCILLATIONS} \rightarrow \text{INSTABILITY} !! \)

**Aolβ:** Loop Gain

\( A_{\text{OL}}\beta = -1 \rightarrow \) Phase shift of \( \pm 180^\circ \), Magnitude of 1 (0dB)

**fcl:** frequency where \( A_{\text{OL}}\beta = 1 \) (0dB)

**Stability Criteria:**

At fcl, where \( A_{\text{OL}}\beta = 1 \) (0dB), Phase Shift < \( \pm 180^\circ \)

Desired Phase Margin (distance from \( \pm 180^\circ \) Phase Shift) \( \geq 45^\circ \)
What causes amplifier stability issues???
Fundamental Cause of Amplifier Stability Issues

- Too much delay in the feedback network
Cause of Amplifier Stability Issues

- Example circuit with too much delay in the feedback network

![Circuit Diagram]

- [Example circuit with too much delay in the feedback network]
Cause of Amplifier Stability Issues

- Real circuit translation of too much delay in the feedback network
Cause of Amplifier Stability Issues

- Same results as the example circuit
How do we determine if our system has too much delay??
Phase Margin

- Phase Margin is a measure of the “delay” in the loop

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

Phase (degrees)
0.00
45.00
90.00
135.00
180.00

Phase Margin

AOL

\(1/\beta\) (Unity-Gain)

fcl

Open-Loop

VG1 353.901124n
U2 OPA627E

VF1

V+
V-

VG1 353.901124n
+
-
+
U2 OPA627E
VF1

Open

Loop
Damping Ratio vs. Phase Margin

Small-Signal Overshoot vs. Damping Ratio

AC Peaking vs. Damping Ratio

Rate of Closure

Rate of Closure: Rate at which 1/Beta and AOL intersect

ROC = Slope(1/Beta) – Slope(AOL)

ROC = 0dB/decade – (-20dB/decade) = 20dB/decade
Rate of Closure and Phase Margin

Relationship between the AOL and 1/Beta rate of closure and Loop-Gain (AOL*B) phase margin

Rate of Closure = 20dB/decade

Phase Margin ≥ 45 degrees!
Rate of Closure and Phase Margin

So a pole in AOL or a zero in 1/Beta inside the loop will decrease AOL*B Phase!!
Rate of Closure and Phase Margin

AOL Pole

1/Beta Zero

Rate of Closure
= 40dB/decade!

Phase Margin
≈ 0 degrees!

Pole in AOL

Zero in 1/B

Phase Margin
≈ 0 degrees!
Testing for Rate of Closure in SPICE

- Break the feedback loop and inject a small AC signal

Short out the input source

Break the loop with L1 at the inverting input

Inject an AC stimulus through C1
Breaking the Loop

DC

AC

V-
V+
+
-
+
U1 OPA627E
Vo
Rf 1k
Rg 1k
+
VG2
Vfb
Vin
L1
C1
Plotting AOL, 1/Beta, and Loop Gain

AOL = \( \frac{V_o}{V_{in}} \)

1/Beta = \( \frac{V_o}{V_{fb}} \)

AOL*B = \( \frac{V_{fb}}{V_{in}} \)

Phase Margin = 80 degrees
Noise Gain

- Understanding Noise Gain vs. Signal Gain

**Signal Gain, $G = -1$**

**Signal Gain, $G = 2$**

\[ NG = 1 + ISGI = 2 \]

\[ NG = SG = 2 \]

Both circuits have a **NOISE GAIN** (NG) of 2.
Noise Gain

- Noise Gain vs. Signal Gain
  Gain of -0.1V/V, Is it Stable?

Signal Gain, $G = -0.1$

Noise Gain, $NG = 1.1$

If it’s unity-gain stable then it’s stable as an inverting attenuator!!!
Capacitive Loads
Capacitive Loads

**Unity Gain Buffer Circuits**

- Circuit with U1 OPA627E, Vin, Vo, CLoad 1uF
- Circuit with V+ V- Vin Vo

**Circuits with Gain**

- Circuit with R3 4.99k, R2 100k, Vin, Vo
- Circuit with Vin, Vo, CLoad 1u

**Waveforms**

- Vin (V) vs. Time (seconds)
- Vo (V) vs. Time (seconds)
Capacitive Loads – Unity Gain Buffers - Results

Determine the issue:

Pole in AOL!!

ROC = 40dB/decade!!

Phase Margin 0!!

NG = 1V/V = 0dB

Rate of Closure = 40dB/decade!

Phase Margin = 0.2 degrees!

AOL + AOL*B

1/B

Pole in AOL

Phase

AOL*B

Phase Margin = 0.2 degrees!
Capacitive Loads – Unity Gain Buffers - Theory
Capacitive Loads – Unity Gain Buffers - Theory

Transfer function:
\[ W(s) = \frac{1}{1 + R_o C_{\text{load}} s} \]

Gain (dB):
-80.00
-60.00
-40.00
-20.00
0.00

Frequency (Hz):
1.00 10.00 100.00 1k 10k 100k 1M 10M 100M

Phase (degrees):
-90.00
-45.00
0.00

Loaded AOL Pole

Gain (dB) Phase (degrees) Frequency (Hz)

Vin
\[ + \]

Ro 54

\[ - \]

VL

 Loaded AOL

\[ + \]

C_{\text{Load}} 1u

Loaded AOL

\[ f(\text{pole}) = \frac{1}{2 \pi R_o C_{\text{Load}} s} \]
Capacitive Loads – Unity Gain Buffers - Theory

AOL

AOL Load

Loaded AOL

X
Stabilize Capacitive Loads – Unity Gain Buffers
Stability Options

Unity-Gain circuits can only be stabilized by modifying the AOL load.
Method 1: Riso

![Circuit Diagram](attachment:image.png)
**Method 1: Riso - Results**

**Theory:** Adds a zero to the Loaded AOL response to cancel the pole

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Gain (dB)</th>
<th>Phase [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-40.00</td>
<td>0.00</td>
</tr>
<tr>
<td>10</td>
<td>-20.00</td>
<td>45.00</td>
</tr>
<tr>
<td>100</td>
<td>0.00</td>
<td>90.00</td>
</tr>
<tr>
<td>1,000</td>
<td>20.00</td>
<td>135.00</td>
</tr>
<tr>
<td>10,000</td>
<td>40.00</td>
<td>180.00</td>
</tr>
<tr>
<td>100,000</td>
<td>60.00</td>
<td></td>
</tr>
<tr>
<td>1,000,000</td>
<td>80.00</td>
<td></td>
</tr>
</tbody>
</table>

**Gain (dB):**

-40.00  -20.00  0.00  20.00  40.00  60.00  80.00  100.00  120.00

**Phase [deg]:**

0.00  45.00  90.00  135.00  180.00

**Rate of Closure:**

\[ \text{Rate of Closure} = 20 \text{dB/decade} \]

**Phase Margin:**

\[ \text{Phase Margin} = 87.5 \text{degrees}! \]
Method 1: Riso - Results

When to use: Works well when DC accuracy is not important, or when loads are very light
Method 1: Riso - Theory
Method 1: Riso - Theory

Transfer function:

Loaded AOL(s) = \frac{1 + C_{Load} \cdot R_{iso} \cdot s}{1 + (R_o + R_{iso}) \cdot C_{Load} \cdot s}

Pole Equation:

f(pole) = \frac{1}{2 \cdot \pi \cdot (R_o + R_{iso}) \cdot C_{Load} \cdot s}

Zero Equation:

f(zero) = \frac{1}{2 \cdot \pi \cdot R_{iso} \cdot C_{Load} \cdot s}
Method 1: Riso - Theory
Method 1: Riso - Design

Ensure Good Phase Margin:

1.) Find: fcl and f(AOL = 20dB)
2.) Set Riso to create AOL zero:
   - Good: f(zero) = Fcl for PM ≈ 45 degrees.
   - Better: f(zero) = F(AOL = 20dB) will yield slightly less than 90 degrees phase margin

fcl = 222.74kHz
f(AOL = 20dB) = 70.41kHz

Zero Equation:
\[ f(zero) = \frac{1}{2 \pi R_{iso} C_{Load} s} \]
Method 1: Riso - Design

Ensure Good Phase Margin: Test

\[ f(AOL = 20\text{dB}) = 70.41\text{kHz} \]

\[ \rightarrow \text{Riso} = 2.26\text{Ohms} \]

\[ f(\text{cl}) = 222.74\text{kHz} \]

\[ \rightarrow \text{Riso} = 0.715\text{Ohms} \]

\[
f\text{(zero)} = \frac{1}{2 \cdot \pi \cdot R_{iso} \cdot C_{Load} \cdot s}
\]
Method 1: Riso - Design

Prevent Phase Dip:

Place the zero less than 1 decade from the pole, no more than 1.5 decades away

Good: 1.5 Decades: \( F(\text{zero}) \leq 35 \times F(\text{pole}) \) \( \rightarrow \) \( \text{Riso} \geq \frac{\text{Ro}}{34} \) \( \rightarrow \) 70° Phase Shift

Better: 1 Decade: \( F(\text{zero}) \leq 10 \times F(\text{pole}) \) \( \rightarrow \) \( \text{Riso} \geq \frac{\text{Ro}}{9} \) \( \rightarrow \) 55° Phase Shift

\( \text{Riso} = \frac{\text{Ro}}{9} \)

\( \text{Riso} = \frac{\text{Ro}}{34} \)

\( F(\text{pole}) = 2.65\text{kHz} \)

\( F(\text{zero}) = 26.5\text{kHz} \)

\( \text{PM}_{\text{min}} = 35° \)

\( F(\text{pole}) = 2.86\text{kHz} \)

\( F(\text{zero}) = 100.2\text{kHz} \)

\( \text{PM}_{\text{min}} = 20° \)
Method 1: Riso - Design

Prevent Phase Dip: Ratio of Riso to Ro

If \( \text{Riso} \geq 2 \times \text{Ro} \rightarrow F(\text{zero}) = 1.5 \times F(\text{pole}) \rightarrow \sim 10^\circ \text{ Phase Shift} 
**Almost completely cancels the pole.**

\[ \text{Riso} = \text{Ro} \times 2 \]

**Phase Shift vs. \( \frac{\text{Riso}}{\text{Ro}} \)**

- **PM_min = 80°**
Method 1: Riso – Design Summary

Summary:

1.) Ensure stability by placing $F_{\text{zero}} \leq F(AOL=20\text{dB})$
2.) If $F_{\text{zero}}$ is $> 1.5$ decades from $F(\text{pole})$ then increase $R_{\text{iso}}$ up to at least $R_o/34$
3.) If loads are very light consider increasing $R_{\text{iso}} > R_o$ for stability across all loads
Method 1: Riso - Disadvantage

Disadvantage:

Voltage drop across Riso may not be acceptable
Method 2: Riso + Dual Feedback
**Method 2: Riso + Dual Feedback**

**Theory:** Features a low-frequency feedback to cancel the Riso drop and a high-frequency feedback to create the AOL pole and zero.

![Circuit Diagram](image)

Graph showing the frequency response with labels:
- **Gain (dB)**
- **Phase (degrees)**

- **Rate of Closure** = 20dB/decade
- **Phase Margin** = 87.5 degrees!
Method 2: Riso + Dual Feedback

**When to Use:** Only practical solution for very large capacitive loads ≥ 10uF

When DC accuracy must be preserved across different current loads
Method 2: Riso + Dual Feedback - Design

Ensure Good Phase Margin:

1.) Find: fcl and f(AOL = 20dB)
2.) Set Riso to create AOL zero:
   Good: f(zero) = Fcl for PM \approx 45 degrees.
   Better: f(zero) = F(AOL = 20dB) will yield slightly less than 90 degrees phase margin
3.) Set Rf so Rf >> Riso
   \[ R_f \geq (R_{iso} \times 100) \]
4.) Set Cf \geq (200 \times R_{iso} \times C_{load})/R_f

\[ f_{cl} = 222.74kHz \]
\[ f(AOL = 20dB) = 70.41kHz \]

Zero Equation:
\[ f(zero) = \frac{1}{2 \cdot \pi \cdot R_{iso} \cdot C_{load} \cdot s} \]
Method 2: Riso + Dual Feedback - Summary

Ensure Good Phase Margin (Same as “Riso” Method):

1.) Set Riso so $f(\text{zero}) = F(\text{AOL} = 20\,\text{dB})$
2.) Set $R_f$: $R_f \geq (Riso \times 100)$
3.) Set $C_f$: $C_f \geq (200 \times Riso \times C_{\text{load}})/R_f$

Phase Margin = 87.5 degrees!
Capacitive Loads – Circuits with Gain
Capacitive Loads – Circuits with Gain

![Circuit Diagram]

- **Rg**: 4.99k
- **Rf**: 100k
- **U1**: OPA627E
- **Vo**: Output
- **VG1**: 0
- **VL**: 100n

![Graph]

- **Time (seconds)**: 0.00, 150.00u, 300.00u
- **Voltage (V)**: 0.00, 10.00m, 20.00m, 30.00m, 40.00m
Capacitive Loads – Circuits With Gain - Results

Same Issues as Unity Gain Circuit

Pole in AOL!!

ROC = 40dB/decade!!

Phase Margin = 10°!!
Stabilize Capacitive Loads – Circuits with Gain
Stability Options – Circuits with Gain

Circuits with gain can be stabilized by modifying the AOL load and by modifying 1/Beta
Method 1 + Method 2

Methods 1 and 2 work on circuits with gain as well!

Method 1: Riso

Method 2: Riso+Dual Feedback
Method 3: Cf

- U1 OPA627E
- CLoad 100n
- Vo
- Rf 100k
- Rg 4.99k
- C1 27p
- VG1
- V- V+
Method 3: Cf - Results

Theory: 1/Beta compensation. Cf feedback capacitor causes 1/Beta to decrease at -20dB/decade and if placed correctly will cause the ROC to be 20dB/decade.

Gain (dB)
-40.00  -20.00   0.00   20.00   40.00   60.00   80.00   100.00   120.00
Frequency (Hz)
1.00   10.00   100.00   1.00k   10.00k   100.00k   1.00M   10.00M   100.00M
Phase (deg)
0.00   45.00   90.00   135.00   180.00

ROC = 20dB/decade
PM = 68°
Method 3: Cf - Results

When to use: Especially effective when NG is high, \( \geq 30\text{dB} \).

Systems where a bandwidth limitation is not an issue
- Limits closed-loop bandwidth at \( \frac{1}{2\pi RfCf} \)

![Circuit Diagram]

<table>
<thead>
<tr>
<th>Time (s)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>150.00u</td>
<td>5.00m</td>
</tr>
<tr>
<td>300.00u</td>
<td>10.00m</td>
</tr>
</tbody>
</table>

*Figure showing a step response with rising voltage.*
Method 3: Cf - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL while its slope is -20dB/decade.
Therefore: \( f(1/B \text{ pole}) < f(\text{cl}_\text{unmodified}) \)
\( f(1/B \text{ zero}) > f(\text{AOL} = 0\text{dB}) \)

\[ f(\text{cl}_\text{unmodified}) = 152.13\text{kHz} \]
\[ f(\text{AOL} = 0\text{dB}) = 704.06\text{kHz} \]

**1/B Pole Equation:**
\[ f(1/B \text{ pole}) = \frac{1}{2\cdot\pi\cdot R_f \cdot C_f} \]

**1/B Zero Equation:**
\[ f(1/B \text{ zero}) = \frac{1}{2\cdot\pi\cdot (R_g || R_f) \cdot C_f} \]
Method 3: Cf - Design

Ensure Good Phase Margin:

1.) Find \( f(AOL=0dB) \)
2.) Set \( f(1/B \text{ zero}) \) by choosing \( Cf \):
   
   Good: Set \( f(1/B \text{ zero}) = f(AOL = 0dB) \) for \( PM \approx 45 \) degrees.
   
   Better: Set \( f(1/B \text{ zero}) \) so \( AOL @ f(cl) = \frac{1}{2} \) Low-Frequency NG in dB

\[
 f(AOL = 0dB) = 704.06kHz
\]

\[f(1/B \text{ zero}) = \frac{1}{2 \cdot \pi \cdot (R_g || R_f) \cdot C_f}\]
Method 3: Cf – Design - Summary

Summary:

1.) Ensure stability by placing:
   a) $f(1/B \text{ zero}) \geq f(AOL = 0\text{dB})$
   b) $f(1/B \text{ pole}) \leq f(cl\_unmodified)$
2.) Try to adjust the zero location so the $1/B$ curve crosses the AOL curve in the middle of the $1/B$ span allowing for shifts in AOL

Final Circuit

Gain (dB)

Phase (degrees)

PM = 68°
Method 4: Noise-Gain

```
Rg 4.99k
Rn 75
Cn 820n
VG1

U1 OPA627E

Vo

CLoad 100n
```
Method 4: Noise Gain - Results

**Theory:** 1/Beta compensation. Raise high-frequency 1/Beta so the ROC occurs before the AOL pole causes the AOL slope to change.
Method 4: Noise Gain - Results

When to use: Better for lighter capacitive loading

When $\text{AOL} @ f(\text{AOL pole}) < (\text{Closed loop gain} + 20\text{dB})$

Due to the increase in noise gain, this approach may not be practical when required noise gain is greater than the low-frequency signal gain by more than $\sim 25-30\text{dB}$.
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL above the AOL pole.
Therefore: \(|\text{High-Freq NG}| > |\text{AOL}| @ f(\text{AOL pole})\)
\(f(1/B \text{ zero}) < f(\text{AOL} = \text{High-Freq NG})\)

\(|\text{AOL}| @ f(\text{AOL pole}) = 52.11\text{dB}\)
\(f(\text{AOL pole}) = 29.49\text{kHz}\)

High-Freq Noise-Gain Equation:
\[
\text{HF NG} = \frac{R_f}{(R_g \parallel R_n)}
\]

1/B Zero Equation:
\[
f(1/B \text{ zero}) = \frac{1}{2 \pi R_n C_n}
\]

1/B Pole Equation:
\[
f(1/B \text{ pole}) = \frac{1}{2 \pi (R_n + (R_g \parallel R_f) \cdot C_f)}
\]
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

1.) Find \( f(\text{AOL pole}) \) and \( |\text{AOL}| @ f(\text{AOL pole}) \)
2.) Set High-Freq Noise-Gain by choosing \( R_n \):
   - Good: \( |\text{HF NG}| \geq |\text{AOL}| @ f(\text{AOL pole}) \)
   - Better: \( |\text{HF NG}| \geq |\text{AOL}| @ f(\text{AOL pole}) + 10\text{dB} \)

High-Freq Noise-Gain Equation:
\[
\text{HF NG} = \frac{R_f}{(R_g || R_n)}
\]

\( |\text{AOL}| @ f(\text{AOL pole}) \) = 52.11\text{dB}

\( f(\text{AOL pole}) \) = 29.49kHz
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

3.) Find \( f(\text{cl\_modified}) = f(\text{AOL @ |HF NG|}) \)
4.) Set \( f(1/B \text{ zero}) \) by choosing \( C_n \):
   \[
   \begin{align*}
   \text{Good:} & \quad f(1/B \text{ zero}) \leq f(\text{cl\_modified}) \\
   \text{Better:} & \quad f(1/B \text{ zero}) \leq f(\text{cl\_modified}) / 3.5 \quad (\sim \frac{1}{2} \text{ decade})
   \end{align*}
   \]

\( f(\text{cl\_modified}) = 29.49\text{kHz} \)

High-Freq Noise-Gain Equation:
\[
\text{HF NG} = \frac{R_f}{(R_g \parallel R_n)}
\]
Method 4: Noise Gain - Summary

Summary:

1.) Ensure stability by setting:
   a) \(|HF \ NG| \geq (|AOL| @ f(AOL \ pole) + 10\text{dB})
   b) \(f(1/B \ zero) \leq f(cl_{\text{modified}}) / 3.5\)

Final Circuit

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00
Frequency (Hz)
1.00
10.00
100.00
1.00k
10.00k
100.00k
1.00M
10.00M
100.00M

Phase (degrees)
0.00
45.00
90.00
135.00
180.00

Gain (dB) Phase (degrees) Frequency (Hz)
100
PM = 56°
Method 4: Noise Gain

Quick reminder that inverting and non-inverting noise gain circuits are different!

\[ \text{U1 OPA627E} \]

\[ + \quad - \]

\[ Rg 4.99k \quad Rf 100k \]

\[ Rn 75 \quad Cn 820n \]

\[ V_+ \quad V_- \]

\[ C_{\text{Load}} 100n \]

\[ V_o \]
Circuits with High Feedback Network Impedance
Circuits with High Feedback Network Impedance

![Circuit Diagram]

- U1 OPA627E
- Rg 499k
- Rf 499k
- Cstray 20p
- Vin
- Vo

- Vo (V)
- Vin (V)

- Time (seconds)
  - 0.00 150.00u 300.00u

- Voltage Levels:
  - V-:
  - V+:
  - +:
  - -:

- Resistance:
  - Rg 499k
  - Rf 499k

- Components:
  - Cstray 20p
Circuits with High Feedback Network Impedance

Determine the issue:

Zero in $1/B$!!

$ROC = 40\text{dB/decade}!!$

Phase Margin 2!!

Gain (dB)

-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)

1.00
10.00
100.00
1.00k
10.00k
100.00k
1.00M
10.00M
100.00M

Phase (deg)

0.00
45.00
90.00
135.00
180.00

PM = 2°

$1/B$ Zero

$ROC = 40\text{dB/decade!}$
Circuits with High Feedback Network Impedance - Theory
Beta Pole & 1/Beta Zero Equation:

\[
f(B \text{ pole}) = f(1/\text{B zero}) = \frac{1}{2 \pi (R_g || R_f) C_{in}}
\]
Stabilize Circuits With High Feedback Network Impedance
Stability Options – Zero in 1/Beta

The only practical option is to add a pole to cancel the 1/Beta Zero
Method 1: Cf

![Circuit Diagram]

- \( R_g \): 499k
- \( R_f \): 499k
- \( C_{stray} \): 20p
- \( C_f \): 21p
- \( U_1 \): OPA627E
- \( V_G 1 \)
- \( V_o \)
Method 1: Cf - Results

Theory: 1/Beta compensation. Cf feedback places a pole in 1/Beta to cancel the zero from the input capacitance.
Method 1: Cf - Results

When to use: Almost always a safe design practice.
Limits gain at $1/(2\pi R_f C_f)$

![Circuit Diagram]

![Graph](Time (seconds))

When to use: Almost always a safe design practice. Limits gain at $1/(2\pi R_f C_f)$.
# Method 1: Cf - Design

## Ensure Good Phase Margin:

For 20dB/decade ROC, the 1/Beta pole must flatten the 1/Beta Zero before $f(cl)$

Therefore $f(1/$Beta pole$) \leq f(cl)$

### $f(cl) = 445.6kHz$

### 1/B Pole Equation:

$$f(1/$B pole$)=\frac{1}{2\cdot\pi\cdot R_f\cdot C_f}$$

### 1/B Zero Equation:

$$f(1/$B zero$)=\frac{1}{2\cdot\pi\cdot (R_g \parallel R_f)\cdot C_{in}}$$
Method 1: Cf - Design

Ensure Good Phase Margin:

1.) Find \( f(\text{cl}) \)
2.) Set \( f(1/B \text{ pole}) \) by setting \( Cf \):
   - Good: \( f(1/B \text{ pole}) \leq f(\text{cl}) \)
   - Better: \( f(1/B \text{ pole}) \leq f(\text{cl})/3.5 \) (~ \( \frac{1}{2} \) decade)

1/B Pole Equation:
\[
f(1/B \text{ pole}) = \frac{1}{2\pi R_f C_f}
\]

1/B Zero Equation:
\[
f(1/B \text{ zero}) = \frac{1}{2\pi (R_g + R_f) C_{in}}
\]
Method 1: Cf - Summary

Summary:
1.) Ensure stability by setting $f(1/B \text{ pole}) \leq f(\text{cl})/3.5 \ (\sim \frac{1}{2} \text{ decade})$
Ro vs. Zo
When Ro is really Zo!!

Vos 80.0432u

Vos -25.3845uV

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY
With Complex Zo, Accurate Models are Key!

Gain (dB)
-60.00
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00
140.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

Phase (degrees)
-90.00
-45.00
0.00
45.00
90.00
135.00
180.00

PM = -77°!!

ROC = 60dB/decade!

AOL ÷ AOL*B
With Complex Zo, Accurate Models are Key!

Vos -25.3845uV

U1 OPA2376

Vo

IG1

Frequency (Hz)

Impedance (Ohms)

Gain (dB)
Questions/Comments?

Thank you!!

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