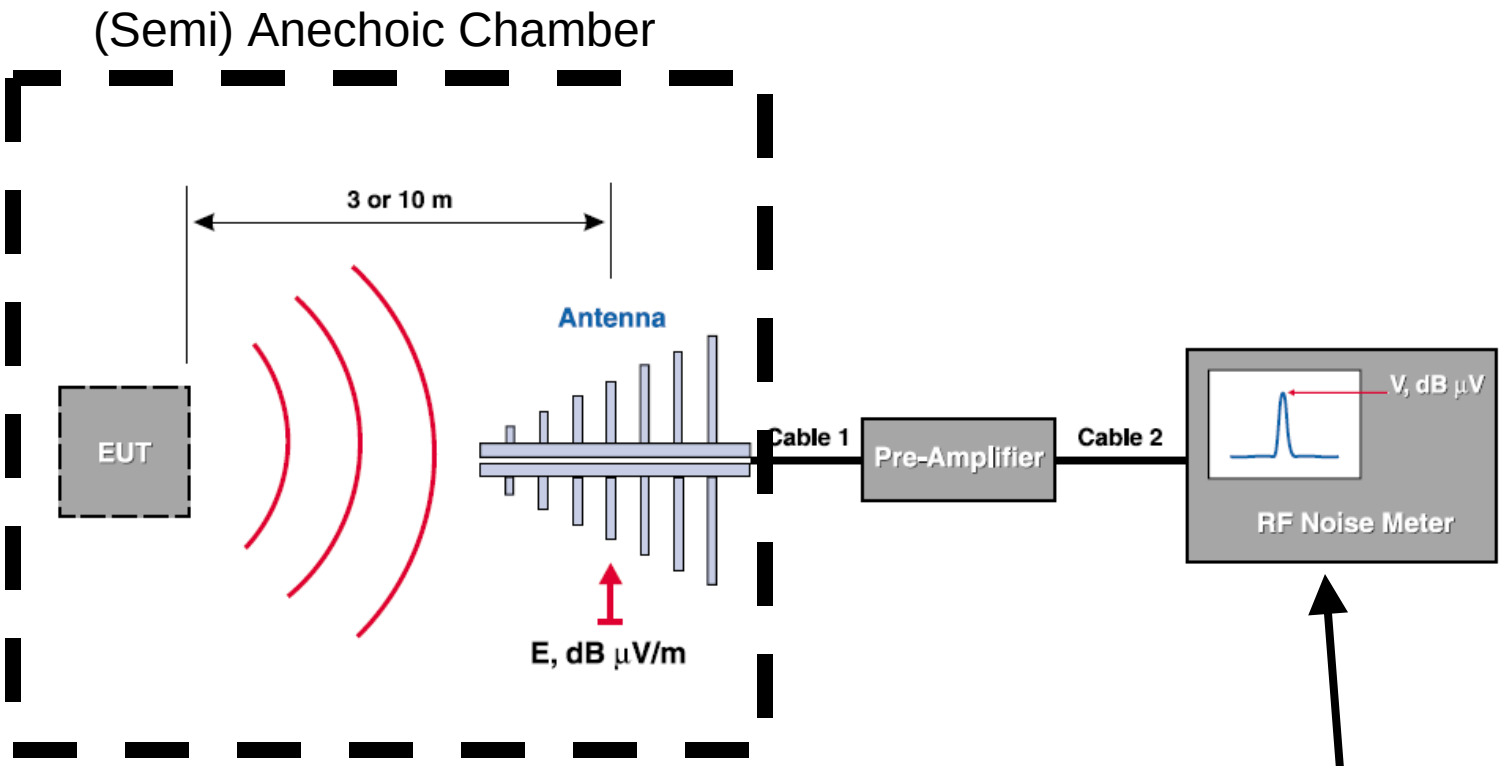
How to Overcome EMI Problems by Using Clock Generators Equipped with Spread-Spectrum Clocking (SSC)

Agenda

- How Radiated Emissions are measured
- Clocks and EMI
- Solutions to reduce EMI generated by clocks
  - SSC
  - Slew Rate Control
  - Sine wave

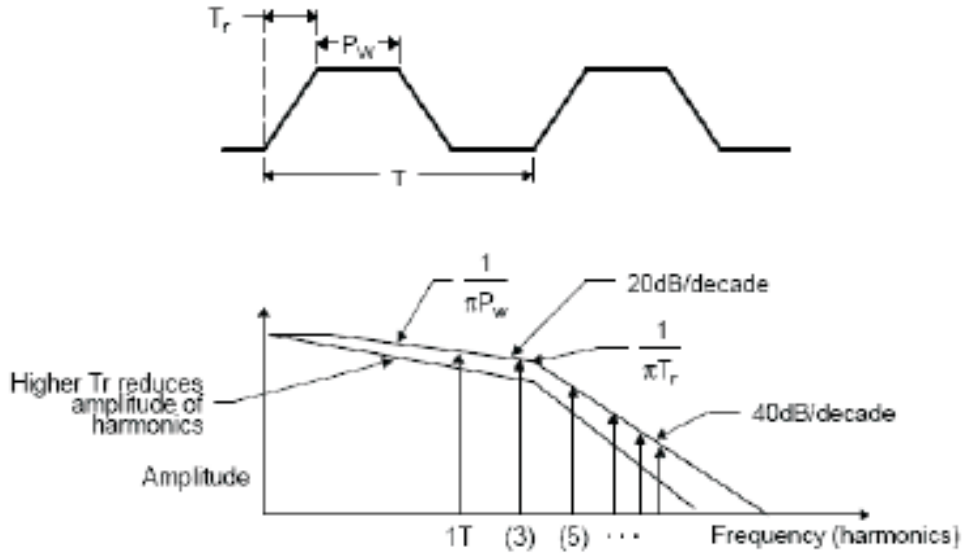
Measuring Radiated Emissions



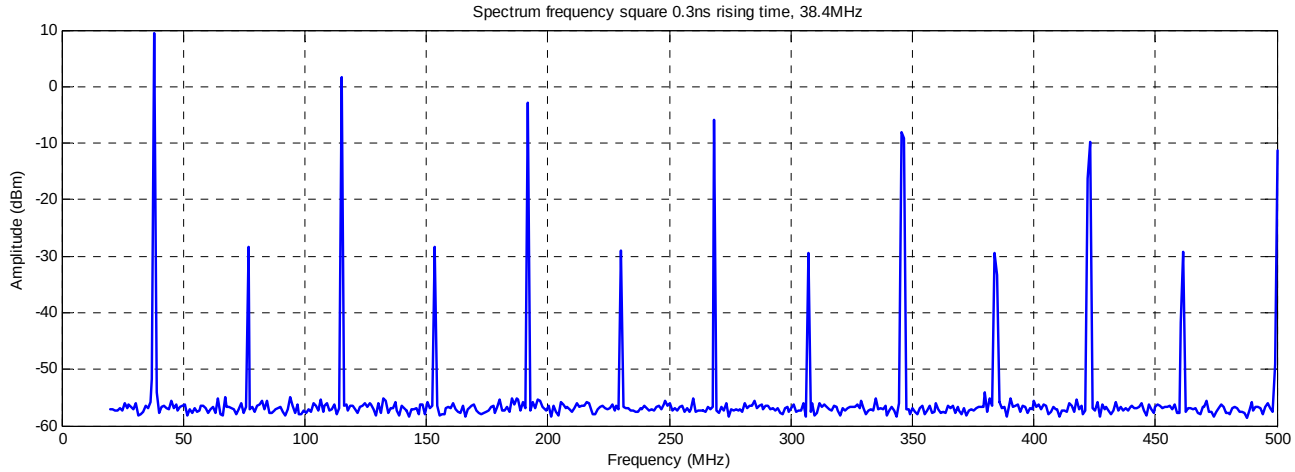
IF filter sweeps with 120kHz Bandwidth

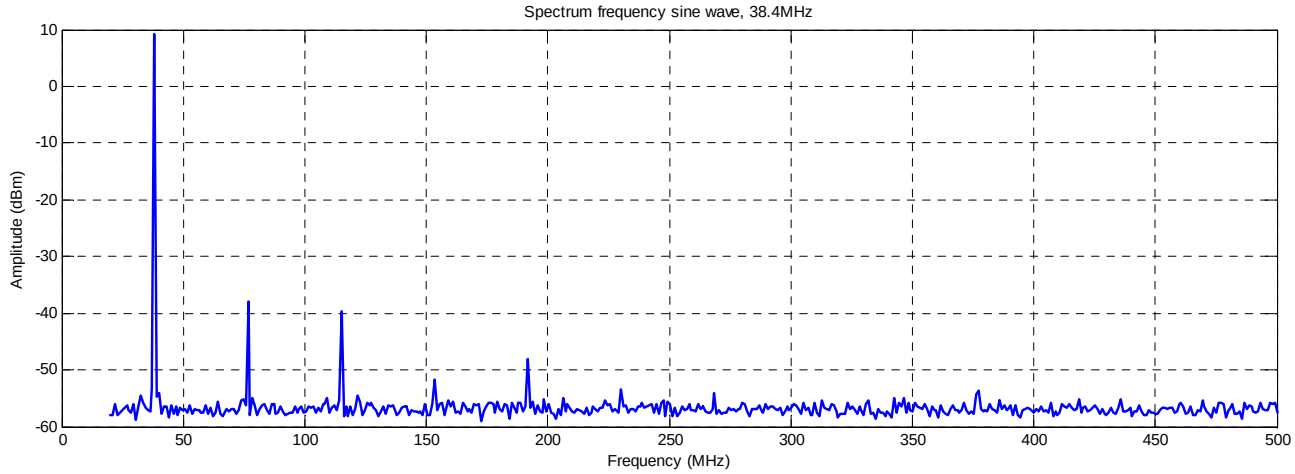
Clocks and EMI

- **Ideal Clocks have short rise and fall times to avoid Duty Cycle Distortion and other problems**
- **For good rise and fall times a greater number of odd harmonics is necessary**
- **Even low frequency clocks can have components that can cause high frequency EMI**



Square vs. Sine Wave





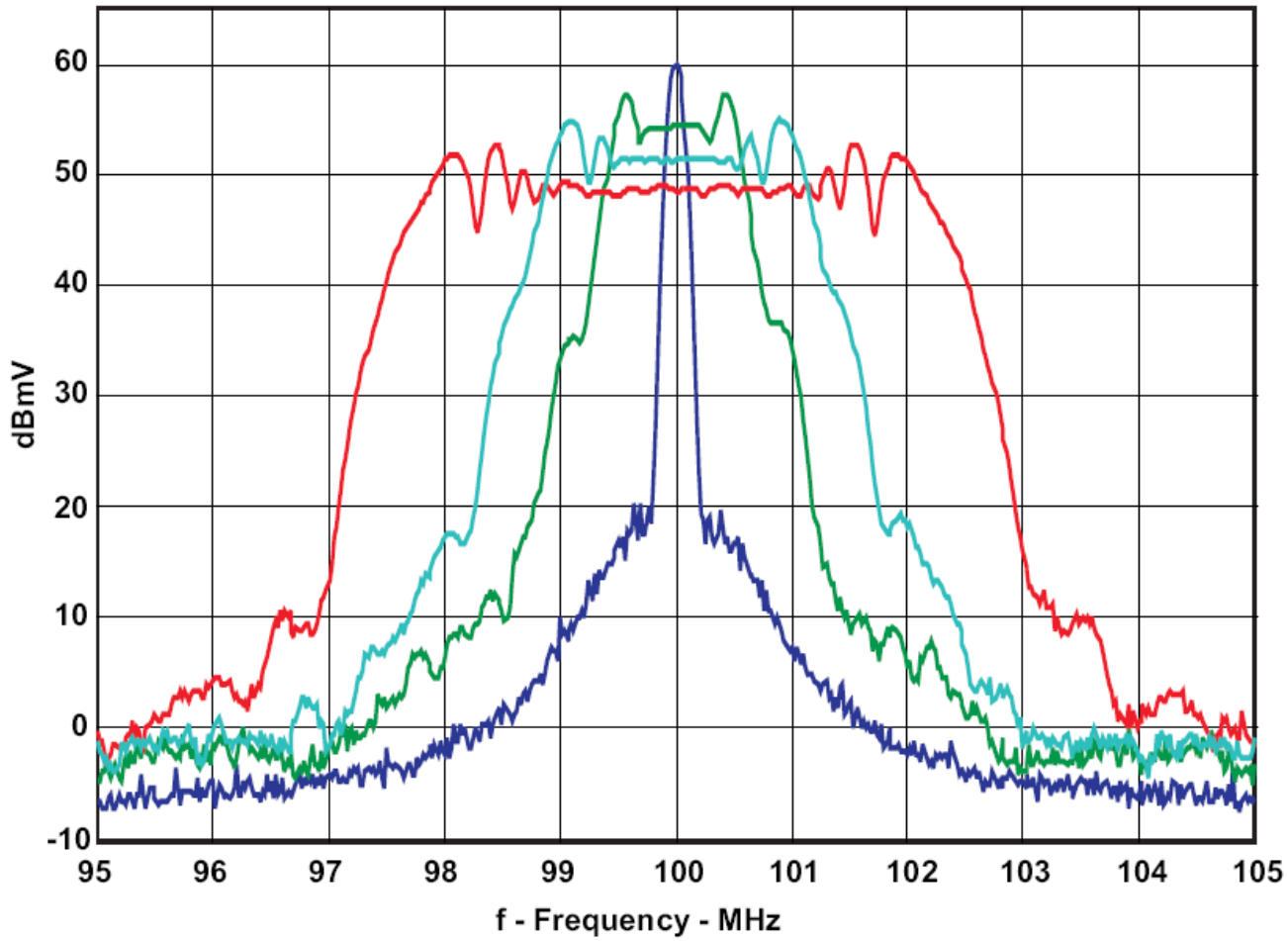
Spread-Spectrum Clocking (SSC)

- SSC is a way to reduce the emitted energy from a signal
- It simply distributes energy from a single frequency to a frequency band near the original frequency
- If only a part of the signal is emitted, the radiated energy is significantly less
- A welcome side effect is that only a part of the original signal is losing energy and therefore also most of the original signal is still available

SSC Parameters

- Amount of SSC
- Center or down spread
- SSC profile
- Modulation frequency

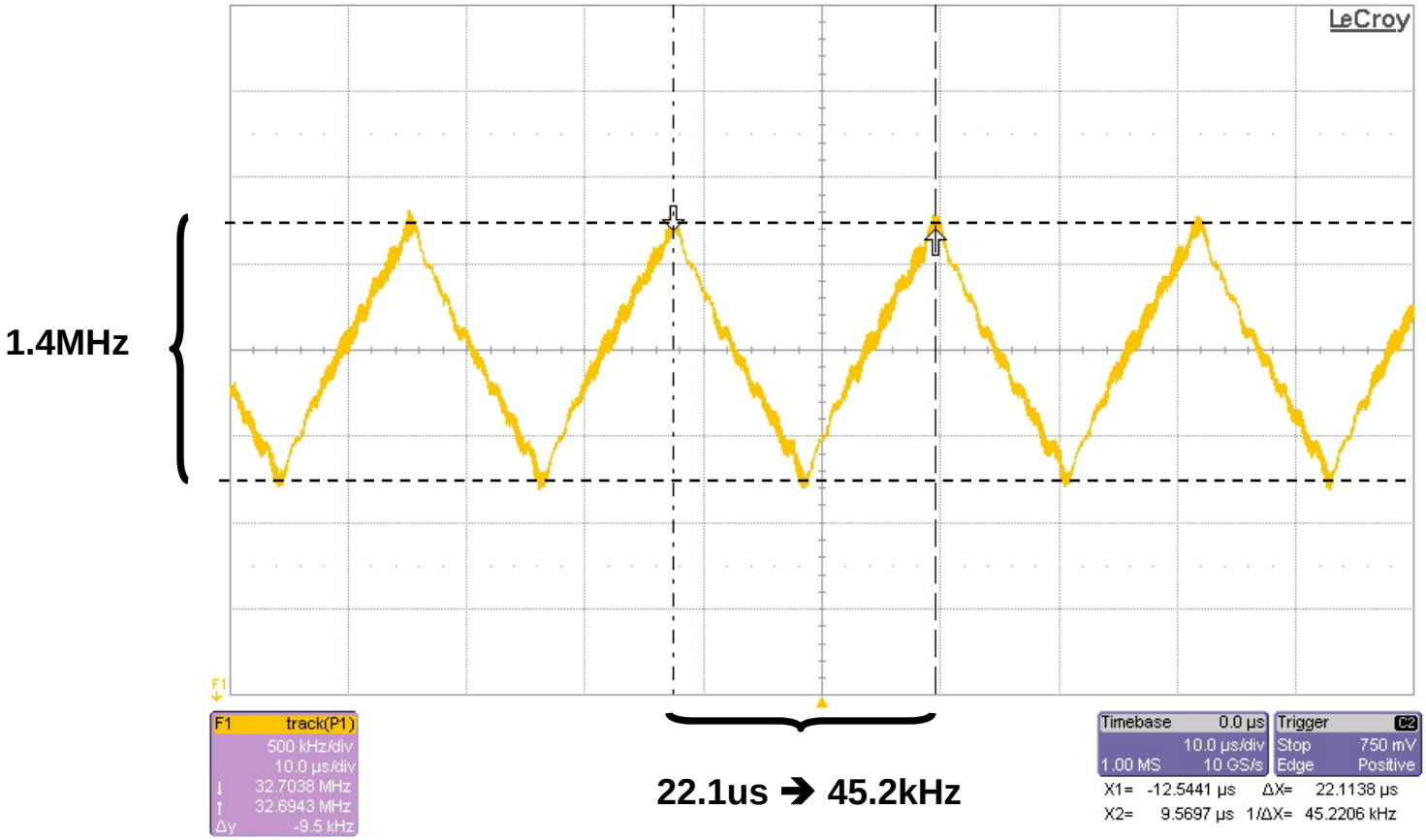
SSC in the Frequency Domain



CDCS502 With a 25-MHz Crystal, FS = 1, Fout = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

SSC in the Time Domain

- **Frequency vs cycles**



CDCS502 Jitter (multiply x 1)

- F_{in} = 25MHz crystal
- F_{out} = 25MHz

SSC amount	Cycle – Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5	93	512
±1	117	1001
±2	195	1990

CDCS502 Jitter (multiply x 4)

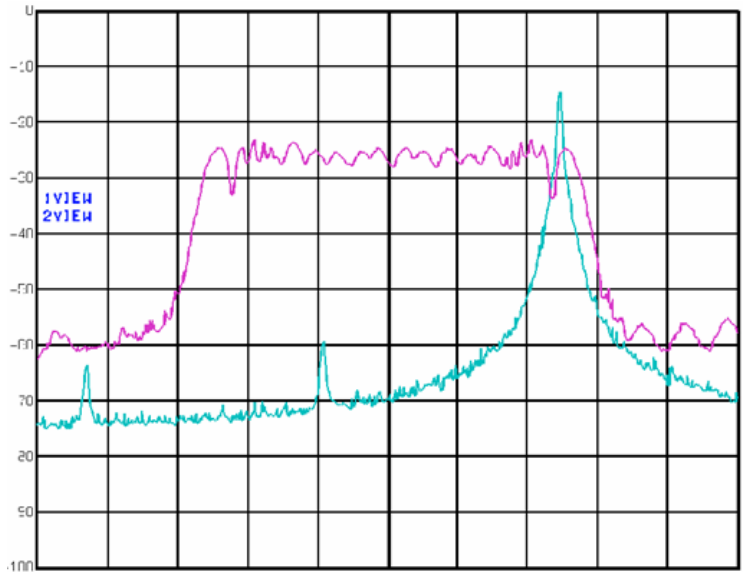
- F_{in} = 25MHz crystal
- F_{out} = 100MHz

SSC amount	Cycle – Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5	72	178
±1	72	292
±2	78	529

Different Methods of SSC

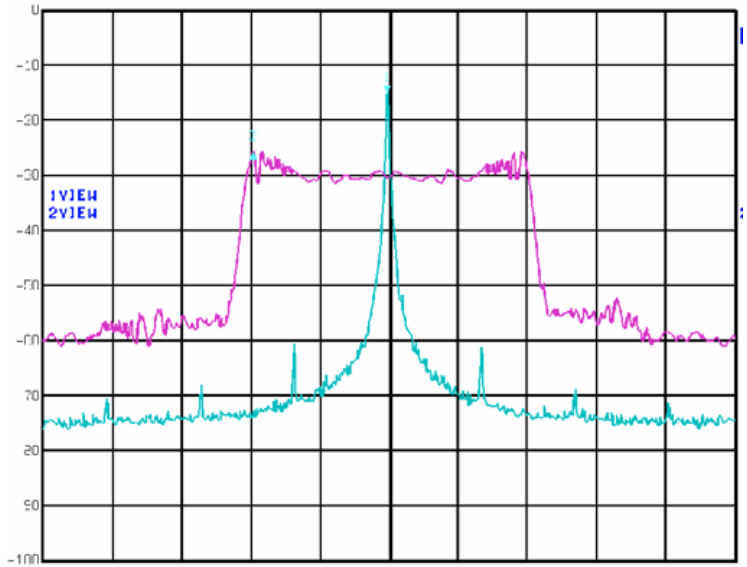
Down spread:

Highest frequency is the one that is programmed into the device



Center spread:

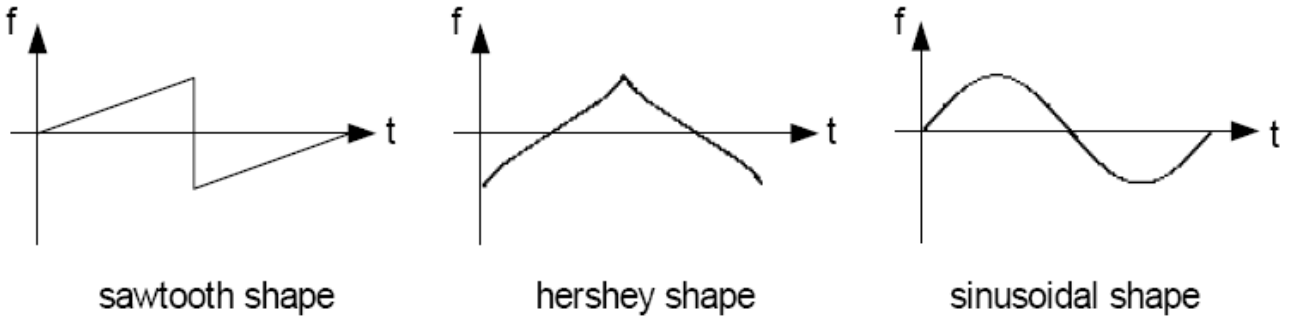
Frequencies are distributed around the desired clock frequency



Important SSC Parameters

- **Spread frequency**
  - **Is the frequency the signal gets changed with**
  - **If too low, its modulation products can interfere with audio frequencies**
  - **If too high, the follow on system might be influenced (e.g. added jitter, loss of functionality)**

- **Spread function**
  - **To allow for an even frequency distribution of the spreaded signal, one has to use a special function to sweep through the spread frequency range (see figure below)**
  - **The best sweep function is called “Hershey Kiss” profile**
  - **Since this profile is hard to create, many designs use a triangular profile**
  - **Triangular shape does not create a completely even frequency spectrum, the frequencies at the “end” of the spread are more dominant**



sawtooth shape hershey shape sinusoidal shape

SSC and EMI Standards

- **The EMI guidelines defining the Spectrum Analyzer settings**
  - **Amongst others: Filter bandwidth, video bandwidth and detector type**
- **Since these settings can be close to the commonly used SSC modulation frequencies, a small change in the way the SSC is done can show a different result in the Spectrum Analyzer**
- **So even two devices with the same amount of spread can appear different in EMI measurements**

SSC Advantages

- SSC is an easy and cheap way to reduce EMI
- If a clocking device is used that can switch SSC on and off, it can even be applied after the system design is done and therefore can save time and money
- It does not require RF knowledge
- Cheap compared with shielding and special layout needs

Can I use SSC in my application?

- What kind of jitter is critical in my application?

- Cycle-to-cycle 
- Peak-to-peak 
- Period jitter
- RMS
- Phase jitter

Examples

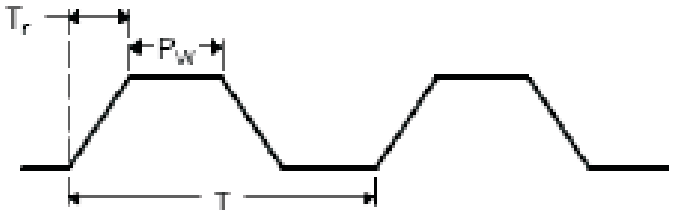
- My microprocessor specifies cycle-to-cycle jitter max of 200ps. Can I use the SSC generator (CDCS502)?

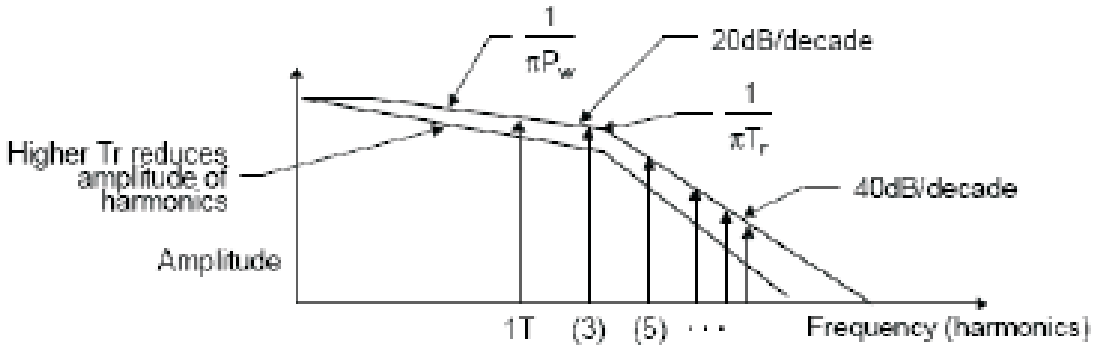
- My microprocessor specifies 50ps peak-peak jitter. Is SSC an option?

- PCI Express accepts -0.5% down spread modulation.

When SSC is not an option

- **Slew Rate Control (SRC)**
  - **It smoothes the edges of the clock. This produces less harmonics.**
  - **Jitter is affected by the slow edges.**





TI Clocking Solutions with SSC

- **CDCS50x Family: EMI Expert**
  - Clock Buffer / Driver (501)
  - Clock Generation / XO Replacement (502)
  - Clock Buffer / Driver with Multiplier (503)
- **CDCE(L)9xx Family: Programmable SSC**
  - Clock Generation with up to 4 PLLs, 9 outputs
- **CDCE906/CDCE706: Programmable SSC**
  - Clock Generation with 3 PLLs, 6 outputs
- **CDC3S04: Sine Wave Buffer**
  - 4-Output Buffer with Integrated LDO

CDCS501/503

Clock Driver with Optional Spread Spectrum Clocking (SSC)

Features

- Wide Input / Output frequency range
  - 40 - 108 MHz for 501
  - 8 - 32 MHz Input / 8 - 108MHz Output for 503
- Selectable Spread-Spectrum Modulation of ±0.0%, ±0.5%, ±1.0%, and ±2.0%
- Selectable frequency multiplication rates of 1x and 4x (CDCS503 only)
- 8 pin TSSOP package
- Operation condition: Single 3.3V power supply, wide temperature range (-40 to 85)

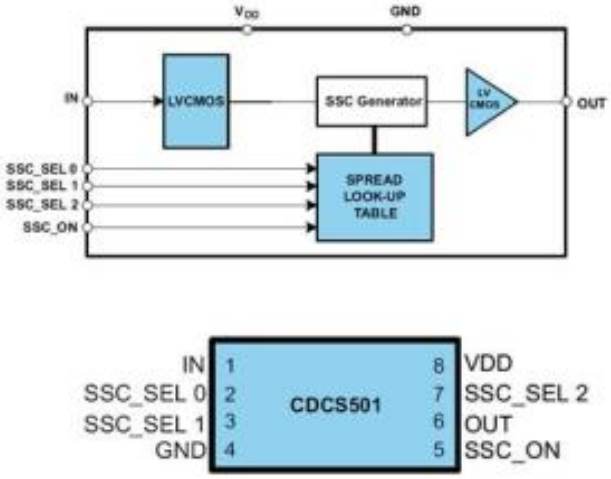
Benefits

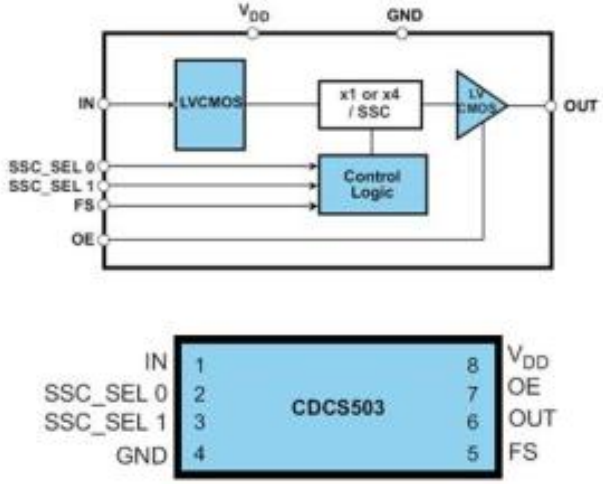
- Saves BOM: single device covers multiple designs
- Reduce EMI thru selectable amount of SSC modulation up to 10dB
- Saves component for higher frequency XO
- Small board space
- Simple power supply scheme; applicable to wider applications with better reliability

Applications

General purpose clock driver with EMI reduction capability:

- Audio/Video entertainment
- Flat Panel TV; Set-top Boxes;
- Blu-Ray DVDR
- Printers; PCs
- Communications access point / gateway / networking card
- Industrial





CDCS502

XTAL-In Clock Generator with Optional SSC

Features

- Crystal input from 8MHz to 32MHz
- Selectable multiplier rates of 1x and 4x so that generate output frequency from 8MHz to 110MHz
- Selectable Spread-Spectrum Modulation of ±0.5%, ±1.0%, and ±2.0%
- 8 pin TSSOP package
- Single 3.3V power supply, wide temperature range -40 , 85

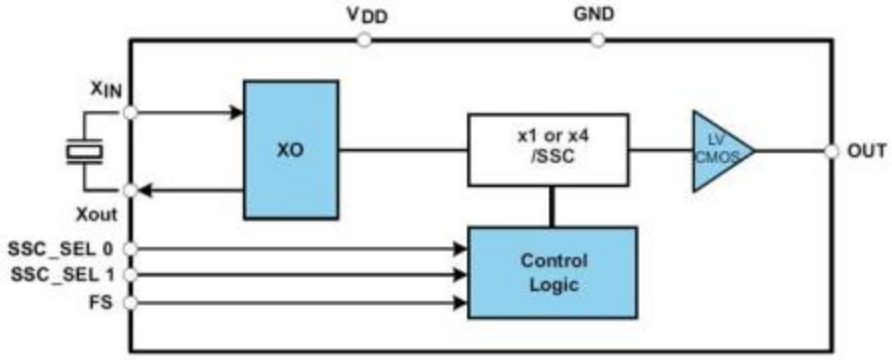
Benefits

- Replacing more costly crystal oscillators
- Wider output frequency range enables one device across multiple designs
- Reduce EMI thru selectable amount of SSC modulation up to 10dB
- Low board space consumption
- Simple power supply scheme; Applicable to wider applications with improved reliability

Applications

XO replacement with EMI reduction need:

- Digital Audio/Video Entertainment
  - Flat Panel TV; Set-top Boxes; Blu-Ray DVDR
- PCs, Printers
- Communications access point / Gateway / Networking card
- Industrial



CDCE(L)949

1.8 V Programmable VCXO 4-PLL Clock Synthesizer with 3.3V/2.5V/1.8V I/Os

Features

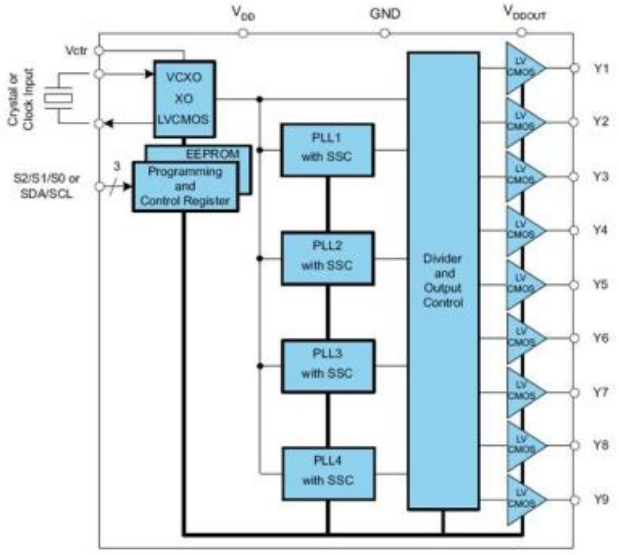
- Input Clock: LVCMOS (160 MHz) and Crystal (8-32MHz)
- VCXO input with ±150ppm (typ) pulling range
- Output frequencies up to 230 MHz @ 1.8V, 2.5V and 3.3V
- 9 low-jitter, low-skew high-performance outputs
- Three user-definable control inputs
- Spread-Spectrum Clocking
- On-chip EEPROM, 24 Pin TSSOP
- 1.8V supply voltage, 3.3V or 2.5V I/O for CDCE949 and 1.8V I/O for CDCEL949

Benefits

- 15% wider I/O frequency range over competition provides customers with higher clocking flexibility
- Fractional PLL enables Zero PPM clocking generation
- Reduces overall system cost by replacing up to 8 different frequency crystal oscillators [on CDCE(L)949]
- SSC clocking allows for ability to reduce EMI noise
- Easy to customize by EEPROM-Lock

Applications

- Digital Media Systems (Audio/Video)
- DSP, DaVinci and OMAP Attached
- IP-STB/TV/Phone
- Streaming Media (i.e. DVD-P/R)
- Automotive Entertainment
- Portable Media
- Print Media



CDCE949PERF-EVM / CDCEL949PERF-EVM

CDCEL9xxPROG-EVM

Texas Instruments

SSC Settings for CDCE(L)9xx

- This is done by choosing the PLL range in every PLL register
- 4 Ranges are implemented:
  - < 125MHz
  - 125MHz <= x < 150MHz
  - 150MHz <= x < 175MHz
  - > 175MHz
- If programmed by hand or with an external controller, this has to be done by the programmer.
- If the TI ClockPro™ Software is used, the software will automatically set the register values.

CDCE706

2:6 Output 3-PLL Clock Synthesizer / Multiplier / Divider

Features

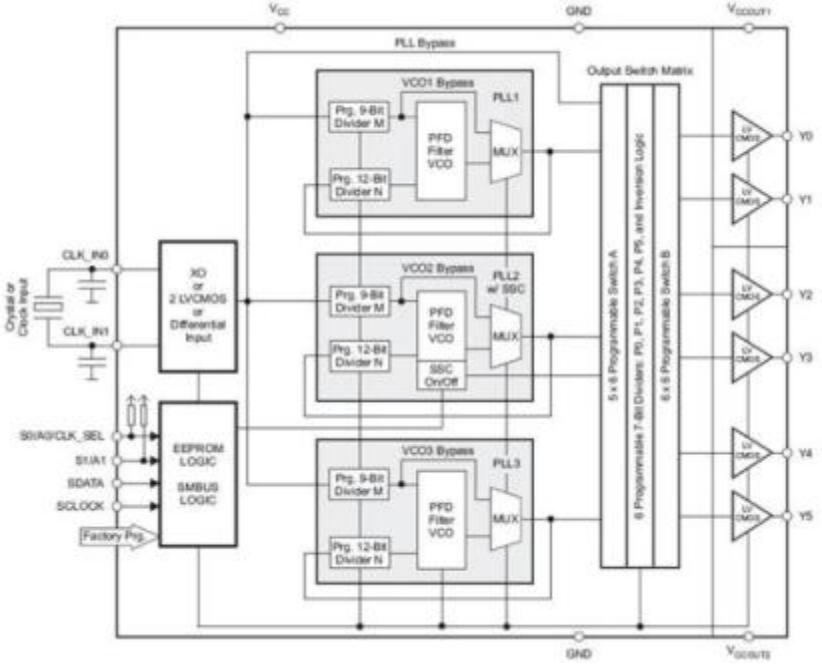
- Input frequencies up to 200MHz SE and differential, 54MHz crystal
- Output frequencies up to 300MHz
- Output provides up to 6 LVTTL
- Low Period Jitter (~ 60ps, pk-pk)
- Provides spread spectrum clocking (SSC)
- On-chip EEPROM
- 180 degree inverting option

Benefits

- Wide divider ratio supports fractional multiplication with 0 ppm error
- Universal input supports two single ended clocks, or differential or crystal input
- 3.3V and 2.5V LVCMOS output signaling levels
- EEPROM saves default start-up settings
- SMBus interface provides in-system programming
- TSSOP-20 package, Temp -40 to 85 C

Applications

- Data Communications
- Medical
- Test Equipment
- Consumer



CDCE906-706PERFEVM

CDCE906-706PROGEVM

Texas Instruments

CDCE906

2:6 Output 3-PLL Clock Synthesizer / Multiplier / Divider

Features

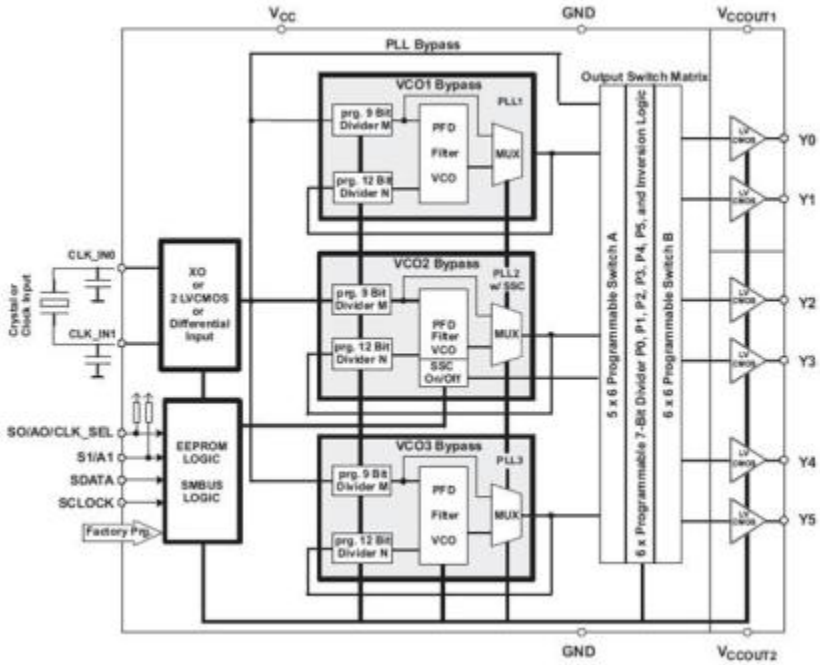
- Input frequencies up to 167 MHz for SE & differential and 54 MHz for crystal
- Output frequencies up to 167 MHz
- Output provides up to 6 LVCMOS/LVTTL
- Low Period Jitter (~ 60ps, pk-pk)
- Provides spread spectrum clocking
- On-chip EEPROM
- 180 degree inverting option

Benefits

- Wide divider ratio supports fractional multiplication with 0 ppm error
- Universal input supports two single ended clocks, or differential or crystal input
- 3.3 V and 2.5 V output signals from single chip
- SMBus interface provides in-system programming
- TSSOP-20 package
- Commercial Temperature range 0 to 70 C

Applications

- Consumer
- DSP clocking
- General purpose frequency synthesizing
- Audio and Video clocking



CDCE906-706PERFEVM

CDCE906-706PROGEVM

Texas Instruments

CDC3S04 - Overview

- What?
  - **1:4 Sine-Wave Buffer**
- For?
  - **Portable EE like Smart-Phones, Navy systems, WL Modems**
- Why?
  - **Eliminate EMI, manage power, replace multiple TCXOs, save board space.**

CDC3S04

1:4 Sine Wave Buffer with Integrated LDO

Features

- 1:4 Low Jitter Clock Sine-to-Sine Clock Buffer
- Ultra-Low Phase Noise and Stand-by current
- On-chip LDO for Low-Noise TCXO
- Individual Clock Request Input for each output
- Serial I2C Interface
- 20-pin WCSP (1.6mm x 2.0mm)

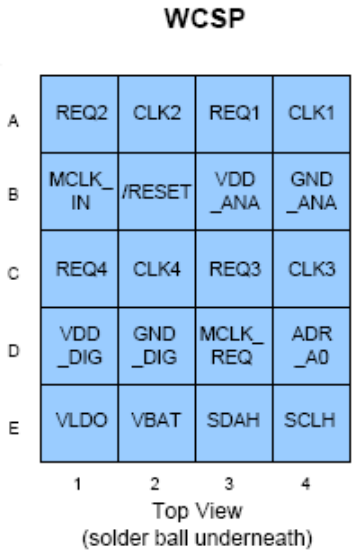
Benefits

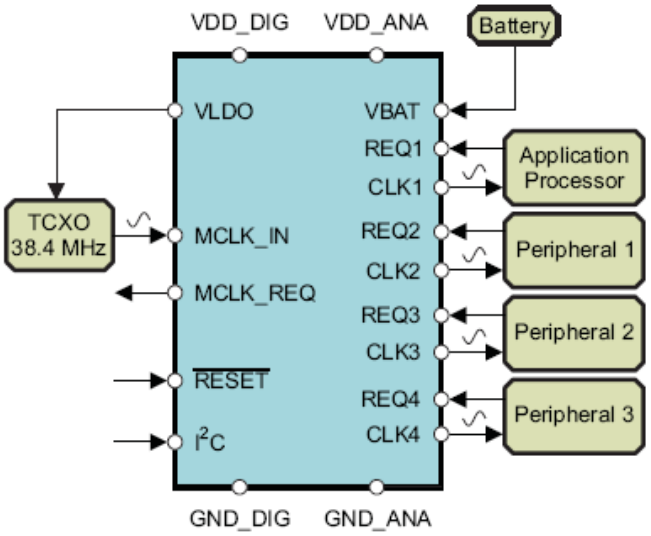
- Replaces multiple TCXOs, saving component costs and guaranteeing phase noise performance
- Preserves power while still maintaining precision
- Converts input battery voltage to output voltage to drive TCXO; acts as TCXO on/off switch to save power
- Ability to toggle clock outputs on/off, saving power
- Control outputs, polarity and internal coding
- Space-saving package for mobile applications

Applications

- UMTS/WCDMA/GSM Cell Phones
- Smart Phones
- Portable Systems
- Navigation Units / GPS
- Wireless Modems

Part Number	Package
CDC3S04	WCSP-20 (YFF)





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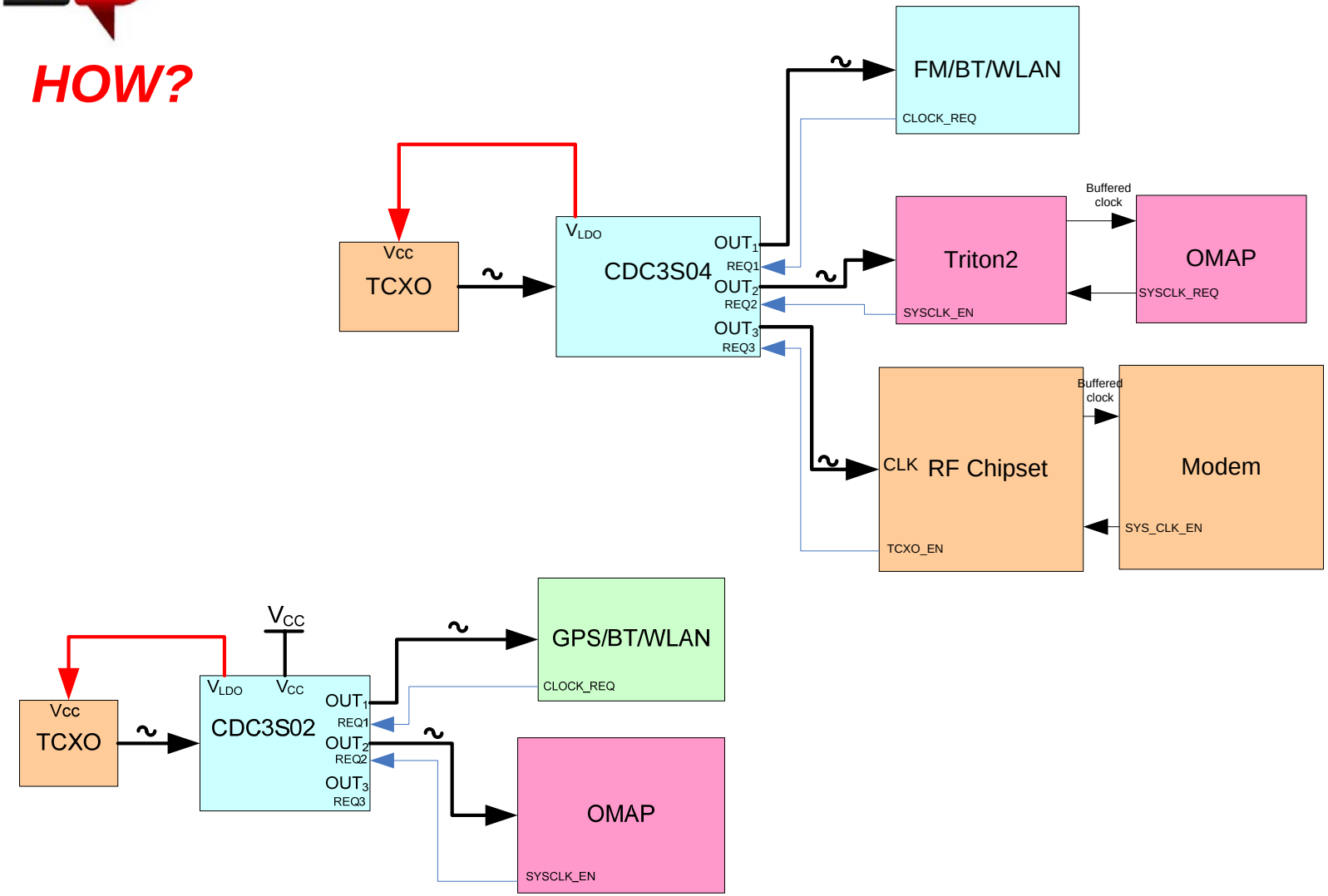
CDC3S04 – Example

HOW?



EMI Summary

- **EMI is a problem in most modern electronic systems**
- **EMI can be countered in several ways**
  - **PCB (Signal Integrity / Layout)**
  - **Active components (SSC / SRC)**
- **Using SSC is a easy, fast and cheap method to reduce EMI**
- **SSC can be implemented into ICs in different ways**
- **Different vendors can use different ways to measure their devices, THEREFORE:**
  - **If in doubt, ask!**
    - **Forum: http://www.ti.com/e2e-clocks**

Device Reference

Part No.	Package Type	Product Description
CDCS501	TSSOP-8	Clock Driver w/ Optional SSC
CDCS502	TSSOP-8	XTAL-In Clock Gen w/ Opt. SSC
CDCS503	TSSOP-8	Clock Driver w/ x4 Mult. + SSC
CDCE706	TSSOP-20	Prog. 3-PLL Synth. (<300MHz)
CDCE906	TSSOP-20	Prog. 3-PLL Synth. (<167MHz)
CDCE(L)913	TSSOP-14	Prog. 1-PLL Synth., 3 Outputs
CDCE(L)925	TSSOP-16	Prog. 2-PLL Synth., 5 Outputs
CDCE(L)937	TSSOP-20	Prog. 3-PLL Synth., 7 Outputs
CDCE(L)949	TSSOP-24	Prog. 4-PLL Synth., 9 Outputs
CDC3S04	DSBGA-20	1:4 Sine Wave Buffer w/ LDO