Protect Your Digital Input Serializer against Lethal Electrical Transients

Digital input serializers (DIS), the heart of digital input modules, must operate in harsh industrial environments. Voltage and current transients caused by electrostatic discharge, switching of inductive loads, or lightning strikes, will corrupt the data flow between field inputs and device output unless effective measures have been taken to diminish transient impact.

This article provides a short overview on the system level operation of a digital input serializer, introduces the three types of transients commonly experienced in industrial applications, and suggests a protection circuitry that ensures data communication between the field inputs and the serial output of a DIS device.

System Operation and Transient Immunity

A digital input serializer is designed for industrial applications using 12V and 24V nominal voltage rails. The device provides eight parallel inputs that connect to a wide variety of sensor switches. Information on the switches' On-Off status is level-shifted and filtered by a signal conditioning stage whose eight parallel outputs are latched into a serializer. Under the control of a system controller the serializer content is clocked out serially. A digital isolator provides an isolated interface for the control and data lines between the serializer on the field-side and the system controller of a PLC- or PC-based system on the control-side.

Ensuring reliable data communication in noisy environment requires that the energy of electrical transients occurring at the field inputs is absorbed before it can unintentionally change the logic input states within the device. Preventive measures in form of transient immunity tests are therefore applied indicating whether a digital input module is able to reliably transmit field input data to the PLC despite transient occurrences.

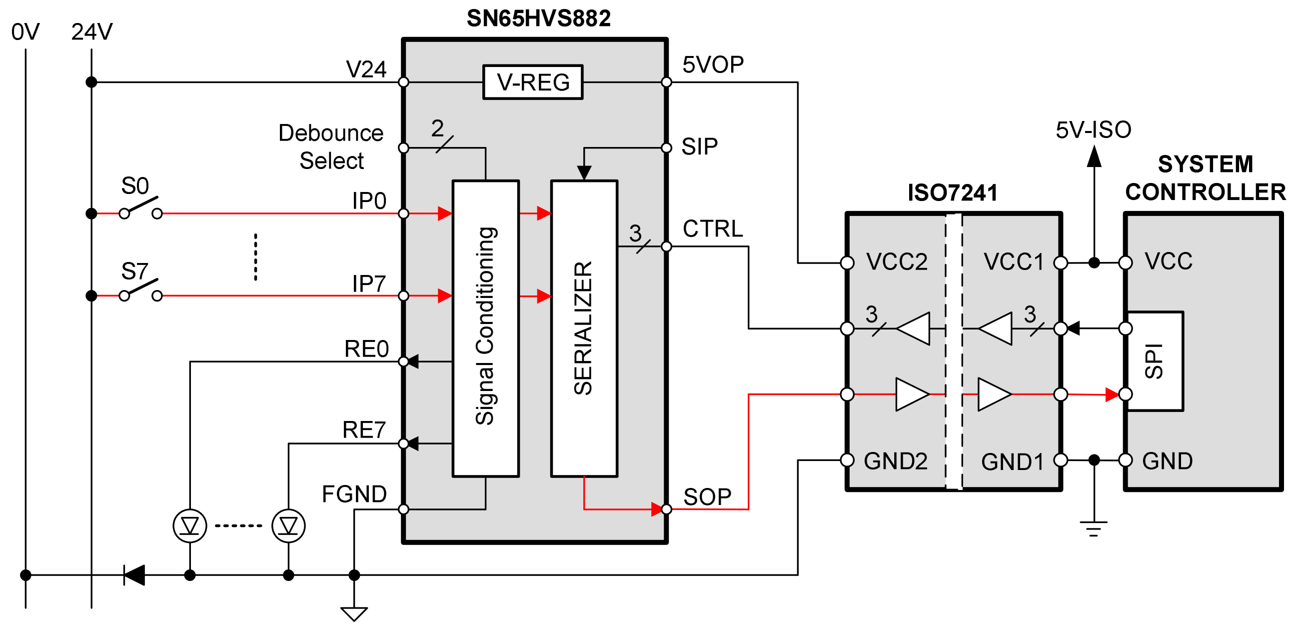

Figure 1. Basic system level diagram

Transient Immunity Tests

The following transient immunity tests are part of the IEC61000-4 family of electromagnetic compatibility tests, specified by the International Electrotechnical Commission (IEC).

The test for **Electrical Fast Transients (EFT) or Burst Immunity, IEC61000-4-4,** often represents the most important test as it simulates every day's switching transients caused by the interruption of inductive loads, relay contact bounce, etc. The test is performed on supply-, data-, and earth ports. A **burst** is defined as the sequence of pulses of limited duration. In this case a burst generator produces a sequence of test pulses with a decay time, (down to 50% of the peak value), of less than 100ns. The typical duration of a burst is 15ms at a repetition rate of 5kHz. The burst period, the time from one burst start to the next, is 300ms. Significant for the test pulse are its short rise time, the high repetition rate, and its low energy content.

While the **Surge Immunity Test, IEC61000-4-5,** is the most severe transient immunity test in points of current and duration, its application is often limited to long data and supply lines (L > 30m). This test simulates switching transients caused by lightning strikes, (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits. A surge generator's output waveforms are specified for open- and short-circuit conditions. The ratio of the open-circuit peak-voltage to the peak short-circuit current is the generator output impedance. Characteristic for this test are the high current, due to low generator impedance, and the long pulse duration, (approximately 1000-times longer than for ESD and Burst tests), indicating a high-energy pulse.

The **Electrostatic Discharge (ESD) Immunity, IEC61000-4-2,** simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. Electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a contact discharge event an ESD generator applies an ESD pulse to the equipment under test. Characteristic for this test are the short rise time and the short pulse duration of less than 100ns, indicating a low-energy, static pulse. ESD – immunity tests have low priority as their potential occurrence is limited to the handling, installation and maintenance work of input modules, during which operators are advised to wear ESD protective clothes as well as to intentionally discharge themselves prior to any direct contact with the module.

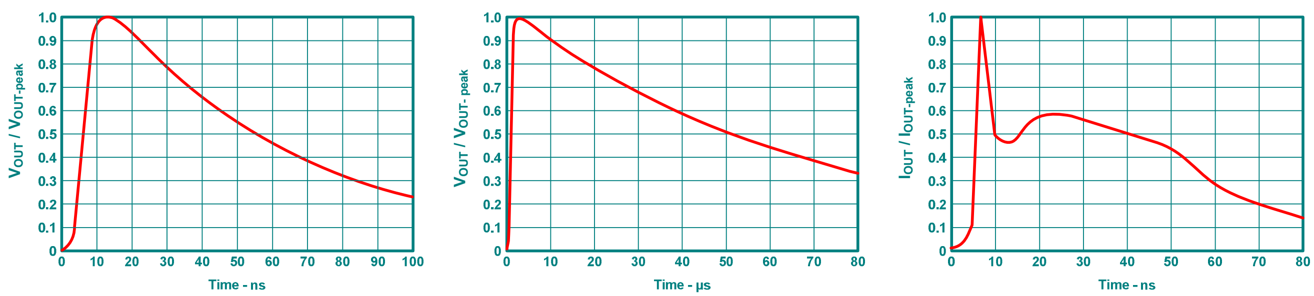

Figure 2. Examples of a Burst- (left), a Surge- (middle), and an ESD pulse (right)
Note, that currents and voltages are normalized. For detailed values and test levels refer to the actual standard.

Transient Protection Circuitry

To protect digital input serializers adequately against electrical transients regional standard bodies have established a list of EMC test requirements which can vary in the level of test voltages applied. Table 1 lists these requirements and their applied test levels for various European countries.

Table 1. EMC Test Requirements

Immunity Test	Standard	Port	Voltage	Level
Peak Pulse Voltage Burst	IEC61000 - 4 - 4	Supply lines	± 4 kV	4
		Data lines	± 2 kV	4
Peak Pulse Voltage Surge	IEC61000 - 4 - 5, (1.2 / 50 µs - 8 / 20 µs), 42 Ω - 0.5 µF	Data lines	± 0.5 kV	1
	IEC61000 - 4 - 5, (1.2 / 50 µs - 8 / 20 µs), 2 Ω - 18 µF	Supply lines	± 1 kV	2
Electrostatic Discharge	IEC61000 - 4 - 2, in air gap	Supply and data lines	± 15 kV	4
	IEC61000 - 4 - 2, in contact	Supply and data lines	± 8 kV	4

Although a digital input serializer possesses internal ESD structures to prevent destruction during device handling, external protection circuitry is needed to absorb the much energy content of Burst- and Surge-transients. Figure 3 gives an example of a protection network for the supply-, data- and ground lines.

C_{HV}	4.7nF, 2kV Polypropylene Capacitor
D_{TVS}	39V, 1500W Transient Voltage Suppressor
C_{D1}	220nF, 100V Decoupling Ceramic Capacitor
R_S	56Ω, 1/3W MELF Resistor
D_S	33V - 36V, Fast Zener Diode
C_B	4.7µF, 60V Ceramic Capacitor
C_{D2}	Muliple 220nF, 100V Ceramic Capacitors
R_{IN}	1.2kΩ, 1/4W MELF Resistor
C_{IN}	220nF, 100V Ceramic Capacitor
D_{RP}	Super Rectifier BYM10-1000
C_{D3}	220nF, 100V Ceramic Capacitor

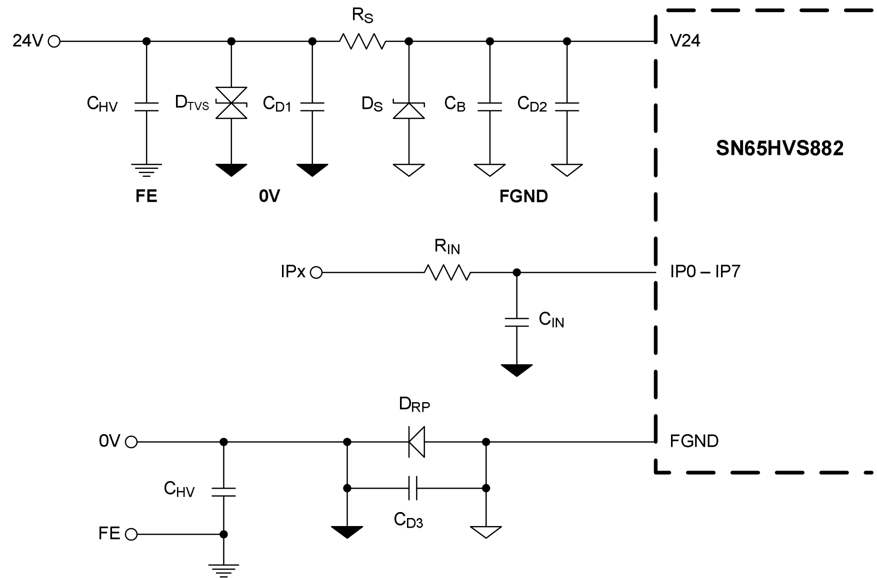

Figure 3. Typical EMC protection circuitry for supply and signal lines

In addition to their high voltage levels, fast electrical transients also consume a wide range of frequencies in the order of 3 MHz to 3 GHz. It is therefore necessary to apply high-frequency decoupling techniques that provide return current paths of low inductance.

Also during transient immunity tests a distinction is made between symmetrical tests, where the test voltage is applied with reference to 0V, and asymmetrical tests, where it is referenced to Functional Earth, FE.
In both cases transient currents must return to their respective reference level without causing voltage potentials on the printed circuit board that might lead to unintentional changes of the logical input states. Thus, for the supply lines, 24V and 0V, two 2 kV high-voltage capacitors, C_{HV}, are used to provide low inductance paths during asymmetrical tests.

Of the five tests listed in Table 1 the surge test performed on the supply lines represents the most energetic one. Here the output impedance of the surge pulse generator is only 2 Ω, representing the ratio of peak surge voltage to peak surge current. Also the duration of a surge pulse exceeds those used in ESD- and Burst tests by a factor of 1000. Hence the protection circuitry required to absorb this large amount of destructive energy becomes substantial.

A transient voltage suppressor, TVS, suppresses the test voltage transient down below 60 V. This type of suppressor is capable of dissipating power transients of up to 1500 W. The 56 Ω MELF resistor, R_S, provides high pulse load capability and further limits the remaining current for the following Zener diode and the digital input serializer. The Zener diode, D_S, reduces the 60 V from the TVS down to approximately 36 V, which is above the maximum specified supply voltage of 35 V and below the threshold of the device internal ESD cells. This Zener diode must have a fast response time to current pulses and should provide up to 2 W of power dissipation.

The protection circuitry of the digital field inputs, IPx, is significantly reduced. Here a 1.2 kΩ MELF resistor, R_{IN}, causes a large voltage drop while drastically reducing the pulse current which then is mainly absorbed by the 220 nF input capacitor, C_{IN}, by directing the current flow to 0 V potential.

Finally a polarity-reversal protection diode, D_{RP}, such as BYM10-1000, is switched into the ground line to protect the digital input serializer against unintentional reversed polarity.

Figure 3 also shows that every diode function in the circuit is paralleled by a decoupling capacitance to provide low inductance return paths for the transient currents. While for the reasons of low inductance and low ESR it is better to establish a decoupling capacitance through the use of multiple, paralleled capacitors of smaller values, the number of external components on a digital input serializer card is limited by its small form factor, thus counteracting the aforementioned approach. This fact has been taken into account during the design of the SN65HVS882 digital input serializer. This device therefore provides internal protection structures that are significantly stronger compared to those of standard industrial ICs.

Conclusion

Digital input serializers must reliably operate in electrical transient contaminated environments. External protection circuitry accompanied by strong, device internal protection structures enable to pass harsh transient immunity tests. Supporting the trend of new digital input designs, Texas Instruments is introducing its SN65HVS88x family of digital input serializers for commercial and industrial applications.

References

Further information is available at www.TI.com/interface by entering the literature numbers provided below in parenthesis into the Keyword Search field.

- SN65HVS882 data sheet (SLAS601)
- SN65HVS882 EVM Manual (SLAU249)
- SN65HVS880 data sheet (SLAS592A)
- SN65HVS880 EVM Manual (SLAU245)
- PowerPAD Thermally Enhanced Package (SLMA002B)
- IEC61000-4-2: Test and Measurement Techniques – Electrostatic Discharge Immunity Test
- IEC61000-4-4: Test and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test
- IEC61000-4-5: Test and Measurement Techniques – Surge Discharge Immunity Test