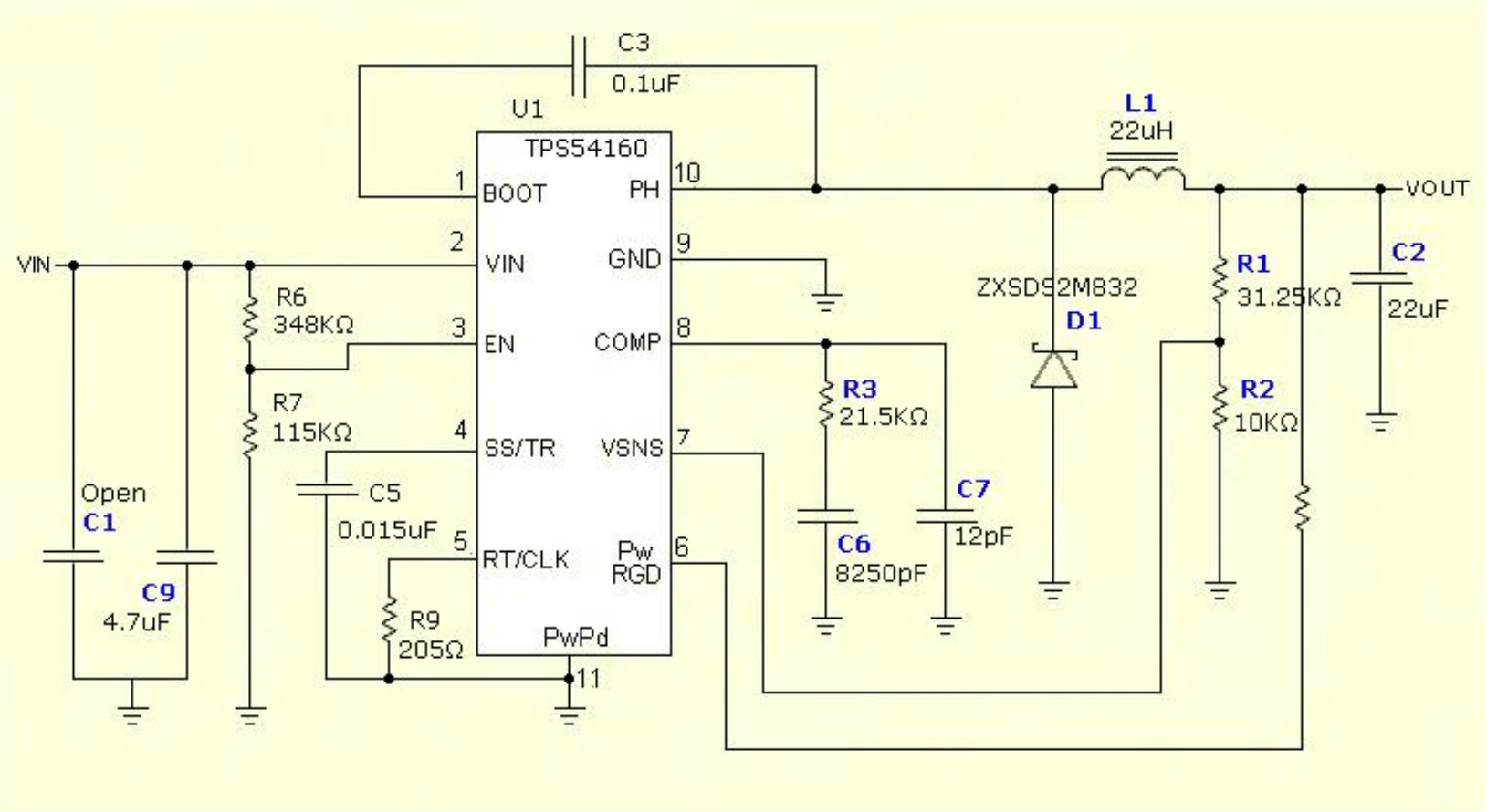
Design Summary

Design Name: **TPS54060_36V_3.3V0.5A**

Design ID:	**25088**	Created By User:	**Kazuaki Ohshita**
Creation Date:	**29 Nov 2008**	Design Type:	**PowerSupply**
Local Time:	**03:56 PM**		

Schematic



Note : Parts with bold blue labels can be completely modified, parts with plain black labels allow only name changes.

Quickly link to data sheets or product home pages by clicking on TI devices.

Analysis

Analysis - Main

Parameter	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum	Units
Input Voltage	4.50	-	36.00	-	-	-	-	-	-	Volts
Input Ripple	-	-	-	-	-	720	-	-	63	mVp-p
UVLO (Start)	-	-	-	-	-	-	-	4.72	-	Volts
UVLO(Stop)	-	-	-	-	-	-	-	3.71	-	Volts
Switching Frequency	-	-	-	-	570	-	-	-	-	KHz
Slow Start	-	-	-	-	6	-	-	-	-	ms
Estimated PCB Area	-	-	-	-	-	-	-	203	-	mm^2
Max Component Height	-	-	-	-	-	25	-	-	3	mm

Analysis - Output1

Parameter	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum	Units
Output Voltage	-	3.300	-	-	-	-	3.250	-	3.418	Volts
Output Ripple	-	-	-	-	-	66	-	-	7	mVp-p
Output Current	-	-	0.500	0.100	-	-	-	-	-	Amps
Inductor Peak to Peak Current	-	-	-	-	-	-	0.060	-	0.344	Amps
Current Limit Threshold	-	-	-	-	2.7	-	-	2.7	-	Amps

Gain Margin	-	-	-	-10	-	-	-	-23	-	dB
Phase Margin	-	-	-	60	-	-	-	84	-	Deg.
Upper FET RDSon	-	-	-	-	-	-	206	-	270	mOhms
Duty Cycle	-	-	-	-	-	-	9.6	-	79.0	%
On Time Min(switch)	-	-	-	-	-	-	137.3	-	1789.0	ns
Cross Over Frequency	-	-	-	-	-	-	-	24	-	KHz

Loop Response

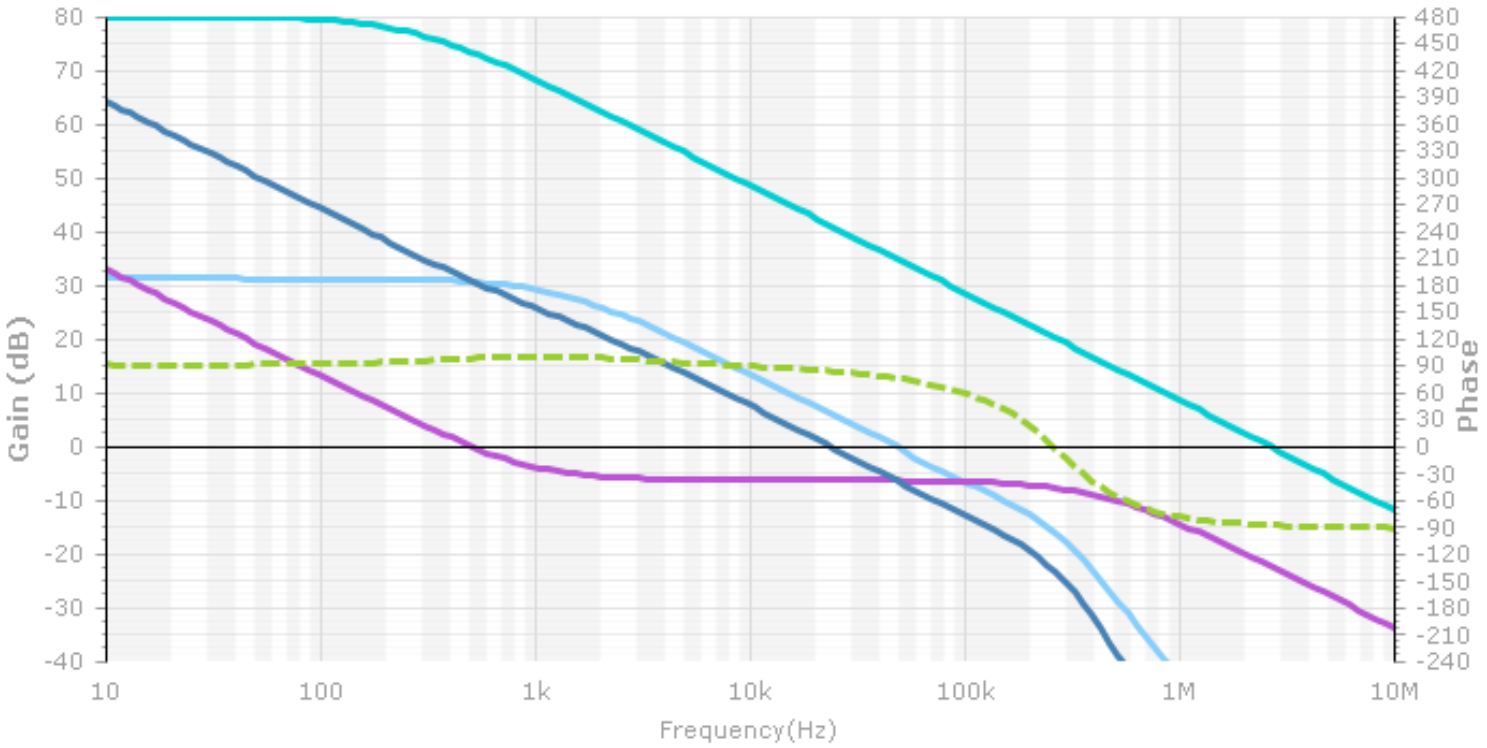
- ☑ Power Stage Gain
- ☐ Power Stage Phase
- ☑ Open Loop Error Amplifier Gain
- ☑ Compensated Error Amplifier Gain
- ☐ Compensated Error Amplifier Phase
- ☑ Total Gain
- ☑ Total Phase

Scale Up

Scale Down

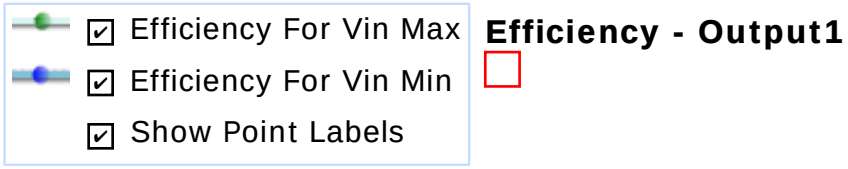
LoopResponse - Output1

Switching Freq	Cross Over Freq	LC Corner Freq	ESR Zero Freq	Gain Margin	Phase Margin
570Khz	**24.2Khz**	**7.2Khz**	**602.9Khz**	**-23 dB**	**84 Deg.**



This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Minimum Load,
Maximum Rdson and Maximum Cap ESR. To customize conditions use the "What If Analysis" form

Efficiency


Efficiency For Vin Max
Efficiency For Vin Min
Show Point Labels
Efficiency - Output1

Stress

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	50V	36.2V	3A	0.25A		319uW	-
C2 (Bulk Output Cap)	6.3V	3.32V	2A	99mA		118uW	-
L1 (Output Inductor)	-	-	0.96A	0.51A		34mW	-
D1 (Catch Diode)	80V	36.2V	1.65A	0.48A		58mW	35•C
U1 (Converter)	65V	36.2V	4A	0.44A		310mW	41•C

Each loss in this view is the worst case calculation for the individual component. The conditions that cause the worst case loss will not all occur at the same time for all components. Therefore adding up the individual worst cases losses to get a total loss of the system is not realistic.

Max Junction Temperature is calculated using Ambient Temperature 25°C along with the resistance (junction to ambient) specified by the manufacturer, with their standards for board layout.

It is recommended that the user review the specifications given by the FET manufacturer for their board layout standards.

Using a low cost PCB with minimal copper will have a great impact on heat dissapation and could lead to much higher junction temperatures.

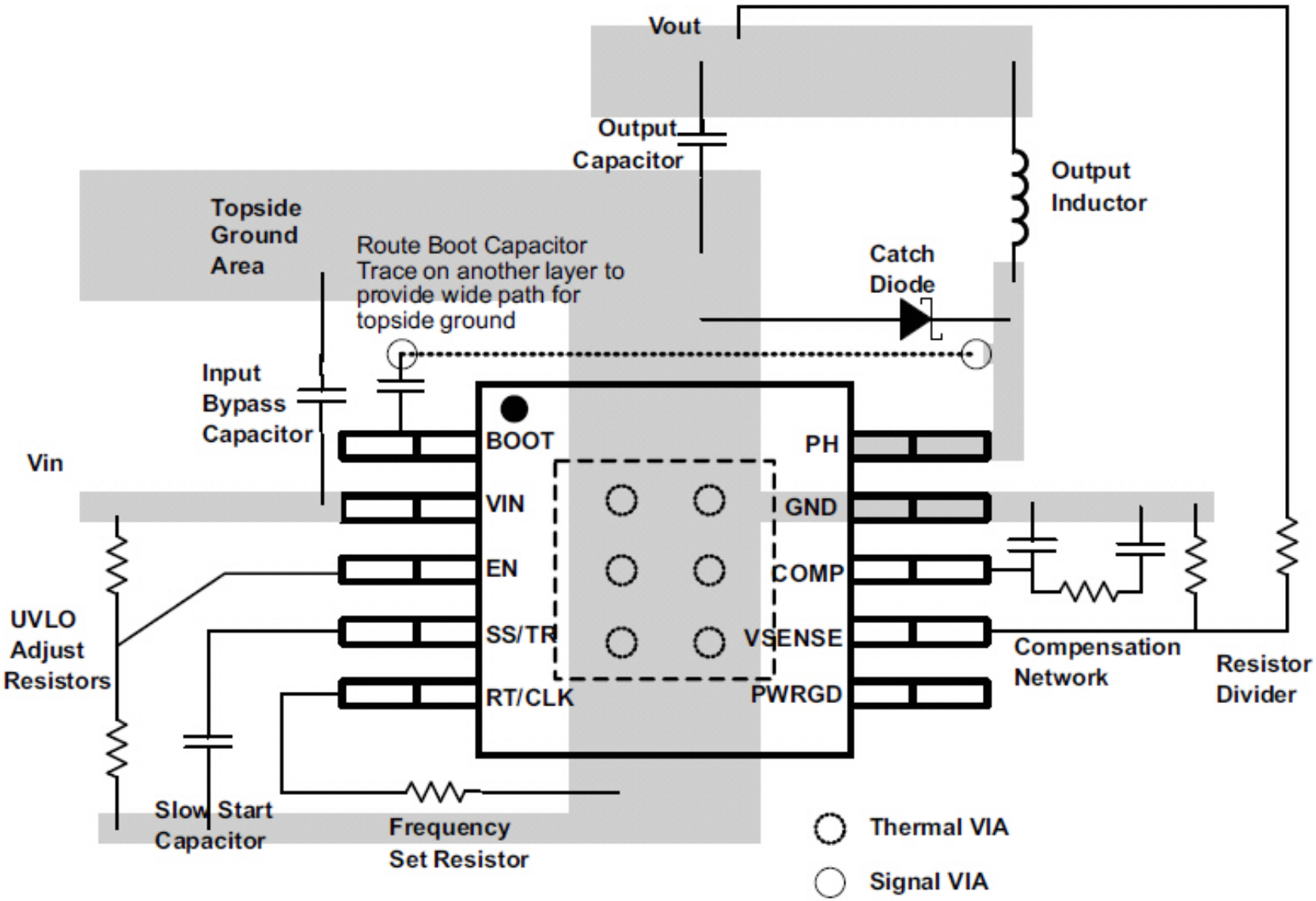
Calculated Voltage does not take into account spike voltages caused by various parasitic inductances and capacitances that are factors of board layout

Bill Of Materials

Name	Quantity	Part Number	Description	Manufacturer	Package	Area (mm²)	Height (mm)
C2	1	C3216X5R0J226M	Capacitor, Ceramic, 22uF, 6.3V, 20%	TDK	C3216 1206	7	1
C3	1	Standard	Capacitor, Ceramic, 0.1uF, 16V, 10%	Standard	0603	2	1
C5	1	Standard	Capacitor, Ceramic, 0.015uF, 6.3V, 0%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 8250pF, 16V, 0%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 12pF, 16V, 0%	Standard	0603	2	1
C9	1	GRM32ER71H475KA88L	Capacitor, Ceramic, 4.7uF, 50V, 10%	muRata	GRM32E 1210	10	2
D1	1	ZXSDS2M832	Diode, Schottky, 80V, 1.65A	Zetex	MLP832	6	1
L1	1	SLF7032T-220M96	Inductor, 22uH, 0.96A, 132mΩ	TDK	SLF7032	49	3
R1	1	Standard	Resistor, SurfaceMount, 31.25KΩ, 62mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 10KΩ, 62mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 21.5KΩ, 62mW, 1%	Standard	0603	2	1
R6	1	Standard	Resistor, SurfaceMount, 348KΩ, 62mW, 1%	Standard	0603	2	1
R7	1	Standard	Resistor, SurfaceMount, 115KΩ, 62mW, 1%	Standard	0603	2	1
R9	1	Standard	Resistor, SurfaceMount, 205Ω, 62mW, 1%	Standard	0603	2	1

U1	1	TPS54160	IC, Converter, 10 pins	Texas Instruments, Inc.	MSOP-Power PAD	16	2

Layout



Layout Guidelines:

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the

bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad.

The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.