Agilent HCPL-260L/ 060L/263L/063L High Speed LVTTL Compatible 3.3 Volt Optocouplers

Data Sheet

Features

- Low power consumption
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 50 V
- High speed: 15 MBd typical
- LVTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40°C to +85°C
- Available in 8-pin DIP, SOIC-8
- Strobable output (single channel products only)
- Safety approvals; UL, CSA, VDE (pending)

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Field buses

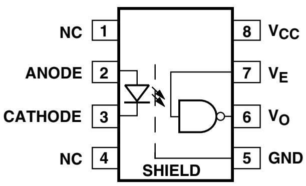
Description

The HCPL-260L/060L/263L/063L are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/ µs.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40°C to +85°C allowing trouble-free system performance.

Functional Diagram

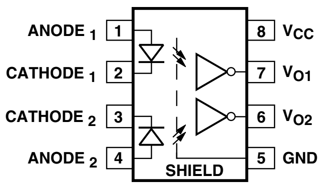
HCPL-260L/060L



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

HCPL-263L/063L



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

These optocouplers are available in an 8-pin DIP and industry standard SO-8 package. The part numbers are as follows:

8-pin DIP	SO-8 Package
HCPL-260L	HCPL-060L
HCPL-263L	HCPL-063L

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

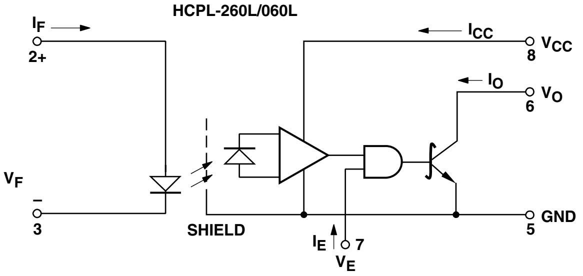
HCPL-260L #XXX

060 = VDE 0884 V_{IORM} = 630 Vpeak Option

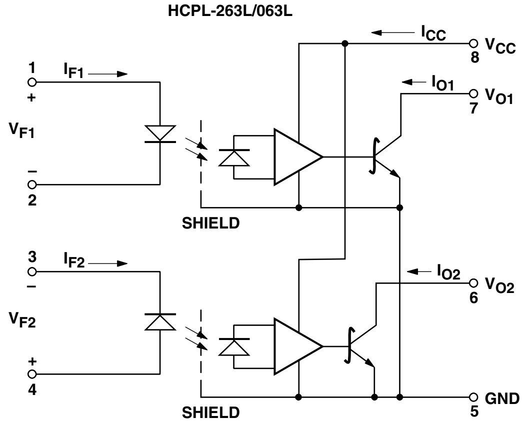
500 = Tape and Reel Packaging Option

Option data sheets available. Contact Agilent sales representative or authorized distributor for information.

Schematic

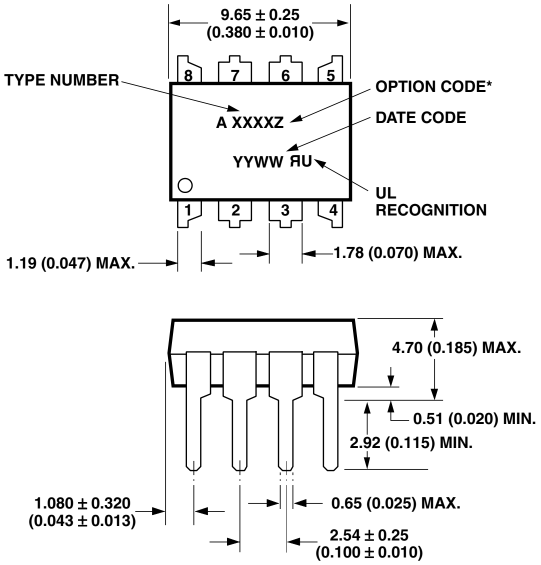


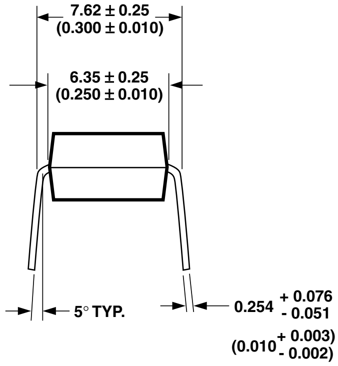
USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 5).



Package Outline Drawings

8-Pin DIP Package

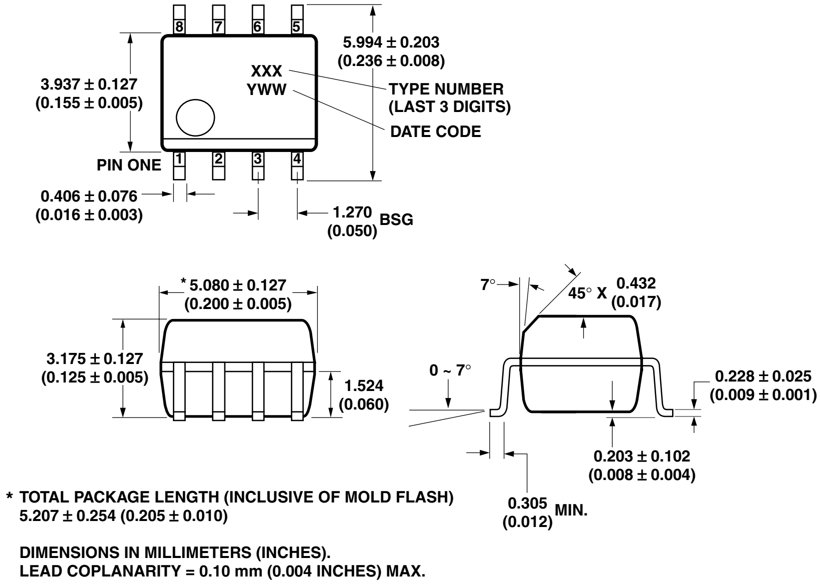




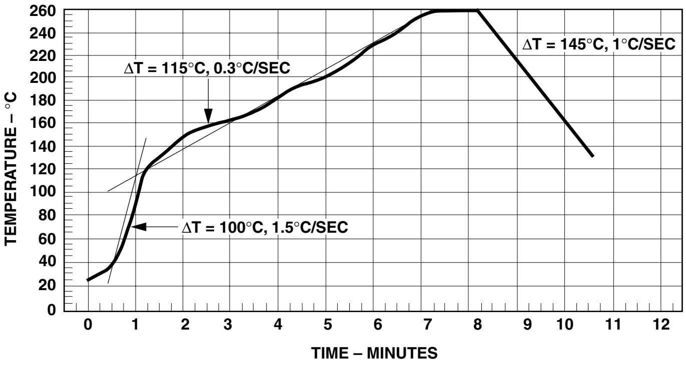
DIMENSIONS IN MILLIMETERS AND (INCHES).

*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

Small Outline SO-8 Package



Solder Reflow Temperature Profile (Surface Mount Option Parts)



NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS HIGHLY RECOMMENDED.

Regulatory Information

The HCPL-260L/060L/263L/063L are pending by the following organizations:

UL

Approval (pending) under UL 1577, Component Recognition Program, File E55361.

CSA

Approval (pending) under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approval (pending) according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L (101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L (102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

VDE 0884 Insulation Related Characteristics

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 450 V rms		 I-IV I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 ˚C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings (No Derating Required up to 85˚C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		–55	125	˚C	
Operating Temperature†	T_A		–40	85	˚C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8		20	mA	2
		Dual 8-Pin DIP Dual SO-8		15		1, 3
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	1
				3		
Input Power Dissipation	P_I			40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8		V_{CC} + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage	V_O			7	V	1
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		1, 4
Lead Solder Temperature (Through Hole Parts Only)	T_{LS}	8-Pin DIP	260˚C for 10 sec., 1.6 mm below seating plane			
			260˚C for 10 sec., up to seating plane			
Solder Reflow Temperature Profile (Surface Mount Parts Only)		SO-8	See Package Outline Drawings section			

**Ratings apply to all devices except otherwise noted in the Package column.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	2.7	3.3	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Operating Temperature	T_A	–40	85	˚C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

Electrical Specifications

Over Recommended Temperature (T_A = –40°C to +85°C) unless otherwise specified. All Typicals at V_{CC} = 3.3 V, T_A = 25°C. All enable test conditions apply to single channel products only. See Note 5.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		4.5	50	µA	V_{CC} = 3.3 V, V_E = 2.0 V, V_O = 3.3 V, I_F = 250 µA	1	1, 15
Input Threshold Current	I_{TH}		3.0	5.0	mA	V_{CC} = 3.3 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2	15
Low Level Output Voltage	V_{OL}*		0.35	0.6	V	V_{CC} = 3.3 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3	15
High Level Supply Current	I_{CCH}		4.7	7.0	mA	V_E = 0.5 V V_{CC} = 3.3 V I_F = 0 mA		
Low Level Supply Current	I_{CCL}		7.0	10.0	mA	V_E = 0.5 V V_{CC} = 3.3 V I_F = 10 mA		
High Level Enable Current	I_{EH}		–0.5	–1.2	mA	V_{CC} = 3.3 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*		–0.5	–1.2	mA	V_{CC} = 3.3 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			15
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25°C I_F = 10 mA	5	1
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		1
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		–1.6 –1.9		mV°C	I_F = 10 mA		1
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		1

*The JEDEC Registration specifies 0°C to +70°C. Agilent specifies –40°C to +85°C.

Switching Specifications

Over Recommended Temperature (T_A = –40°C to +85°C), V_{CC} = 3.3 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 3.3 V.

Parameter	Sym.	Package**	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}				90	ns	T_A = 25°C	R_L = 350 Ω, C_L = 15 pF	6, 7, 8	1, 6, 15
Propagation Delay Time to Low Output Level	t_{PHL}				75	ns				1, 7, 15
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	8-Pin DIP SO-8			25	ns			8	9, 15
Propagation Delay Skew	t_{PSK}				40	ns				8, 9, 15
Output Rise Time (10-90%)	t_r			45		ns				1, 15
Output Fall Time (90-10%)	t_f			20		ns				1, 15
Propagation Delay Time of Enable from V_{EH} tp V_{EL}	t_{ELH}			45		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		9	10
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			30		ns				11

*JEDEC registered data for the 6N137.
**Ratings apply to all devices except otherwise noted in the Package column.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-263L HCPL-063L	15,000	25,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 3.3 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	11	12, 14, 15
		HCPL-260L HCPL-060L	15,000	25,000		$\|V_{CM}\|$ = 50 V			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-263L HCPL-063L	15,000	25,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 3.3 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	11	13, 14, 15
		HCPL-260L HCPL-060L	15,00	25,000		$\|V_{CM}\|$ = 50 V			

Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Sym.	Package	Min.	Typ.	Max	Units	Test Conditions	Fig.	Note
Input-Output Insulation	$I_{I\text{-}O}$*	Single 8-Pin DIP Single SO-8			1	µA	45% RH, t = 5 s, $V_{I\text{-}O}$ = 3 kV DC, T_A = 25°C		16, 17
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP, SO-8	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C	16, 17	
Input-Output Resistance	$R_{I\text{-}O}$	8-Pin, SO-8		10^{12}		Ω	$V_{I\text{-}O}$ =500 V dc		1, 16, 19
Input-Output Capacitance	$C_{I\text{-}O}$	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25°C		1, 16, 19
Input-Input Insulation Leakage Current	$I_{I\text{-}I}$	Dual Channel		0.005		µA	RH ≤ 45%, t = 5 s, $V_{I\text{-}I}$ = 500 V		20
Resistance (Input-Input)	$R_{I\text{-}I}$	Dual Channel		10^{11}		Ω			20
Capacitance (Input-Input)	$C_{I\text{-}I}$	Dual 8-Pin Dip		0.03		pG	f = 1 MHz		20
		Dual SO-8		0.25					

*The JEDEC Registration specifies 0°C to +70°C. Agilent specifies –40°C to +85°C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
5. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 11. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
8. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
9. See test circuit for measurement details.
10. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
11. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
12. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (i.e., V_o > 2.0 V).
13. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_o < 0.8 V).
14. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).
15. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only. See application information provided.
16. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
17. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, $I_{I\text{-}O}$ ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
18. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage detection current limit, $I_{I\text{-}O}$ ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
19. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
20. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

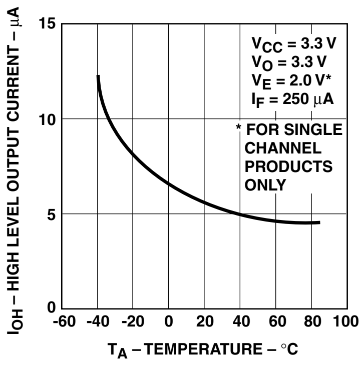


Figure 1. Typical high level output current vs. temperature.

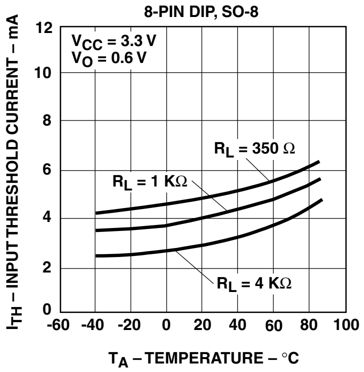


Figure 2. Typical input threshold current vs. temperature.

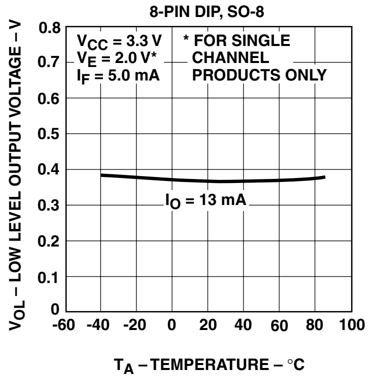


Figure 3. Typical low level output voltage vs. temperature.

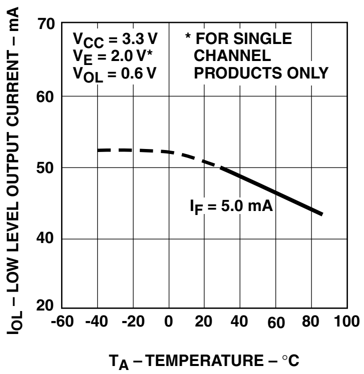


Figure 4. Typical low level output current vs. temperature.

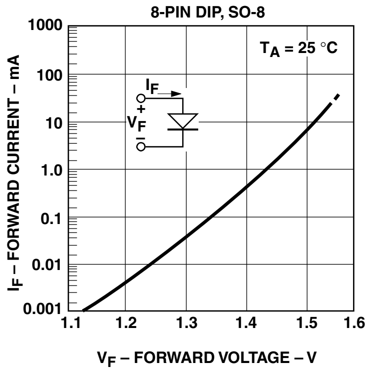


Figure 5. Typical input diode forward characteristic.

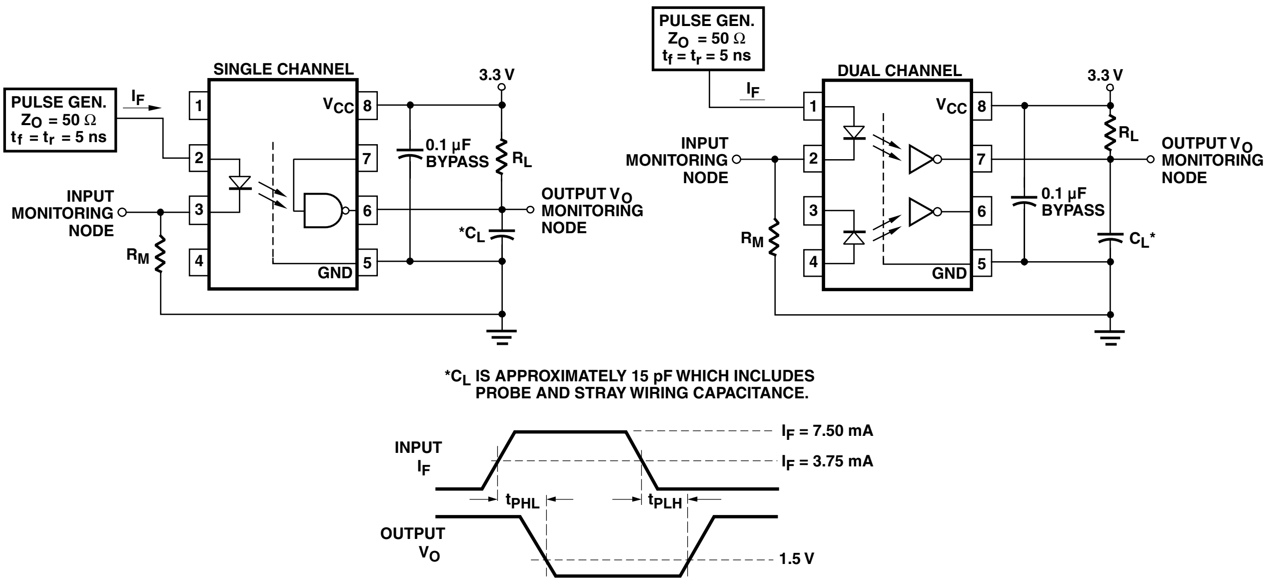


Figure 6. Test circuit for t_{PHL} and t_{PLH}.

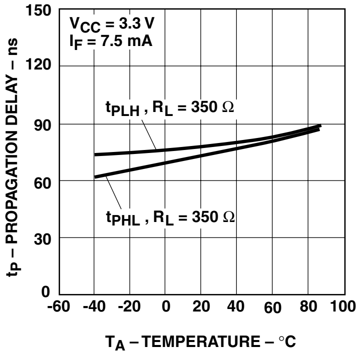


Figure 7. Typical propagation delay vs. temperature.

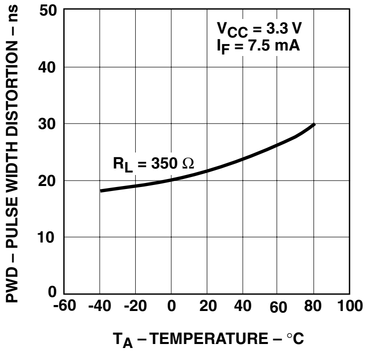


Figure 8. Typical pulse width distortion vs. temperature.

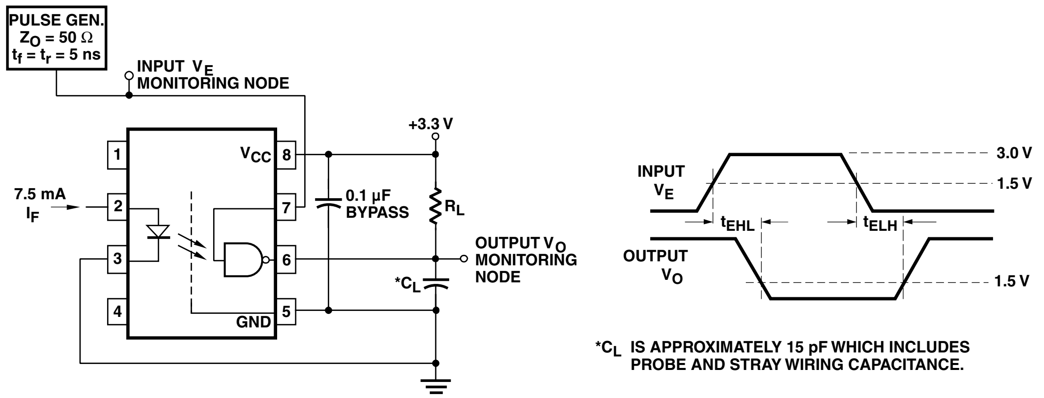


Figure 9. Test circuit for t_{EHL} and t_{ELH}.

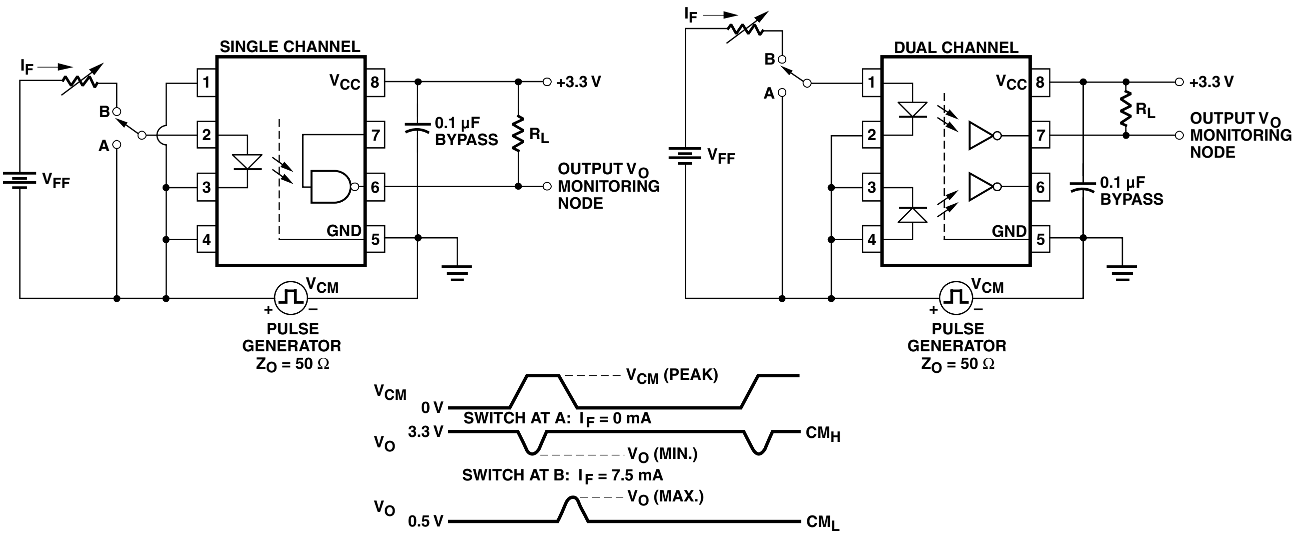


Figure 10. Test circuit for common mode transient immunity and typical waveforms.

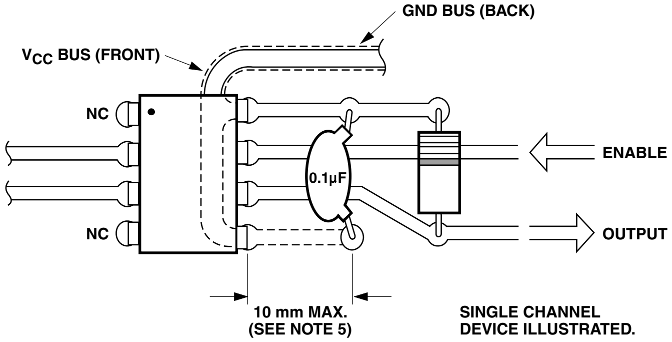
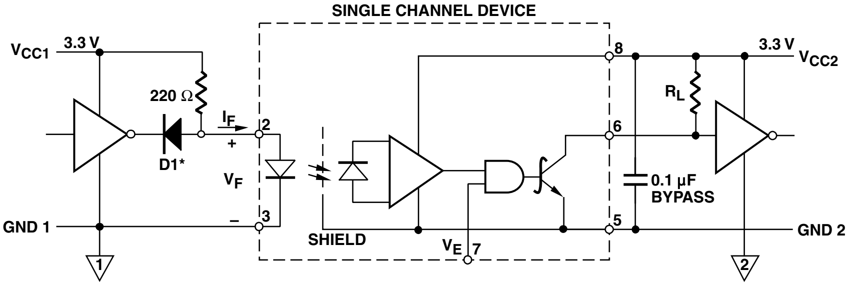


Figure 11. Recommended printed circuit board layout.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

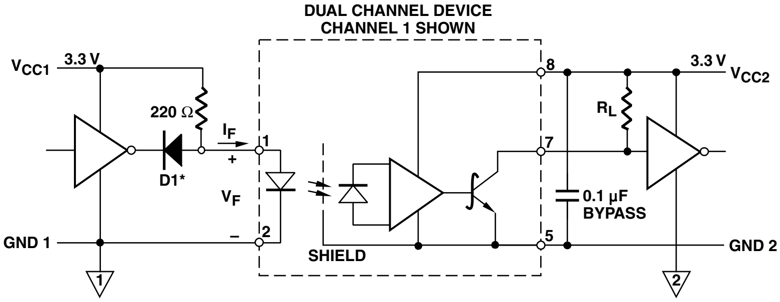


Figure 12. Recommended LVTTL interface circuit.

Application Information

Common-Mode Rejection for HCPL-260L Families:

Figure 13 shows the recommended drive circuit for optimal common-mode rejection performance. Two main points to note are:

1. The enable pin is tied to V_{CC} rather than floating (this applies to single-channel parts only).
2. Two LED-current setting resistors are used instead of one. This is to balance I_{LED} variation during common-mode transients.

If the enable pin is left floating, it is possible for common-mode transients to couple to the enable pin, resulting in common-mode failure. This failure mechanism only occurs when the LED is on and the output is in the Low State. It is identified as occurring when the transient output voltage rises above 0.8 V. Therefore, the enable pin should be connected to either V_{CC} or logic-level high for best common-mode performance with the output low (CMR_L). This failure mechanism is only present in single-channel parts which have the enable function.

Also, common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 14 shows the parasitic capacitances which exists between LED anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 14 on the input side is an AC-equivalent circuit.

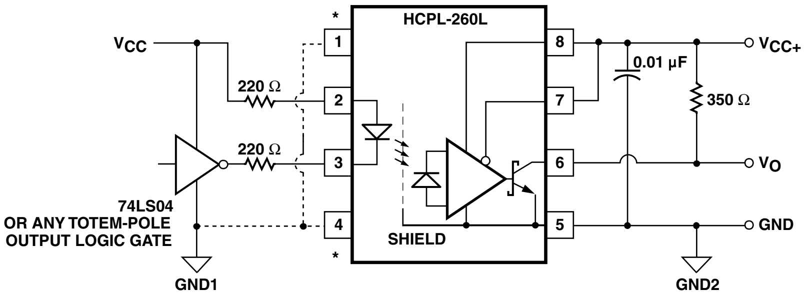


Figure 13. Recommended drive circuit for High-CMR.

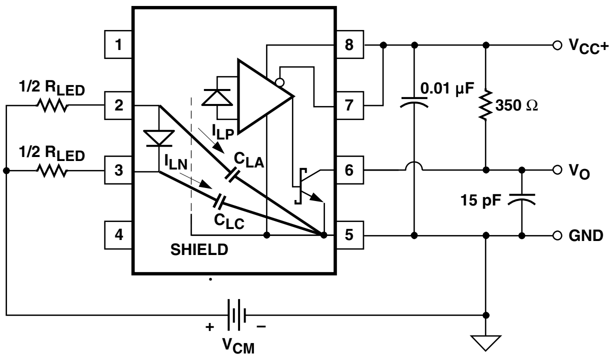


Figure 14. AC equivalent circuit.

For transients occurring when the LED is on, common-mode rejection (CMR_L, since the output is in the “low” state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CMR_L also depends on the extent which I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F will cause common-mode failure for transients which are fast enough.

Likewise for common-mode transients which occur when the LED is off (i.e. CMR_H, since the output is “high”), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient “signal” may cause the output to spike below 2 V (which constitutes a CMR_H failure).

By using the recommended circuit in Figure 13, good CMR can be achieved. The balanced I_{LED}-setting resistors help equalize I_{LP} and I_{LN} to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}

CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 13 may be enhanced by following these guidelines:

1. Use of drive circuits where current is shunted from the LED in the LED "off" state (as shown in Figures 15 and 16). This is beneficial for good CMR_H.
2. Use of I_{FH} > 3.5 mA. This is good for high CMR_L.

Figure 15 shows a circuit which can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices which have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 16 may be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 17 may be used. The diode in parallel with the R_{LED} speeds the turn-off of the optocoupler LED.

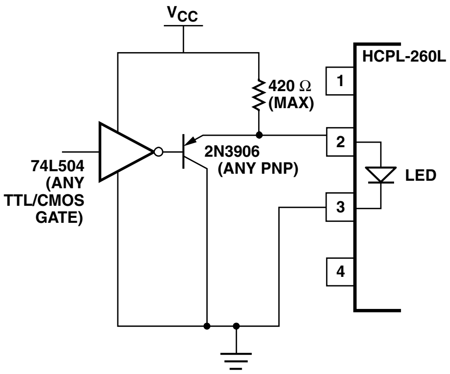


Figure 15. TTL interface circuit.

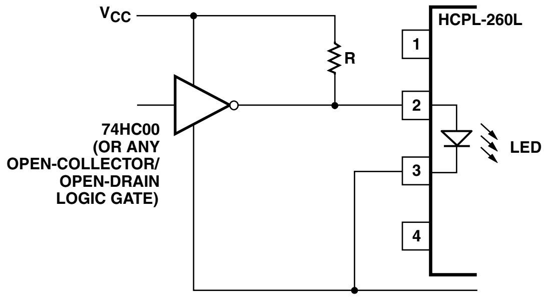


Figure 16. TTL open-collector/open drain gate drive circuit.

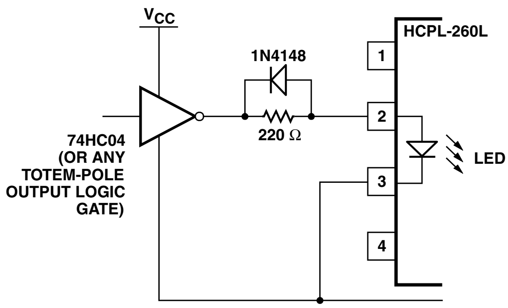


Figure 17. CMOS gate drive circuit.

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