

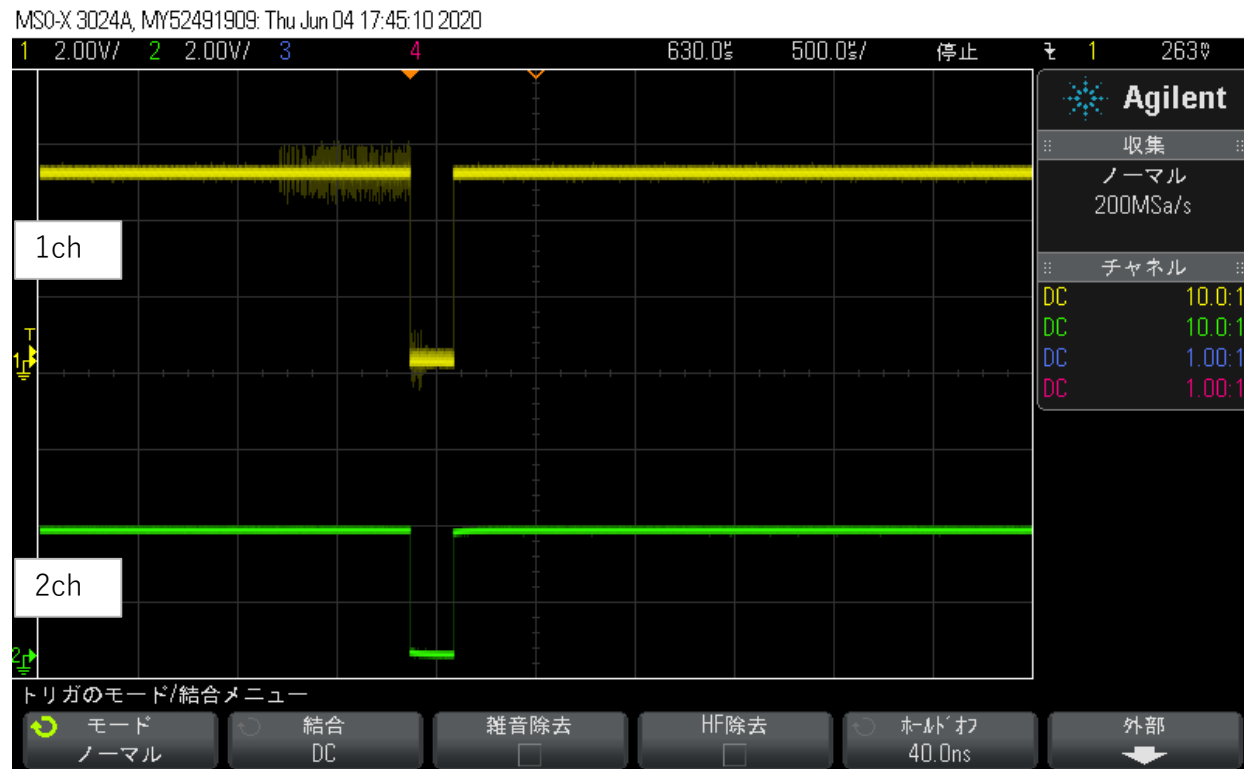
connector → (RI2 pin) SN75LV4737ADB (RQ2 pin) → (IND pin) ISO7242ADW (OUTD) → FPGA

↑  
Chattering signal  
(random pulse)

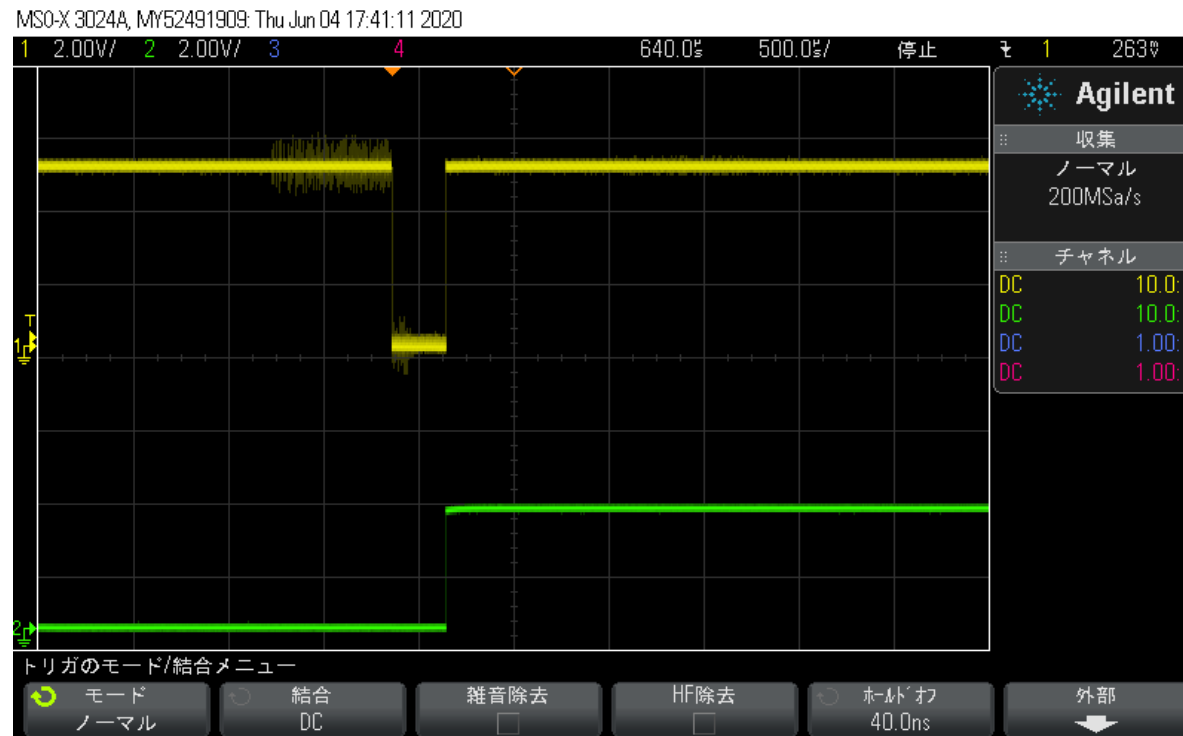
↑  
ch1

↑  
ch2

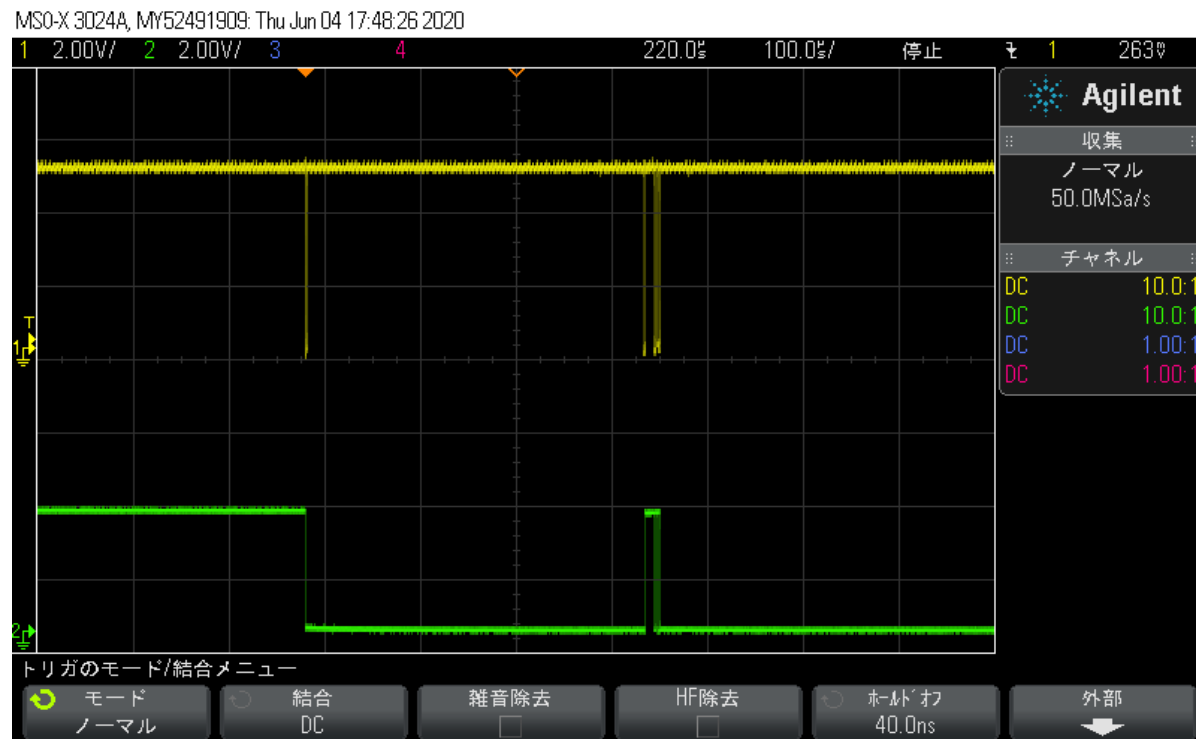
■ Inserting cable(Chattering)  
OK



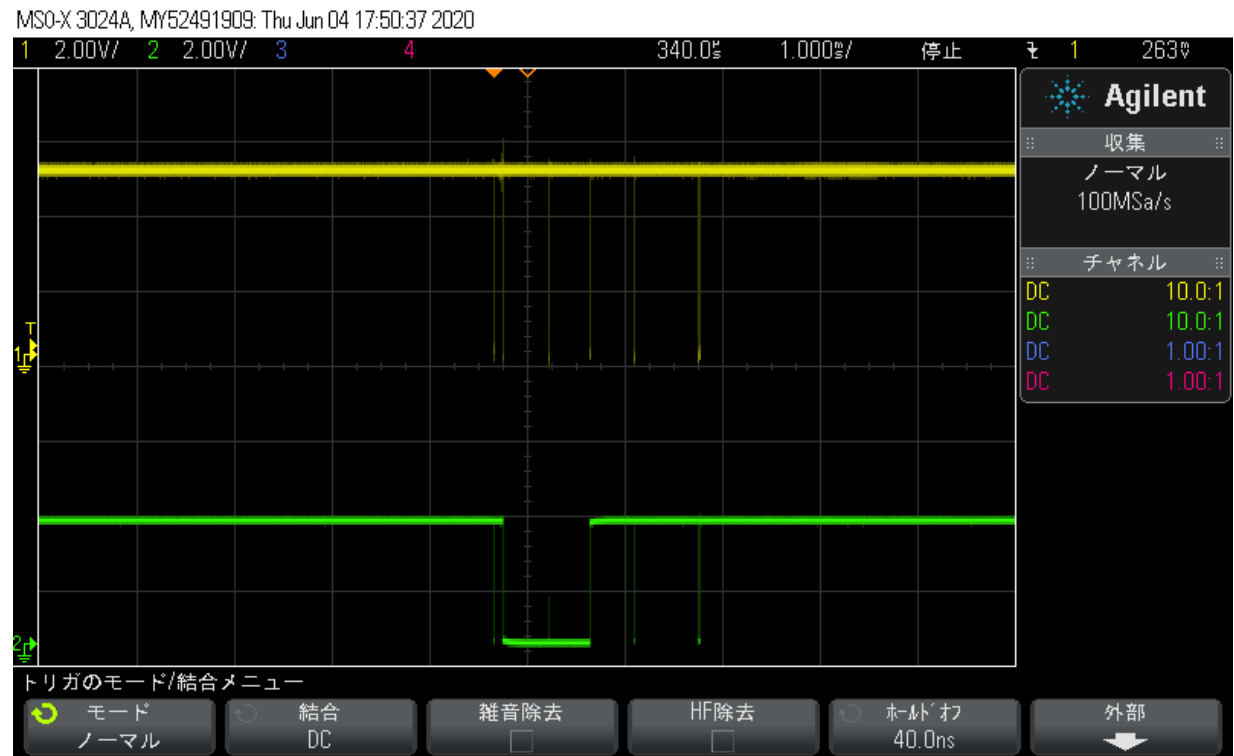
# ■ Inserting cable(Chattering) NG1



# ■ Inserting cable(Chattering) NG2



# ■ Inserting cable(Chattering) NG3



# ■ Inserting cable (Chattering) NG4

