5kVrms Isolated Half- and Full-Duplex RS-485 Transceivers

Data Sheet

Pai8485/Pai8486

1 Features

- Compatible with TIA/EIA-485-A
- Up to 5000Vrms Insulation voltage
- Logic side supply voltage (VDD1): 2.5V to 5.5V
- Bus side supply voltage (VDD2): 3V to 5.5V
- Low-EMI 500-kbps,16Mbps Data Rates
- Failsafe receiver for bus open, short, and idle
- 1/8 Unit load up to 256 nodes on bus
- High CMTI：±85kV/us (Typical)
- Operation temperature: -40°C to 105°C
- RoHS-compliant, Wide-body SOIC-16 package
- Pin compatible to most isolated RS-485 transceivers
- Safety-related certifications: (Pending)
  - –1414-VPK VIORM per DIN VDE V0884-11:2017-01
  - – 5000-V_{RMS} isolation for 1 minute per UL 1577
  - – CQC, TUV, and CSA approvals

2 Applications

- Isolated RS-485 Communication
- Solar inverter
- Factory automation & control
- Motor drives
- HVAC systems and building automation

3 General Description

The Pai84xx devices are 2PaiSemi isolated RS-485 transceivers which provide outstanding performance characteristics by using 2PaiSemi ***iDivider®*** technology.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai8485 is a Half-Duplex RS-485 Transceiver, while Pai8486 is a Full-Duplex RS-485 Transceiver. Both devices are certified with 5kVrms isolation voltage per UL 1577.

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range.

These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

The data rate of Pai8485 is 500kbps. The data rate of Pai8486 is up to 16Mbps.

4 Functional Block Diagrams

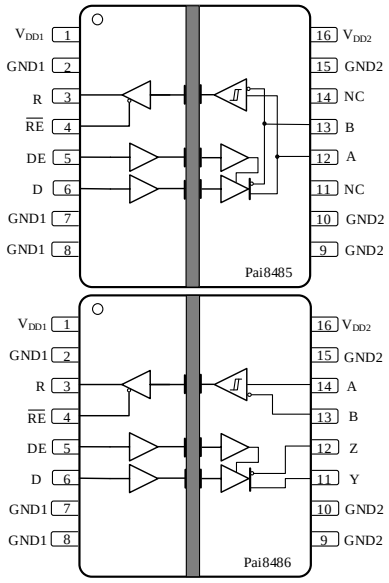

Figure1. Pai8485 & Pai8486 Functional Block Diagrams

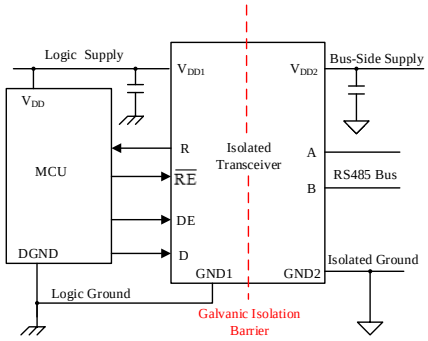

Figure2. Pai8485 Typical Application Circuit

Rev.0.2

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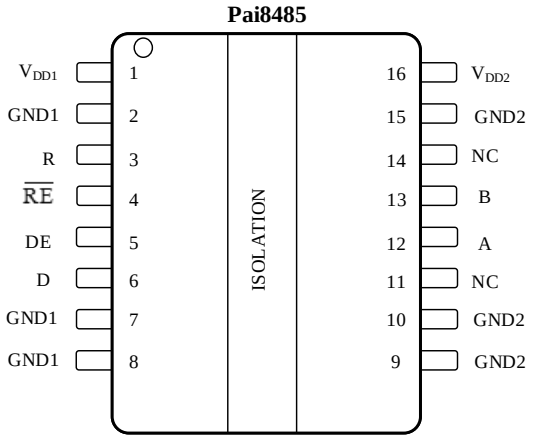
http://www.rpsemi.com/

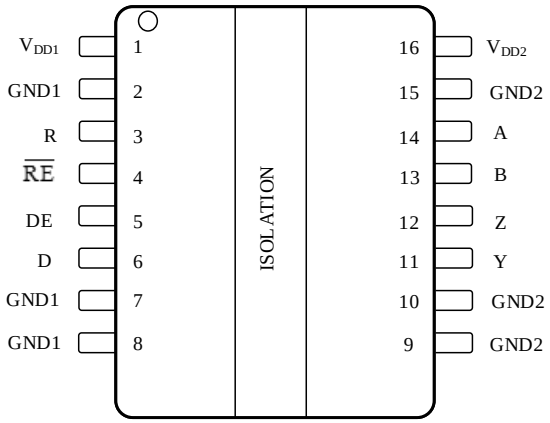
5 Pin Configuration and Functions



Pin Functions: Half-Duplex Device

PIN NO.	NAME	DESCRIPTION
1	VDD1	Logic side power supply (VDD1)
2	GND1	Ground connection for VDD1
3	R	Receiver output
4	$\overline{RE}$	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
5	DE	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
6	D	Driver input
7	GND1	Ground connection for VDD1
8	GND1	Ground connection for VDD1
9	GND2	Ground connection for VDD2
10	GND2	Ground connection for VDD2
11	NC	No internal connection
12	A	Receiver non-inverting input on the bus side
13	B	Receiver inverting input on the bus side
14	NC	No internal connection
15	GND2	Ground connection for VDD2
16	VDD2	Bus side supply voltage (VDD2)

Pai8486



Pin Functions: Full-Duplex Device

PIN NO.	NAME	DESCRIPTION
1	VDD1	Logic side power supply (VDD1)
2	GND1	Ground connection for VDD1
3	R	Receiver output
4	$\overline{RE}$	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
5	DE	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
6	D	Driver input
7	GND1	Ground connection for VDD1
8	GND1	Ground connection for VDD1
9	GND2	Ground connection for VDD2
10	GND2	Ground connection for VDD2
11	A	Receiver non-inverting input on the bus side
12	B	Receiver inverting input on the bus side
13	Z	Driver inverting output
14	Y	Driver non-inverting output
15	GND2	Ground connection for VDD2
16	VDD2	Bus side supply voltage (VDD2)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{DD1}	Supply voltage, side 1	-0.3	6	V
V_{DD2}	Supply voltage, side 2	-0.3	6	
V_{BUS}	Voltage on bus pins (A, B, Y, Z w.r.t GND2)	-7	12	V
V_I	Logic voltage level (D, DE, /RE, R)	-0.5	VDD1+0.5(3)	V
I_O	Output current on R pin		±10	mA
T_J	Maximum junction temperature		150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except bus pins(1)	±6000	V
		Bus pins and GND2(1)	±12000	
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{DD1}	Logic-side supply voltage, Side1	2.5		5.5	V
V_{DD2}	Bus-side supply voltage, Side2	3		5.5	V
V_I	Common Mode voltage at any bus terminal: A or B	-7		12	V
V_{IH}	High-level input voltage (D, DE, /RE inputs)	0.6*VDD1		VDD1	V
V_{IL}	Low-level input voltage (D, DE, /RE inputs)	0		0.3*VDD1	V
V_{ID}	Differential input voltage, A with respect to B	-12		12	V
R_L	Differential input resistance	54			Ω
I_O	Output current, Driver	-60		60	mA
I_{OR}	Output current, Receiver	-8		8	mA
1/t_{UI}	Signaling rate Pai8485			500	kbps
1/t_{UI}	Signaling rate Pai8486			16	Mbps
T_A	Ambient temperature	-40		105	°C

6.4 Device Functional Modes

Driver Functional Table(1)

V_{DD1}	V_{DD2}	INPUT D	DRIVER ENABLE DE	OUTPUTS(2)	
				Y / A	Z / B
PU	PU	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	OPEN	Hi-Z	Hi-Z
		OPEN	H	H	L
PD(3)	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z
PD	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state
(2) The driver outputs are Y and Z for a full-duplex device. The driver outputs are A and B for a half-duplex device.
(3) A strongly driven input signal can weakly power the floating VDD1 through an internal protection diode and cause an undetermined output.

Receiver Functional Table(1)

V_{DD1}	V_{DD2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	RECEIVER ENABLE ($\overline{RE}$)	OUTPUT R
PU	PU	$-0.02\ V \leqslant V_{ID}$	L	H
		$-0.2\ V < V_{ID} < 0.02\ V$	L	Indeterminate
		$V_{ID} \leqslant -0.2\ V$	L	L
		X	H	Hi-Z
		X	OPEN	Hi-Z
		Open, Short, Idle	L	H
PD(2)	PU	X	X	Hi-Z
PU	PD	X	L	H
PD(2)	PD	X	X	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state
(2) A strongly driven input signal can weakly power the floating VDD1 through an internal protection diode and cause an undetermined output.

6.5 Thermal Information

THERMAL METRIC		Pai848x WB SOIC-16	UNIT
$R_{\theta JA}$	Junction-to-Ambient thermal resistance	70	°C/W

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
IEC 60644-1				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)	⩾400	V
	Material Group	IEC 60112	I	
	Overvoltage category	Rated mains voltage ⩽ 150 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 300 V_{RMS}	I-IV	
		Rated mains voltage ⩽400 V_{RMS}	I-IV	
DIN V VDE V 0884-11 (VDE V 0884-11):2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	1000	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Basic insulation, 1.2/50 µs combination wave, VTEST = 1.3 × VIOSM (qualification)	5000	V_{PK}
q_{pd}	Apparent charge(4)	Method b1, V_{PR} = V_{IORM} × 1.5, 100% Production test with t = 1 s	⩽5	pC
C_{IO}	Barrier capacitance, input to output(5)	V_I = 0.4 sin (4E6πt)	1.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C, all pins on each side of the barrier tied together creating a 2-terminal device	$>10^{12}$	Ω
		V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) Pai848x is suitable for basic electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

The Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program[1]	DIN VDE V 0884-11:2017-01[2]	Certified under CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V rms Isolation Voltage	Basic insulation, V_{IORM} = 1414V peak, V_{IOSM} =5000V peak	Basic insulation at 1200V peak working voltage
File (pending)	File (pending)	File (pending)

6.8 Safety Limiting Values

Safety limiting(1)intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 70°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			320	mA
T_S	Safety temperature				150	℃

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: Driver

(All typical specs are at VDD1=5V, VDD2=5V, TA=25°C, Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	Open circuit voltage, unloaded bus, 3 V≤ VDD2 ≤ 5.5 V	3		VDD	V
		R_L = 54 Ω, See Figure 5	1.5	2.3		
		R_L = 100 Ω (RS-422), See Figure 5	2	2.3		
		V_{test} from –7 V to +12 V, See Figure 5	1.5			
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	R_L = 54 Ω or R_L = 100Ω, See Figure 6	-0.2	0	0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or R_L = 100Ω, See Figure 6	1	2.6	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	R_L = 54 Ω or R_L = 100Ω, See Figure 6	-0.1		0.1	
I_{OS}	Short-circuit output current	V_A or V_B at –7 V, Other input at 0 V	-200		200	mA
		V_A or V_B at 12 V, Other input at 0 V				
I_I	Input current	V_D and V_{DE} = 0V or V_D and V_{DE} = V_{DD1}	-10		10	uA
CMTI	Common-mode transient immunity	See Figure 13		85		kV/μs

6.10 Electrical Characteristics: Receiver

(All typical specs are at VDD1=5V, VDD2=5V, TA=25°C, Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH+}	Positive-going input threshold voltage			-110	-10	mV
V_{TH-}	Negative-going input threshold voltage		-200	–140		mV
V_{hys}	Hysteresis voltage (V_{TH+} – V_{TH-})			30		mV
V_{OH}	Output high voltage on the R pin	V_{ID} = 200 mV, I_O = –4 mA	V_{DD1}-0.4			V
V_{OL}	Output Low voltage on the R pin	V_{ID} = –200 mV, I_O = 4 mA			0.4	V
$I_{O(Z)}$	Output high-impendance current on the R pin	V_I = –7 to 12 V, Other input = 0 V	-1		1	uA
I_{i1}	Bus input current	V_A or V_B = 12 V, Other input at 0 V		0.04	0.1	mA
		V_A or V_B = 12 V, V_{DD} = 0, Other input at 0 V		0.06	0.13	
		V_A or V_B = –7 V, Other input at 0 V	-0.1	–0.04		
		V_A or V_B = –7 V, V_{DD} = 0, Other input at 0 V	-0.05	–0.03		
I_i	Input Current on the /RE pin	$V_{/RE}$ = 0V or $V_{/RE}$ = V_{DD1}	-10		10	uA
R_{ID}	Differential input resistance	A, B	96			kΩ
CMTI	Common-mode transient immunity	See Figure 13		85		kV/μs

6.11 Supply Current

over recommended operating condition (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD1}	Logic-side supply current	/RE at 0 V or V_{DD1}, DE at 0 V or V_{DD1} (VDD1=3.3V)			3.2	mA
		/RE at 0 V or V_{DD1}, DE at 0 V or V_{DD1} (VDD1=5V)			3.3	mA
I_{DD2}	Bus-side supply current	/RE at 0 V or V_{DD1}, DE at 0 V, No load			4.4	mA

6.12 Switching Characteristics: Driver

(All typical specs are at VDD1=5V, VDD2=5V, TA=25°C, Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver (Pai8485)						
t_{PLH}, t_{PHL}	Propagation delay	See Figure 7		0.5		us
PWD(1)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 7		20		ns
t_r, t_f	Differential output signal rise and fall time	See Figure 7		1		ns
t_{PZH}	Enable time	See Figure 8		300		ns
t_{PZL}	Enable time	See Figure 9		300		ns
t_{PHZ}	Disable time	See Figure 8		25		ns
t_{PLZ}	Disable time	See Figure 9		25		ns
Driver (Pai8486)						
t_{PLH}, t_{PHL}	Propagation delay	See Figure 7		20		ns
PWD(1)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 7		2.5		ns
t_r, t_f	Differential outputsignal rise and fall time	See Figure 7		1.6		ns
t_{PZH}	Enable time	See Figure 8		23		ns
t_{PZL}	Enable time	See Figure 9		24		ns
t_{PHZ}	Disable time	See Figure 8		27		ns
t_{PLZ}	Disable time	See Figure 9		26		ns

6.13 Switching Characteristics: Receiver

(All typical specs are at VDD1=5V, VDD2=5V, TA=25°C, Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver (Pai8485)						
t_{PLH}, t_{PHL}	Propagation delay	See Figure 10		80		ns
PWD(1)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 10		10		ns
t_r, t_f	Differential outputsignal rise and fall time	See Figure 10		1		ns
t_{PZH}	Enable time	See Figure 11 and Figure 12		9		ns
t_{PZL}	Enable time	See Figure 11 and Figure 12		9		ns
t_{PHZ}	Disable time	See Figure 11 and Figure 12		25		ns
t_{PLZ}	Disable time	See Figure 11 and Figure 12		6		ns
Receiver (Pai8486)						
t_{PLH}, t_{PHL}	Propagation delay	See Figure 10		25		ns
PWD(1)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 10		5		ns
t_r, t_f	Differential outputsignal rise and fall time	See Figure 10		1		ns
t_{PZH}	Enable time	See Figure 11 and Figure 12		9		ns
t_{PZL}	Enable time	See Figure 11 and Figure 12		10		ns
t_{PHZ}	Disable time	See Figure 11 and Figure 12		25		ns
t_{PLZ}	Disable time	See Figure 11 and Figure 12		6		ns

7 Parameter Measurement Information

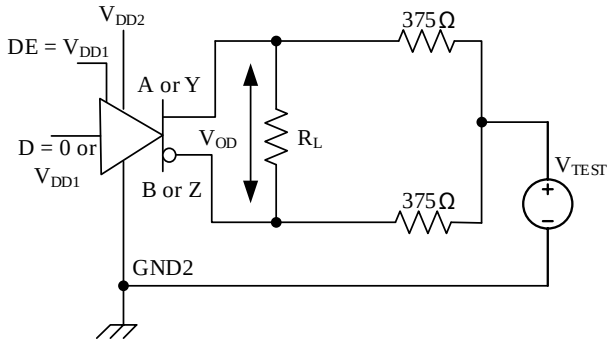
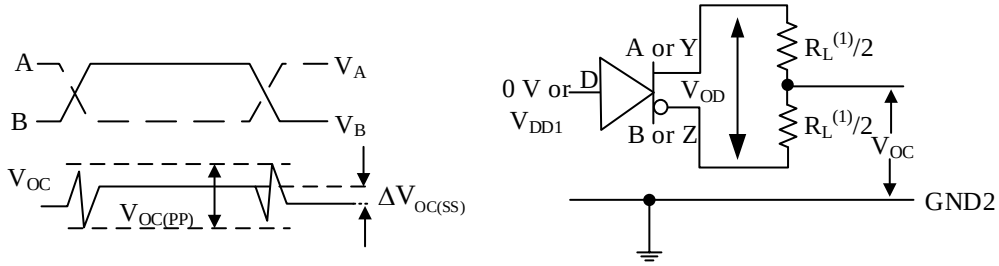
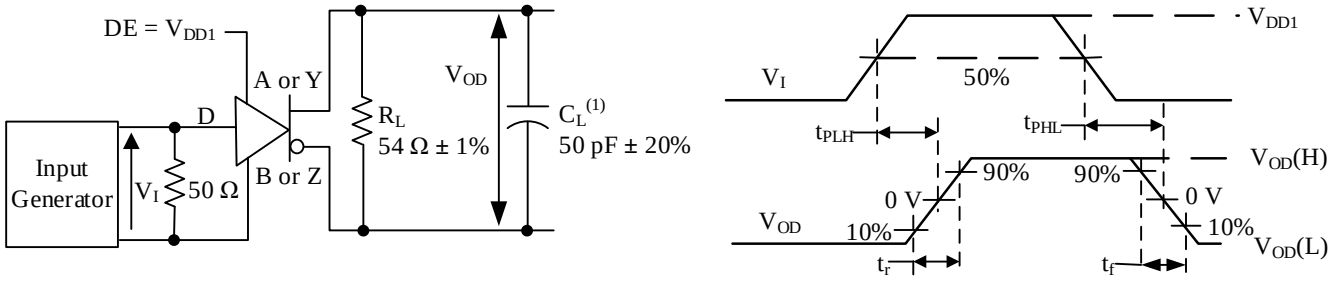


Figure 5. Driver Voltages



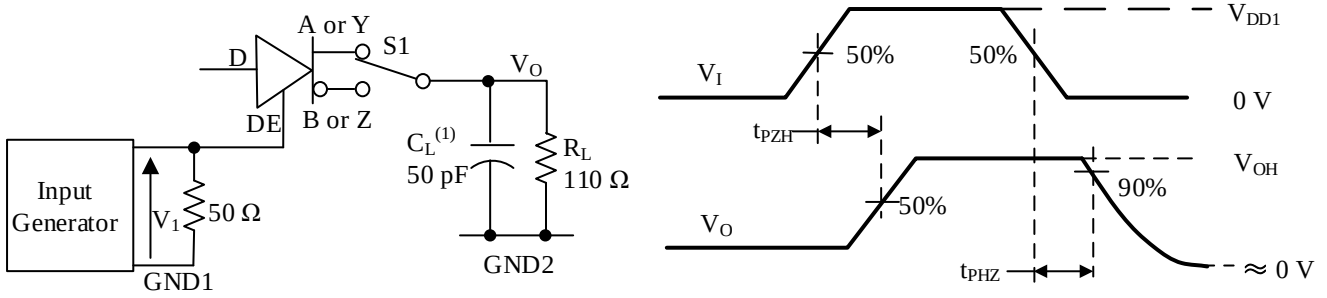
(1) R_L = 100 Ω for RS422, R_L = 54 Ω for RS-485

Figure 6. Driver Voltages



(1) C_L includes fixture and instrumentation capacitance.

Figure 7. Driver Switching Specifications



(1) C_L includes fixture and instrumentation capacitance.

Figure 8. Driver Enable and Disable Times

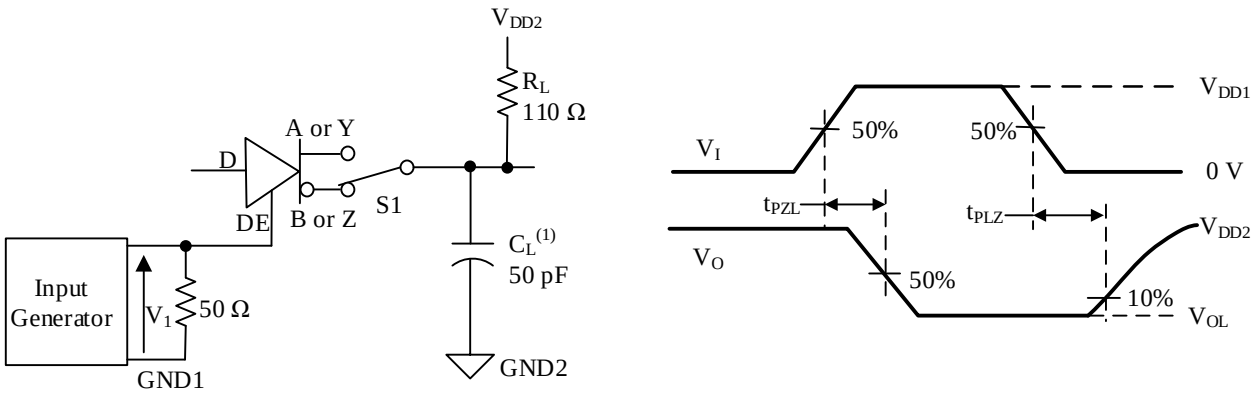


Figure 9. Driver Enable and Disable Times

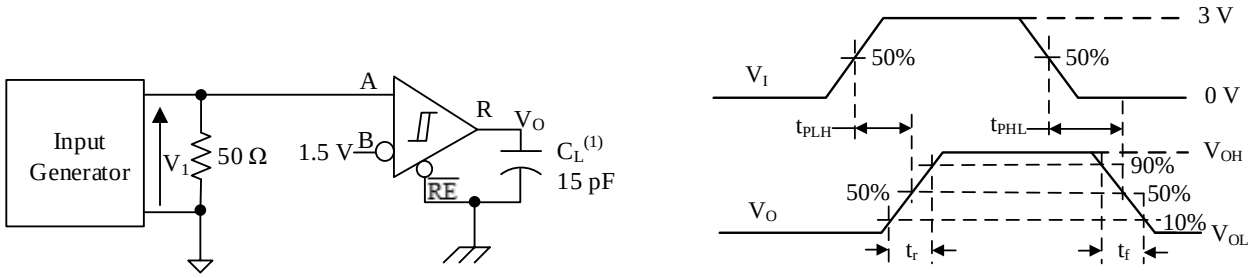


Figure 10. Receiver Switching Specifications

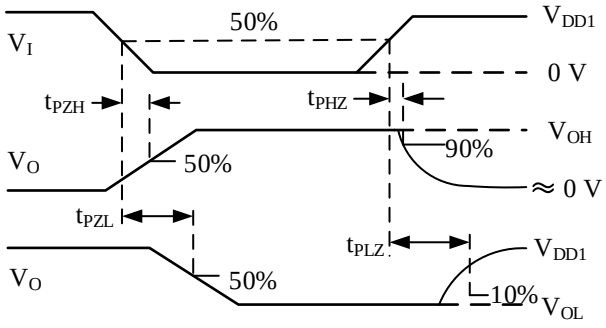


Figure 11. Receiver Enable and Disable Times

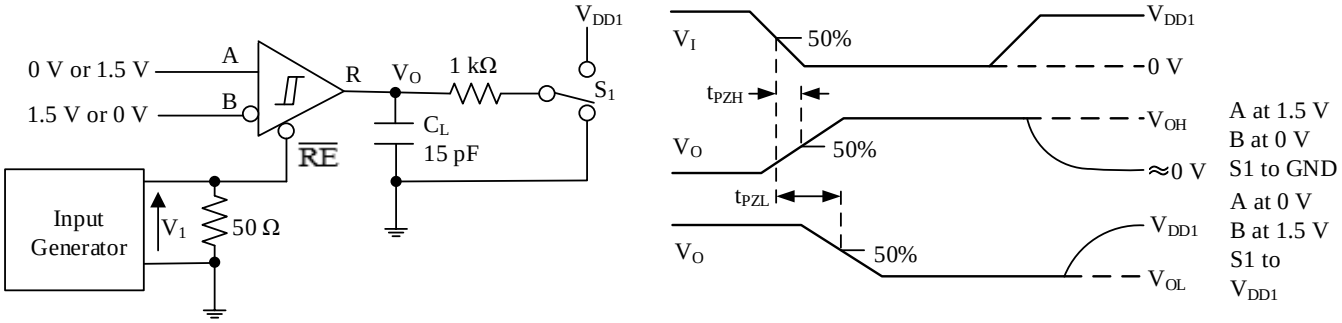
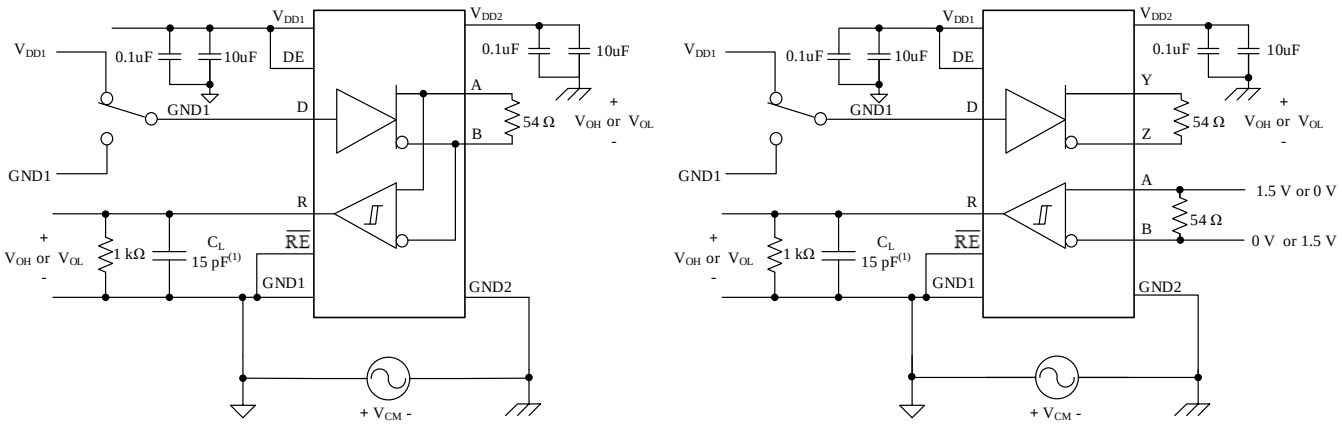


Figure 12. Receiver Enable and Disable Times



(1) C_L includes fixture and instrumentation capacitance.

Figure 13. Common Mode Transient Immunity (CMTI)—Half Duplex (Left) and Full Duplex (Right)

8 Detailed Description

8.1 Overview

The Pai84xx devices are 2PaiSemi isolated RS-485 transceivers which provide outstanding performance characteristics by using 2PaiSemi ***iDivider®*** technology.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai8485 is a Half-Duplex RS-485 Transceiver, while Pai8486 is a Full-Duplex RS-485 Transceiver. Both devices are certified with 5kVrms isolation voltage per UL 1577. These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The data rate of Pai8485 is 500kbps. The data rate of Pai8486 is up to 16Mbps.

Figure 14 shows the functional block diagram of a half-duplex devices and Figure 15 shows the functional block diagram of the full-duplex devices.

8.2 Functional Block Diagrams

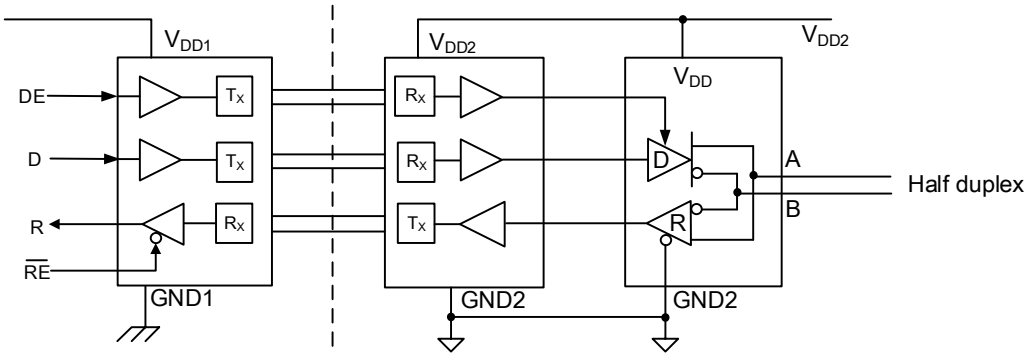


Figure 14. Half-Duplex Block Diagram

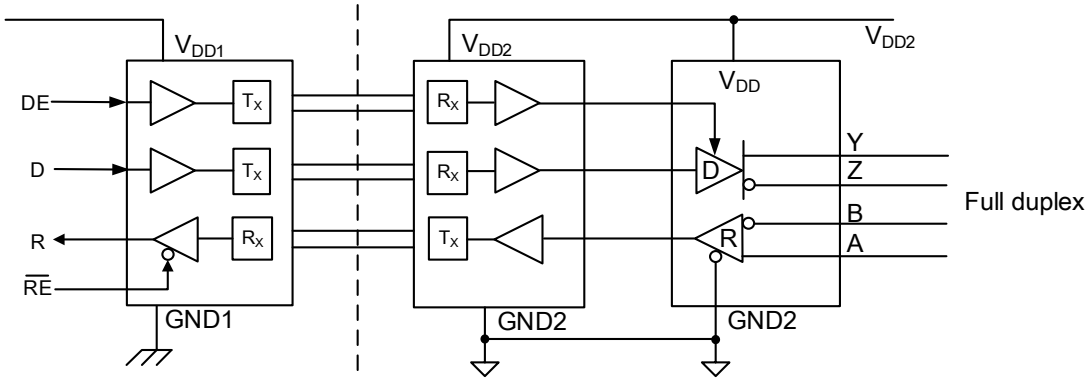


Figure 15. Full-Duplex Block Diagram

8.3 Device I/O Schematics

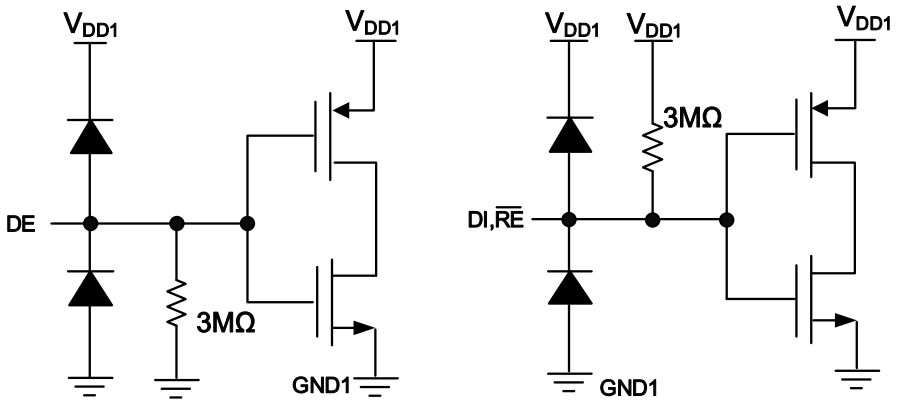


Figure 16. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the 2PAI component specification, and 2PAI does not warrant its accuracy or completeness. 2PAI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The Pai848x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

9.2 Typical Application

The Pai84xx devices are designed for bidirectional data transfer on multipoint RS-485 networks.
An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T, to remove line reflections. The value of R_T matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.
Half-duplex implementation, as shown in Figure 17, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.
Full-duplex implementation, as shown in Figure 18, requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair.

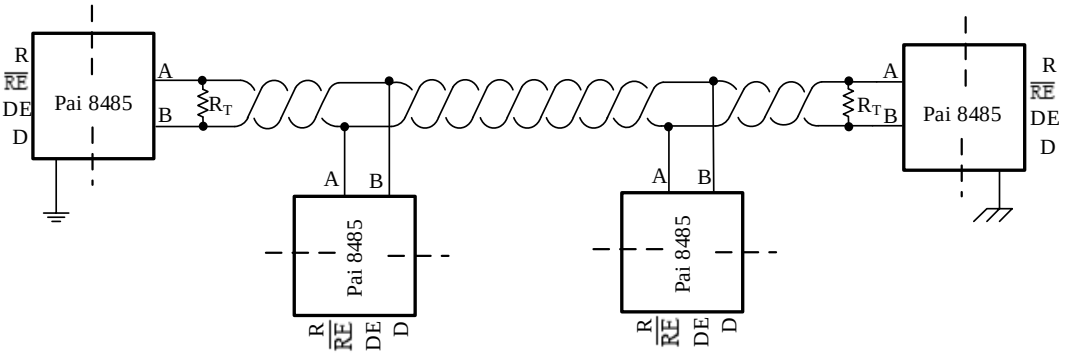


Figure 17. Half-Duplex Transceiver Configurations

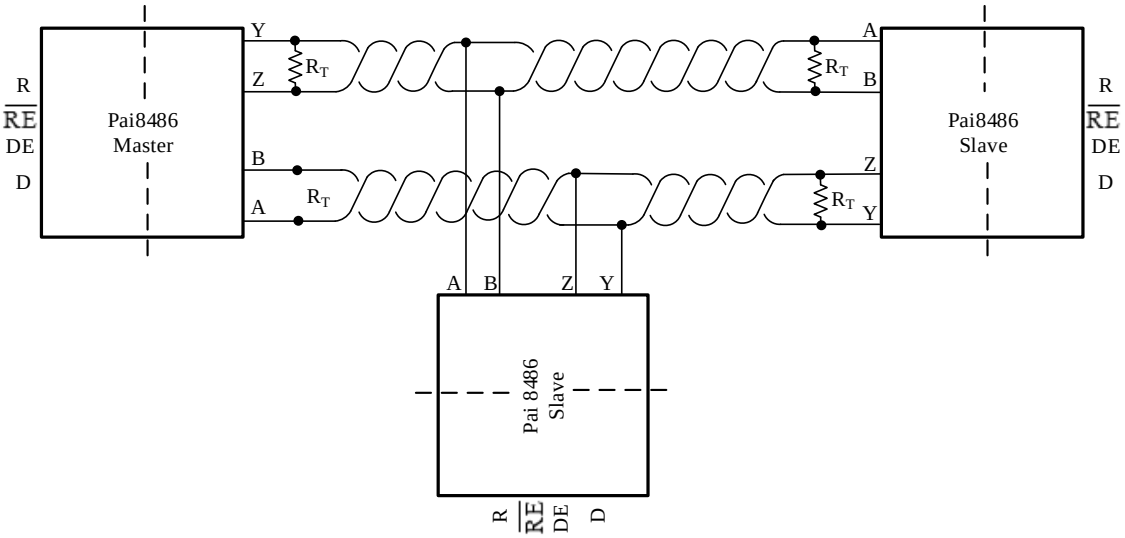


Figure 18. Typical RS-485 Network With Full-Duplex Transceivers

9.3 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the Pai 84xx devices only require external bypass capacitors to operate.

9.4 Detailed Design Procedure

The RS-485 bus is a robust electrical interface suitable for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes

9.5 Bus Loading

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12 kΩ. Standard-compliant drivers must be able to drive 32 of these ULs.The Pai84xx devices have 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

10 Power Supply Recommendations

To make sure device operation is reliable at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the logic and transceiver supply pins (VDD1 and VDD2). The capacitors should be placed as near to the supply pins as possible. Additionally, a 10 µF bulk capacitor on VDD2 improves transceiver performance during bus transitions in transmit mode.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 19). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

Put the V_{DD2} bypass capacitors on the top layer and as near to the device pins as possible. Do not use vias to complete the connection to the V_{DD2} and GND2 pins. If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

11.2 Layout Example

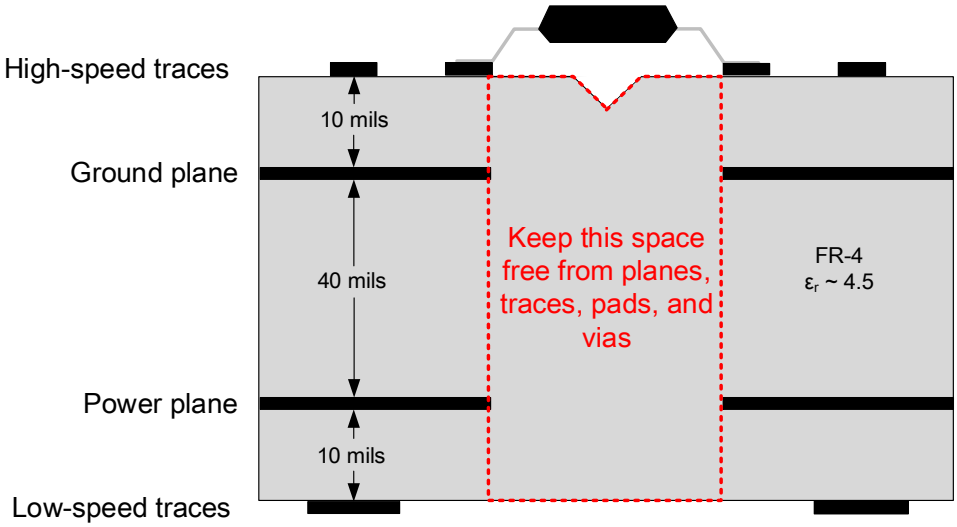


Figure 19. Recommended Layer Stack

OUTLINE DIMENSIONS

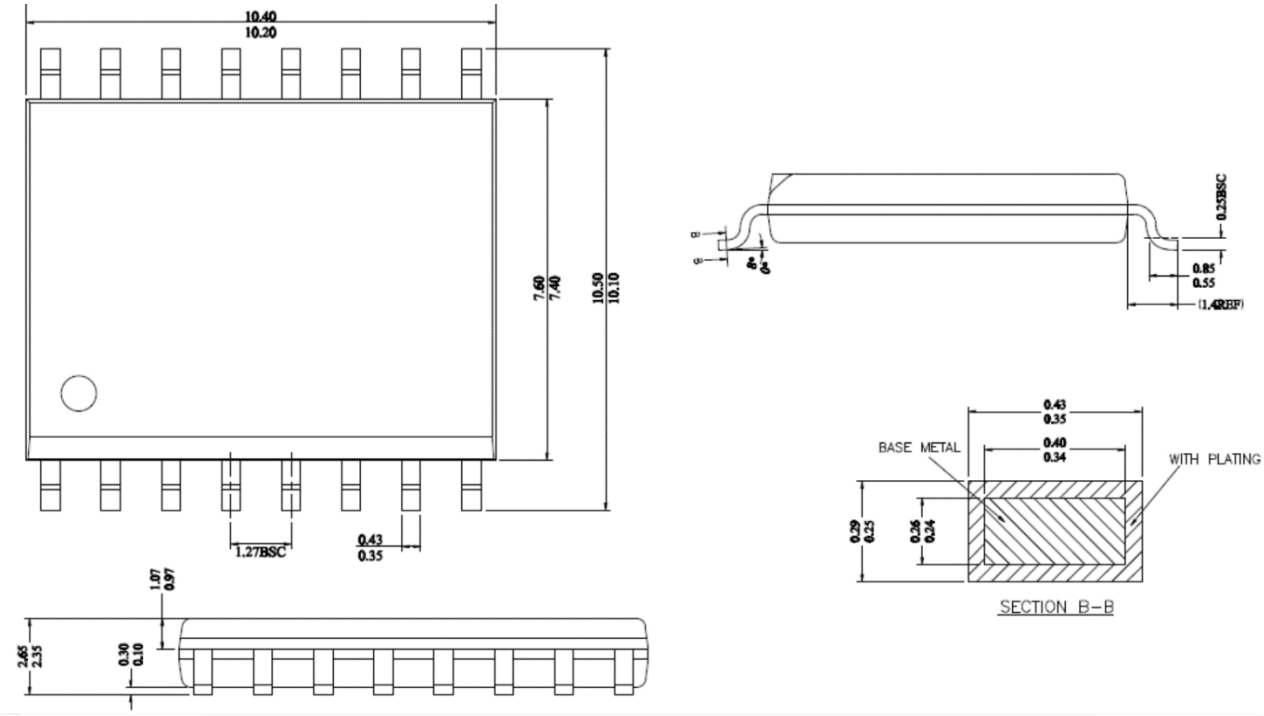


Figure 20.16-Lead Wide Body SOIC [WB SOIC-16] Outline Package–dimension unit(mm)

Land Patterns

16-Lead Wide Body SOIC [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the π1xxxxx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

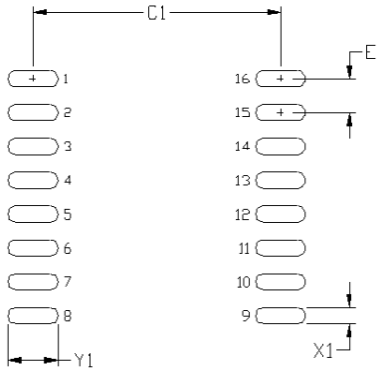


Figure 21. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

Table 17. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

Note：

1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

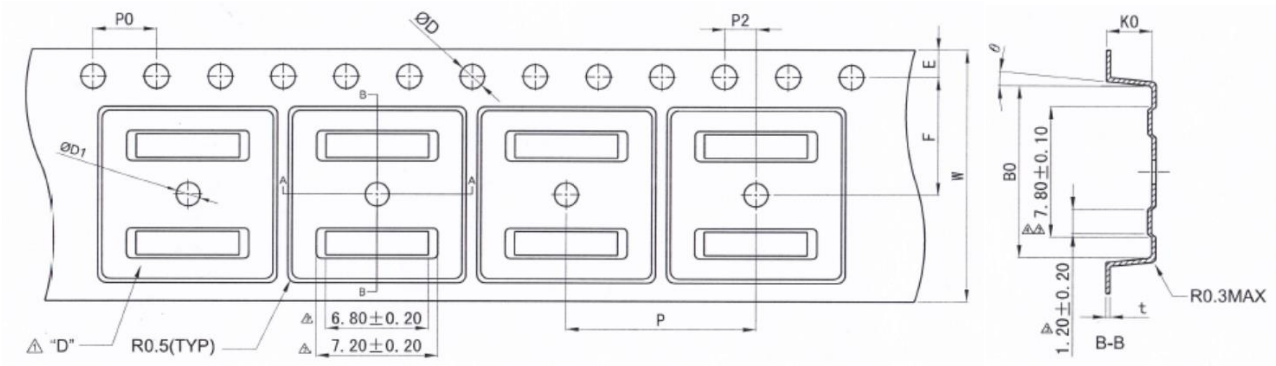
Top Marking

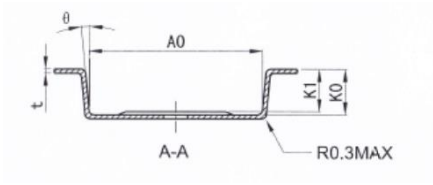
Line 1	PaiXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

Figure 22. Top marking

REEL INFORMATION

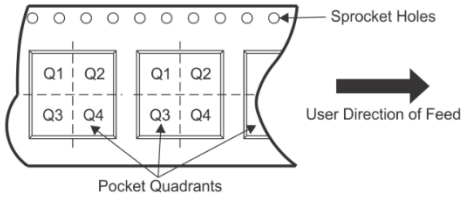
16-Lead Wide Body SOIC [WB SOIC-16]





Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP



Note：The Pin 1of the chip is in the quadrant Q1

Figure 23.16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

ORDERING GUIDE

Model Name	Duplex	Max Data Rate	Isolation Rating	No.of Nodes	Temperature Range	Package	MSL Peak Temp [1]	MOQ/ Quantity per reel[2]
Pai8485-W1R	Half	500kbps	5 kV RMS	256	−40~105°C	WB SOIC-16	Level-2-260C-1 YEAR	1500
Pai8486-W1R	Full	16Mbps	5 kV RMS	256	−40~105°C	WB SOIC-16	Level-2-260C-1 YEAR	1500

[1.] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[2.] MOQ, minimum ordering quantity.

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REVISION HISTORY

Revision	Date	Page	Change Record
0.2	2022.11	All	Initial version