Application Report
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IWR1xxx Radar Digital Front End (DFE)

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ABSTRACT

The IWR family of radar processors have multiple transmitter and four receiver sections in each device. The radar processors utilize Frequency Modulated Continuous Wave (FMCW) processing. This application report provides a receiver simplified description and discusses the digital front-end processing.

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Trademarks

1 Introduction

DFE is a portion of the IWR1xxx receiver architecture (see Figure 1). FMCW can be separated into a reference waveform generated by the chirp generator with the frequency multiplier, a transmitter that has RF power amplifiers and phase offset to generate the RF signal for the transmit antenna, and a receiver section that receives a signal from the receive antenna, amplifies it, provides a block down conversion, filtering, frequency translation, and further baseband processing.

The Tx reference waveform (chirp parameters), receiver configuration, the Analog-to-Digital Converter (ADC) sample rate, the receiver desired bandwidth, and the number of ADC samples are used to provide blocks of chirp Rx samples for baseband processing. If the receiver is operating in real sampling mode, the Inphase ADC and DFE are used. If the receiver is operating in quadrature mode, the Inphase ADC, Quadrature ADC, and DFE are used. After DFE, the output is further processed:

- In hardware accelerator and ARM® software (IWR1443), using internal calculations, the MSS ARM outputs the calculated data. In the IWR1443, the hardware accelerator output can be exported to an external DSP over the CSI-2 interface.
- In DSP and ARM software (IWR1642), using internal calculations, the MSS ARM outputs the calculated data.

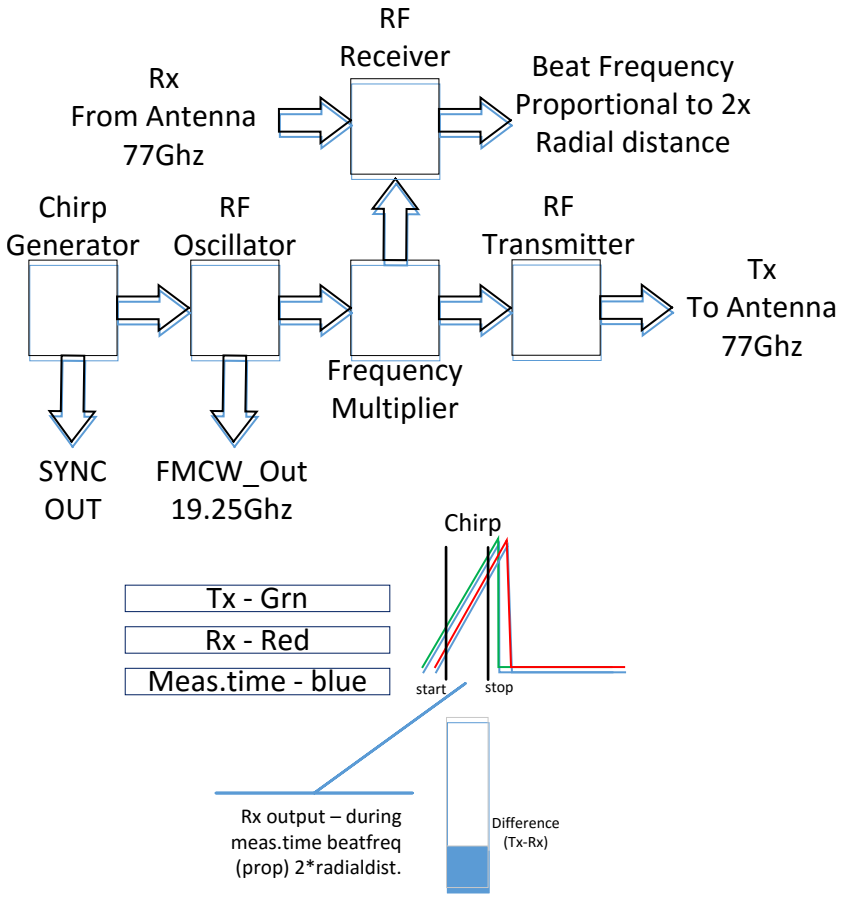

Figure 1. FMCW Radar Simplified Block Diagram

1.1 DFE Operating Modes

DFE can be operated in one of three modes; the DFE operates at 90% of the allowed Nyquist bandwidth for the selected mode (see Figure 2):

- Real – Inphase only sampling, the first Nyquist zone is used for 0 fs to .45 fs, which requires further processing to reject the sample image and generally has an lower Signal-to-Noise Ratio (SNR).
- Complex 1x – Quadrature sampling, special treatment of complex sample rate and tuned frequency; the effect of this mode is to provide a 0.05 fs to .95 fs single sided signal.
- Complex 2x – Quadrature sampling, the output –fs/2 to fs/2 range has a passband of -.45 fs to .45 fs.

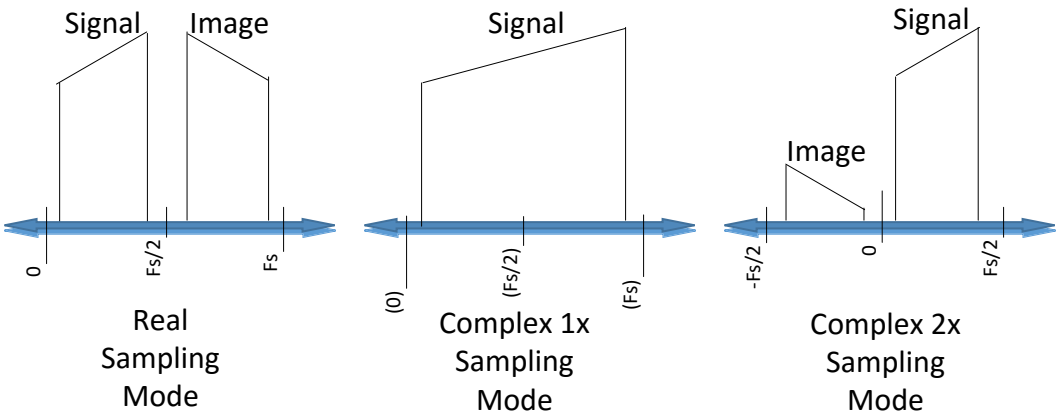

Figure 2. Output Signal Representation With DFE Modes

1.2 DFE Example Configuration for Target BW

The distance calculated from the FMCW radar is based on the baseband Rx output frequency. The chirp parameters are used to provide resolution and distance. Delta frequency is used for other types of processing for velocity and angle; multiple receivers do further processing. The important parameter for the chirp profile is based on Chirp-to-Chirp sample period and additional parameters. Table 1 provides an illustration of the max frequency in each set of modes, the mmwave SDK has APIs to adjust these parameters.

provides specific configurations for the receiver operating mode and DFE parameters.

Table 1. Example ADC and DFE Sample Rates

IWR No.	ADC Mode	DFE OP Mode	BW-maxbeatfr. (.45*OutFs)	1st Stage Inrate	1st Stage Outrate	Special Image Suppression	2nd Stage Outrate	Notes
1443	Full Cmplx	Cmp2x	8.4e6	1800e6	100e6	No	18.75e6	7.5 Mhz BW
1443	Full Cmplx	Cmp1x	16.8e6	1800e6	100e6	Yes	18.75e6	15 Mhz BW
1443	Full Cmplx	Cmp1x	11.2e6	1800e6	100e6	Yes	12.5e6	10 Mhz BW
1443	Full Cmplx	Cmp1x	8.4e6	1800e6	100e6	Yes	9.375e6	7.5 Mhz BW
1443	Low Cmplx	Cmp1x	5.6e6	900e6	50e6	Yes	6.25e6	5 Mhz BW
1642	Low Cmplx	Cmp1x	5.6e6	900e6	50e6	Yes	6.25e6	5 Mhz BW

2 Digital Front End (DFE)

The direct down conversion receiver has several operating modes and selectable features to support signal processing. The main features are:

- Receiver – Complex Down conversion Mixer – the RF signal from the LNA is converted to a complex (Inphase and Quadrature)
- Receiver – Analog filtering is applied to the downconverted mixer output
- Receiver – Sigma Delta analog-to-digital conversion - sample the down converted and Nyquist filtered RF signals. When complex sampling is used, there is an inphase and a quadrature ADC output. When real sampling is used, there is an Inphase ADC output.
- DFE – First stage filtering and decimation – the sampled RF signal is filtered and decimated
- DFE – IQ bias and gain correction – the output from the first stage filtering and decimation has DC removal; I and Q gain balancing is applied to reduce the IQ bias and gain imbalance if complex sampling is used.
- DFE – Second stage filtering and decimation – software controlled filtering, decimation, resampling, complex mixing are performed; the software APIs are used to set the mode and output sample rate for further processing.

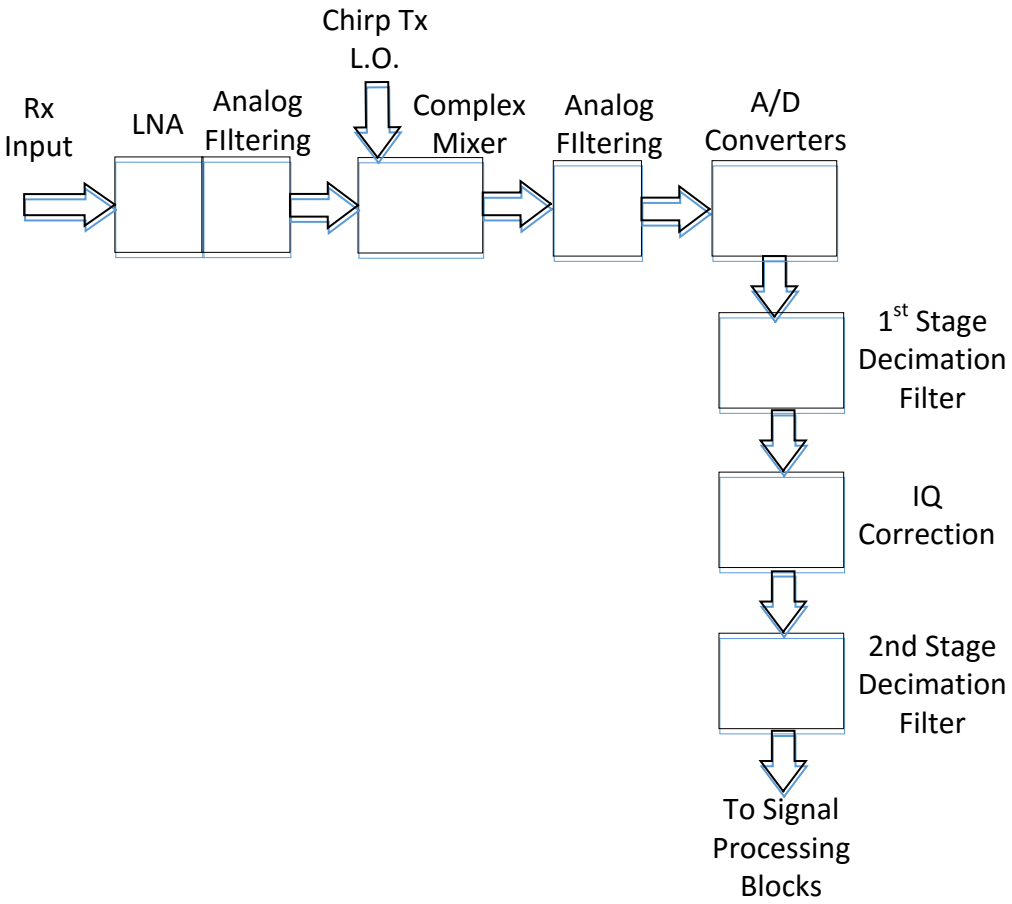

Figure 3. FMCW Receiver Block Diagram

The DFE contains the three processing blocks shown in Figure 3:

- First stage decimation filter
- IQ correction
- Second stage decimation filter, including image suppression filter

The mode (Real, Complex1x, Complex 2x), ADC sample rate, second stage decimation filter settings are controlled through the mmWave API, rlSetAdcOutConfig. The IQ correction is performed as part of the RSS calibration for each receiver channel.

2.1 DFE First Stage Decimation Filter

The Quadrature (I and Q) or real (I only) output of the A-D Converter is filtered and decimated. The multi-stage decimation filter, decimates by 18. The full ADC output of this filter section typically provides a 100 Msps output. The lower ADC output is 50 Msps output.

2.2 DFE IQ Correction

The DFE IQ provides for calibration bias correction and calibration gain correction. The output of this section is monitored for calibration by the BSS/RSS subsystem. The bias removal and IQ gain correction is expected to provide >35 db image rejection ratio (IMRR). The IMRR is a ratio of the desired signal to its image.

2.3 DFE Second Stage Decimation Filter

The DFE second stage decimation filter combines a bank of 5 decimate by 2 filters, a fractional resampler, and final stage decimation filter. The overall second stage decimation and resampling convert the 100 Msps to the final quadrature or real only output. The filters in the 2nd stage decimation filter provide for 45% bandwidth (they are decimate by 2 filters) and have 60db stop band rejection. The resampler provides for fractional decimation ratios of 1 to 2.

There are two operating modes of the DFE Second Stage Decimation Filter:

- Normal low pass filter and decimation
- Image suppression

In the complex 2x or real mode, the low-pass digital filter and decimate by 2 stage are used.

In the complex 1x mode, the image suppression feature is used. This feature uses several blocks together: complex mixer, decimate by 2 low-pass filter, low-pass digital filter, complex mixer, and decimate by 2 stage.

In Figure 4 shows an example of a desired signal range of .1 MHz to 4.9 Mhz for further processing, using each of the sampling modes.

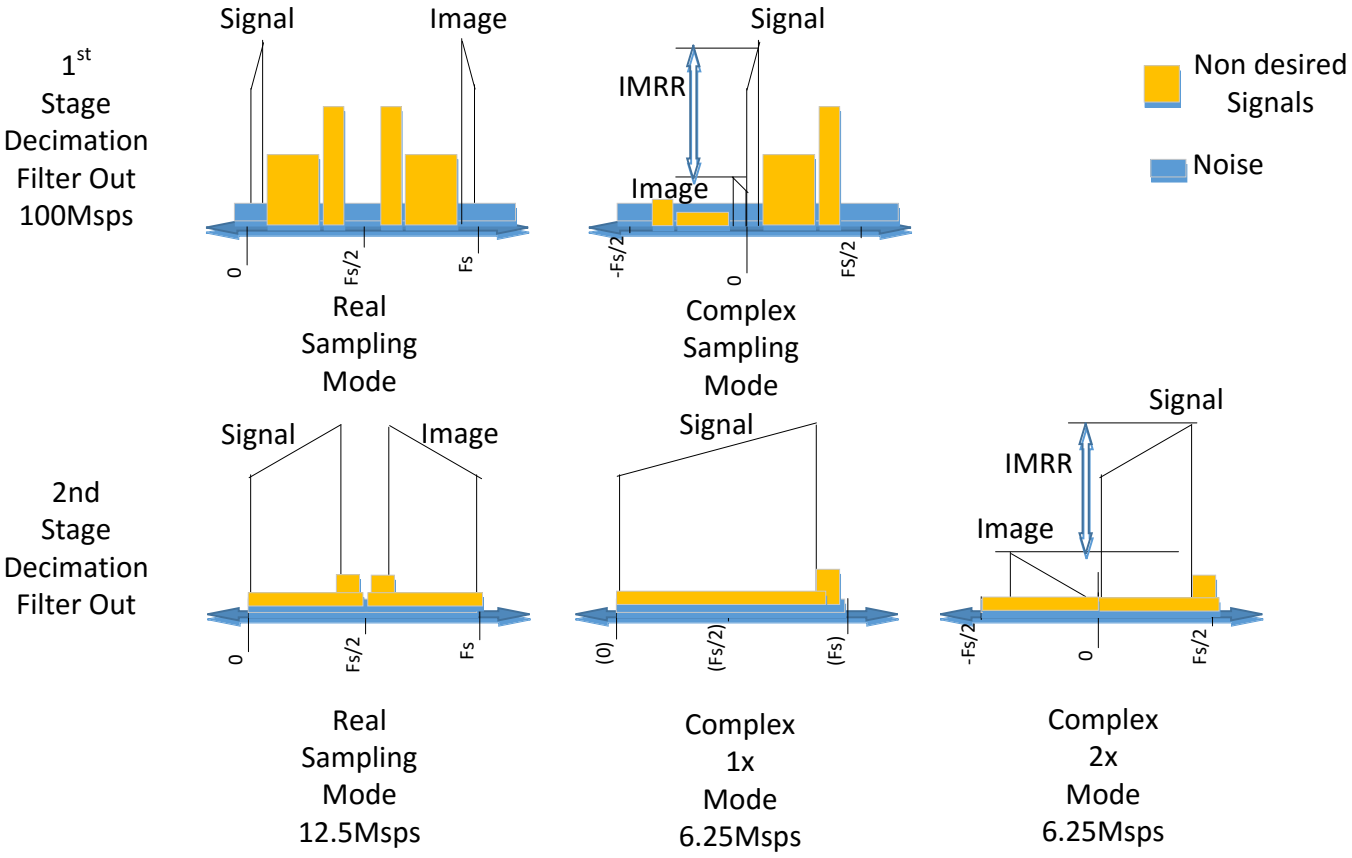

Figure 4. 5 Mhz Signal Bandwidth Example

The output of the second stage decimation filter goes to the ADC buffer in memory. The output data can be rounded and saturated for 12-, 14-, or 16-bit signed integer values. The data format is controlled by the rlGetAdcOutConfig mmWave API. The ADC output buffer is sent to the RSS/BSS calibration processing for gain, and IQ correction in the receiver. The ADC output buffer is sent to the CSI-2 external interface, or processed in the hardware accelerator (IWR1443) or DSP subsystem (IWR1642). A special output is possible for IWR1443 to send the hardware accelerator output over CSI-2.

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