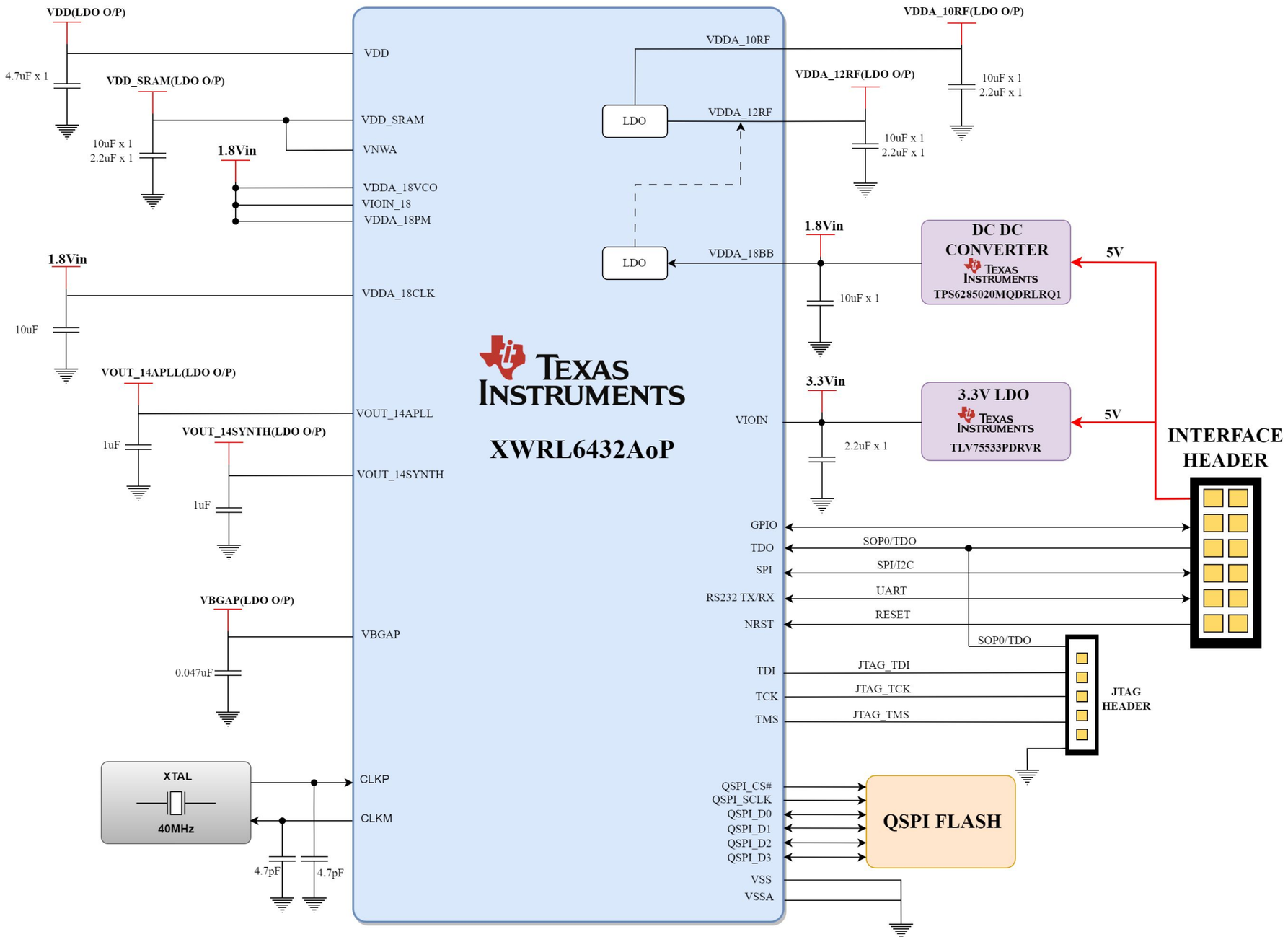
BLOCK DIAGRAM

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
NA	NA	NA	Chethan Kumar	Baseline Schematics

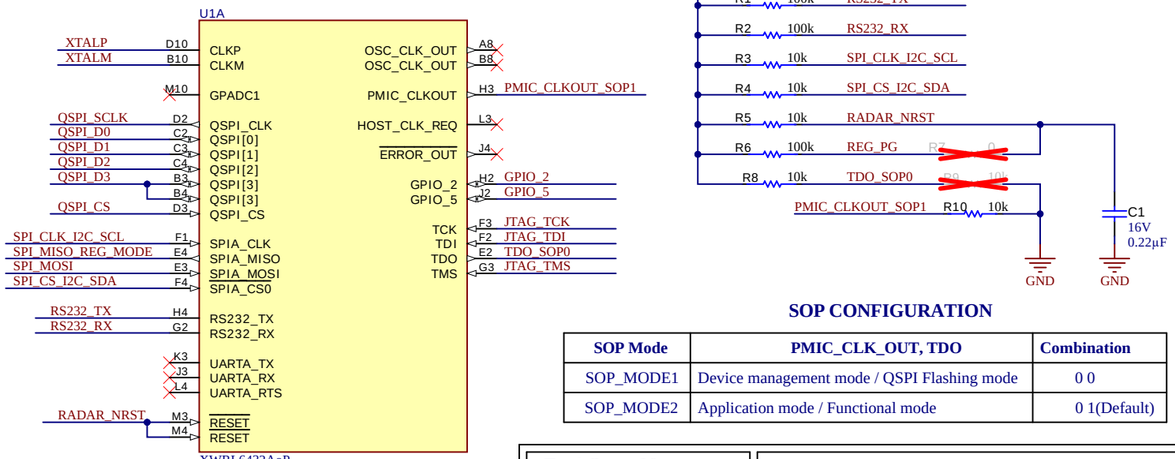


Orderable: xWRL6432AOP_REF		Designed for: Public Release	Mod. Date: 04-09-2023
TID #: N/A		Project Title: xWRL6432 AOP Reference design	
Number: TI DEV	Rev: A	Sheet Title: BLOCK DIAGRAM	
SVN Rev: Not in version control		Assembly Variant: 001_IWR	Sheet: 1 of 2
Drawn By: Texas Instruments		File: 6432AOP_REF_Block_Diagram.SchDoc	Size: B
Engineer: Texas Instruments		Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com

xWRL6432AOP REFERENCE Design

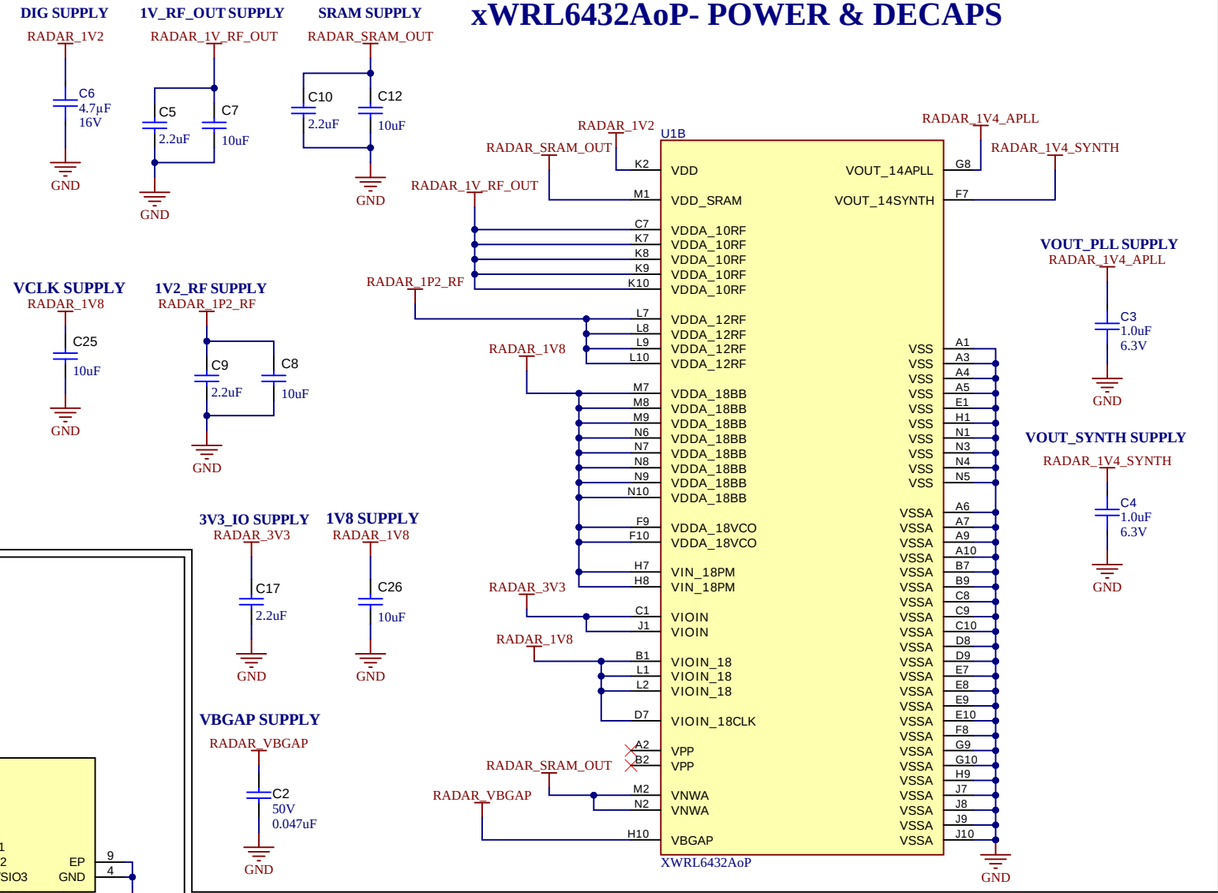
xWRL6432AoP- INTERFACE



SOP CONFIGURATION

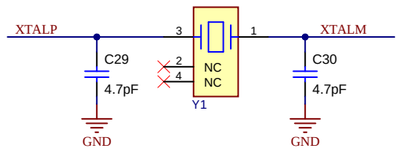
SOP Mode	PMIC_CLK_OUT, TDO	Combination
SOP_MODE1	Device management mode / QSPI Flashing mode	0 0
SOP_MODE2	Application mode / Functional mode	0 1(Default)

xWRL6432AoP- POWER & DECAPS

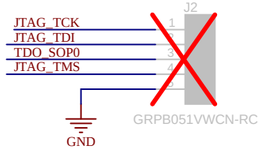


Total Caps : 28
Total Resistors : 20
Total Inductors : 2
Total IC : 4
Crystal : 1
MOSFET: 1
Connector: 2

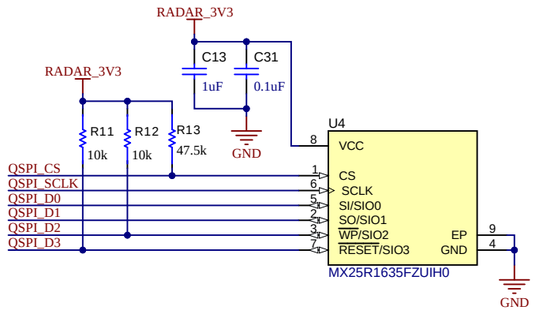
40 MHz CRYSTAL OSCILLATOR



JTAG HEADER

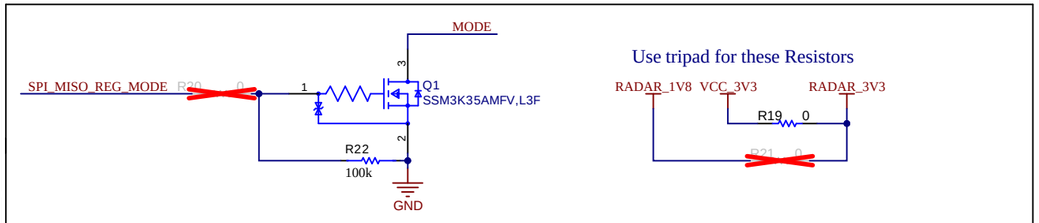


QSPI FLASH

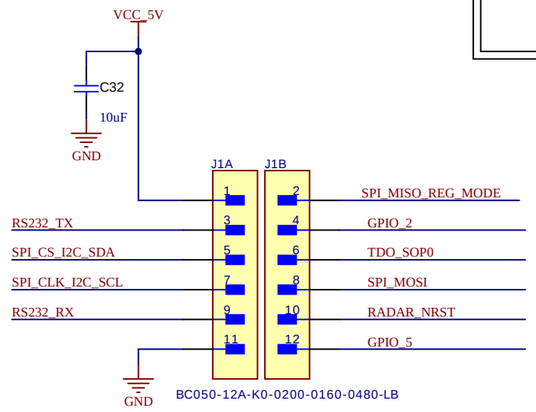


Design note:

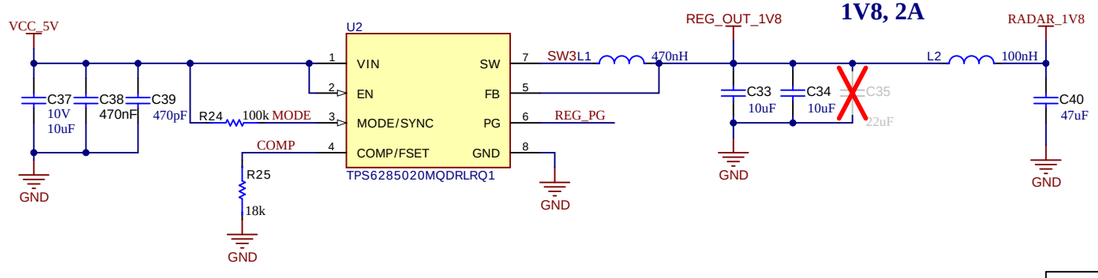
Alternate Flash part is MX25U1632FZUI02 supports VCC from 1.65V to 2.0V
Current design MX25R1635FZUIH0 Flash supports VCC from 1.65V to 3.3V



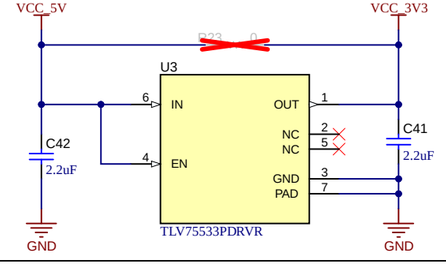
INTERFACE HEADER



DC DC REGULATOR - 1.8V



3.3V LDO, 500mA



Orderable: xWRL6432AOP_REF	Designed for: Public Release	Mod. Date: 07-09-2023
TID #: N/A	Project Title: xWRL6432 AOP Reference design	
Number: TI DEV Rev: A	Sheet Title: 6432aop Chip	
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 2 of 2
Drawn By: Texas Instruments	File: 6432AOP_REF_Chip.SchDoc	Size: B
Engineer: Texas Instruments	Contact: http://www.ti.com/support	

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