

Revisions		
X	5/11/2018	Initial Release
X1	5/15/2018	IC1B AWR1642 Pins J5 H5 G5 Net name was AR-1p3-RF2 now AR-1p3-RF1 Various Typos Fixed
A	7/10/2018	Added PMIC PG to nRESET of AWR1642 Buffered 5V Legacy Display output to reduce leakage Changed GP-ADC Input Scaling per TI's Recommendations Released to Fab

Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	εr	Copper Coverage	Mask Thickness	
1		Rogers 4835 4mil core/H/1 Low Pro	Rogers 4835	0.689	2.067		100.000		
2				4.000	4.000	3.480			
					1.260	1.260		73.000	
			Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.830	3.700		
			Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.830	3.700		
3			Iteq IT 180A 28 mil core 1/1	FR4	1.260	1.260		69.000	
4				28.000	28.000	4.280			
				1.260	1.260		48.000		
		Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.691	3.700			
		Iteq IT 180A Prepreg 1080	Dielectric	4.195	2.691	3.700			
5				1.260	1.260		72.000		
6		Iteq IT 180A 4 mil core 1/H	FR4	4.000	4.000	3.790			
				0.689	2.067		100.000		

Copper Thickness = 9.173 | Dielectric Thickness = 47.041 | Solder Mask Thickness = 0.000 | Stack Up Thickness = 56.214 | Stack Up Thickness with Soldermask = 56.214 | Stack Up Cost = 0.00 |

Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	Edge Coupled Surface Microstrip 1B	1	2	0	5.200	5.000	0.000	102.650	102.650	10.000
2	Surface Coplanar Strips With Lower Ground 1B	1	2	0	7.080	0.000	8.000	51.680	51.680	10.000
3	Surface Coplanar Strips With Lower Ground 1B	1	2	0	6.979	0.000	5.061	50.000	50.000	10.000
4	Edge Coupled Surface Microstrip 1B	6	5	0	5.661	6.339	0.000	100.000	100.000	10.000

Notes:

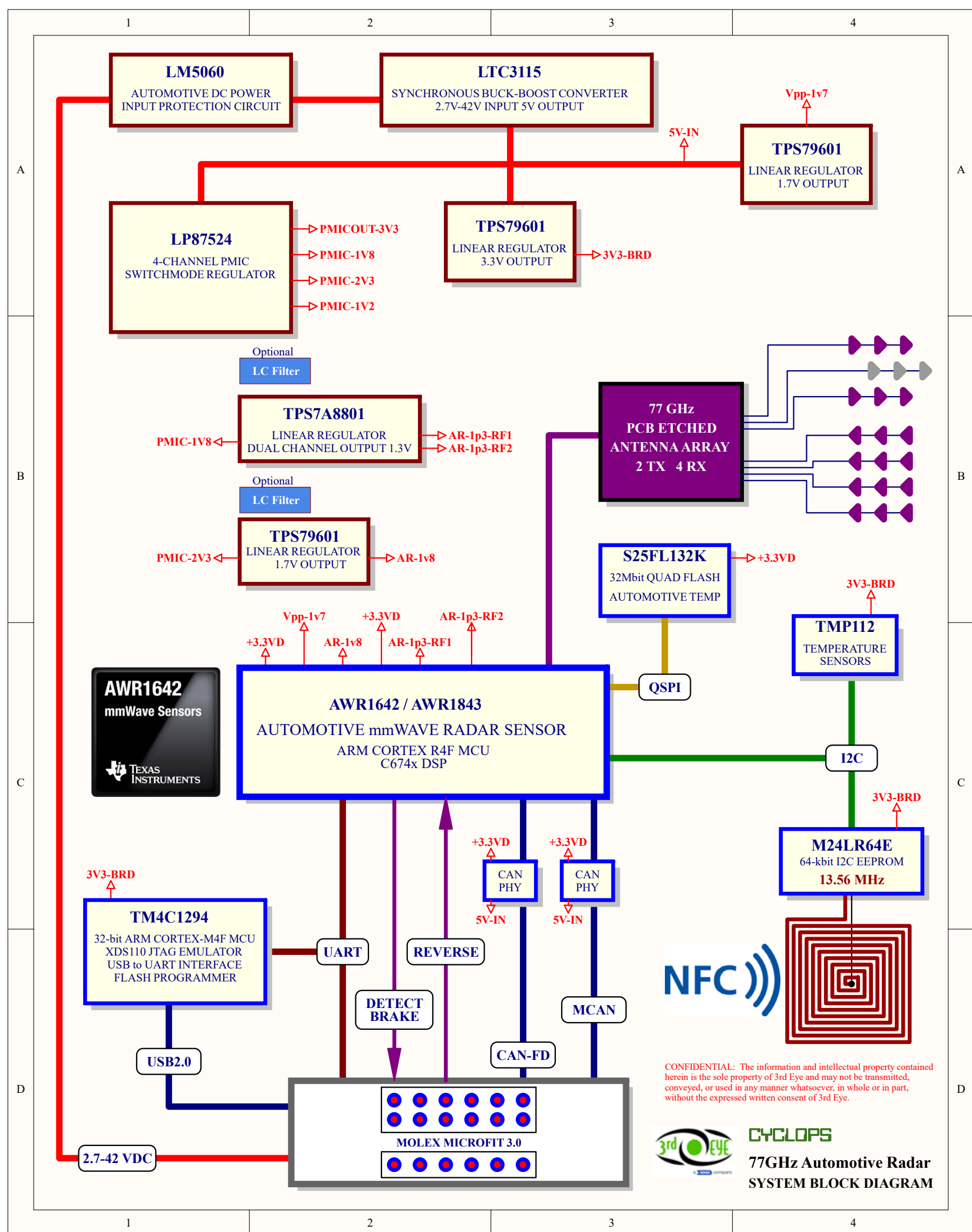
- Some devices have thermal pads, and usually the manufacturer designates this as the highest pad number. Example is IC16, the thermal pad is 17 in literature. In this design all thermal pads' PCB footprint and schematic symbol is redesignated as "Pin 0" in order to easily create, track, filter, and exclude violations in via-pad clearance rules in the PCB design rules construct as thermal pads typically have vias embedded in them for thermal performance.
- mmWave RADAR PMIC (IC2, MP87524) power-on configuration straps read using pullups to net 5V-IN as this power domain is active prior to LP87524 outputs turning on.
- Some devices have thermal pads, and usually the manufacturer designates this as the highest pad number. Example is IC16, the thermal pad is 17 in literature. I change the thermal pads' PCB footprint and schematic symbol from whatever it is to "Pin 0" in order to easily create, track, and exclude violations in via-pad clearance rules in the PCB design rules construct as thermal pads typically have vias embedded in them for thermal performance.
- mmWave RADAR PMIC (IC2, MP87524) power-on configuration straps read using pullups to net 5V-IN as this power domain is active prior to LP87524 outputs turning on.
- The 3.3V output from the PMIC is use as PGOOD for the XDS110 Supply enable, not the actual PGOOD pin.
- Final optimal values for passives calculated at fab release check, values such as resistive dividers for analog voltage sensing not calculated for optional internal buffer which has 1.4V range, not 1.8. Existing values are placeholders to get resistors into design.

- U_System Block
System Block.SchDoc
- U_AWR1642 Signal
AWR1642 Signal.SchDoc
- U_Automotive Front End
Automotive Front End.SchDoc
- U_AWR1642 Power
AWR1642 Power.SchDoc
- U_Buck Boost Vreg
Buck Boost Vreg.SchDoc
- U_XDS110 Interface
XDS110 Interface.SchDoc
- U_mmWave RADAR PMIC
mmWave RADAR PMIC.SchDoc
- U_Vehicle Interface
Vehicle Interface.SchDoc
- U_Local Power Supplies
Local Power Supplies.SchDoc

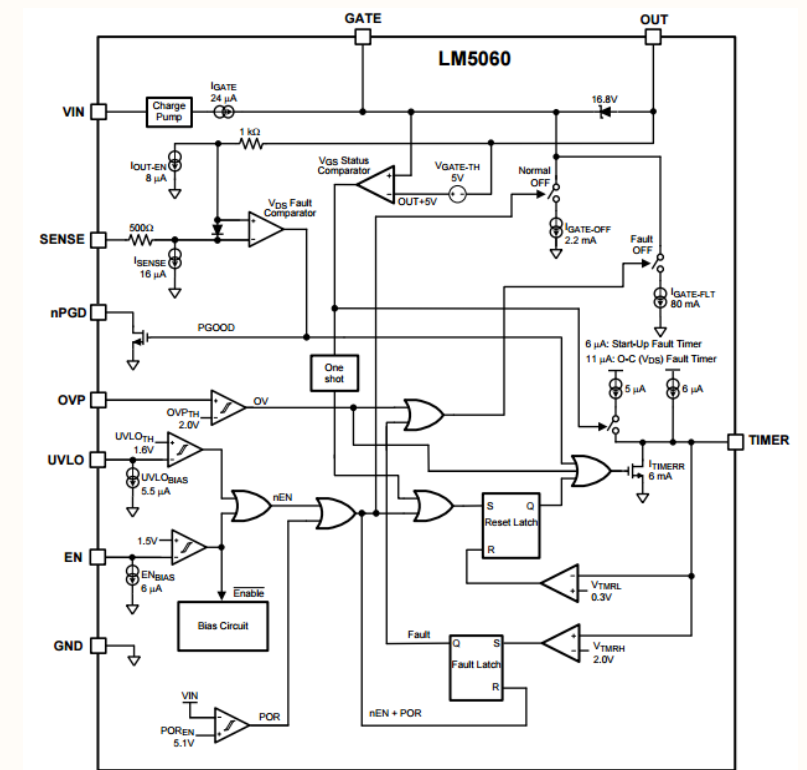
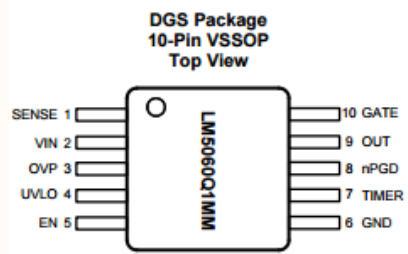
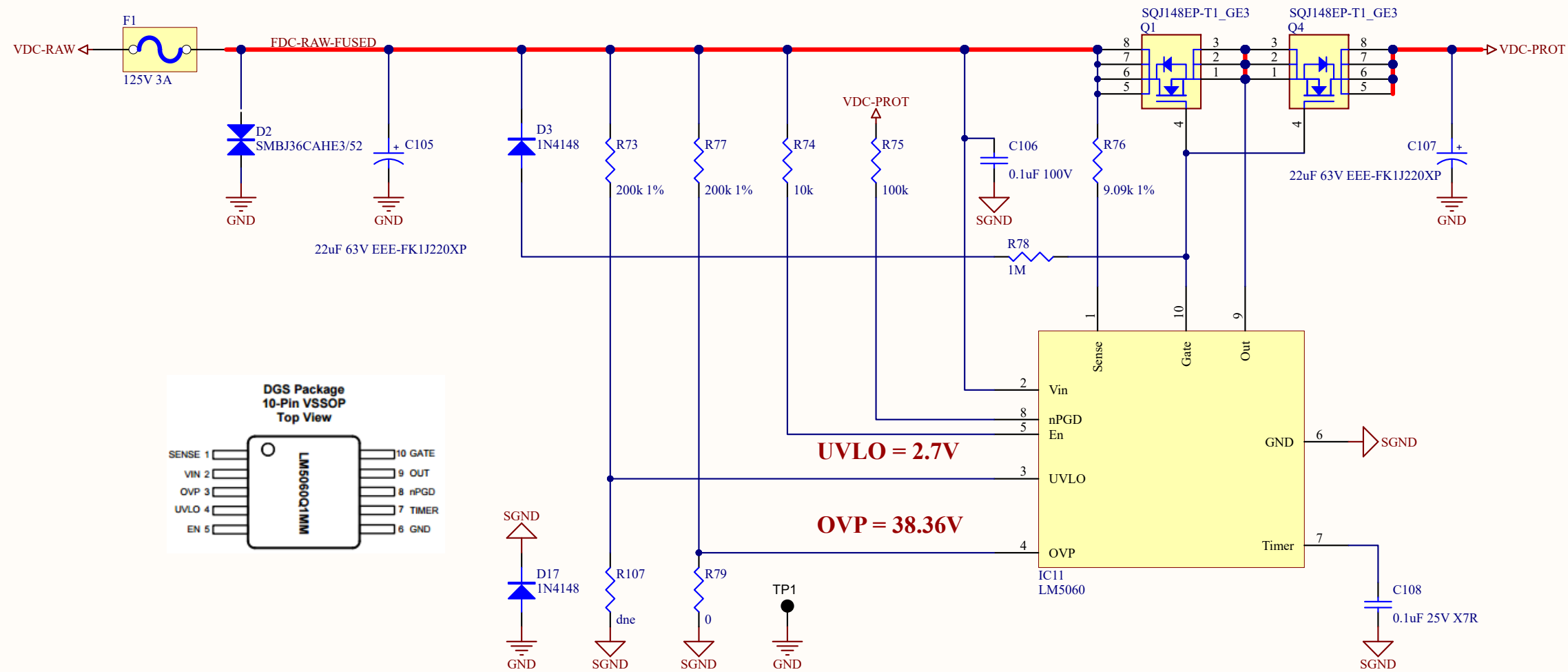


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Title CYCLOPS 77GHz Automotive RADAR		
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File: C:\Users\... \Cyclops.SchDoc	Drawn By:	John W. Whittaker

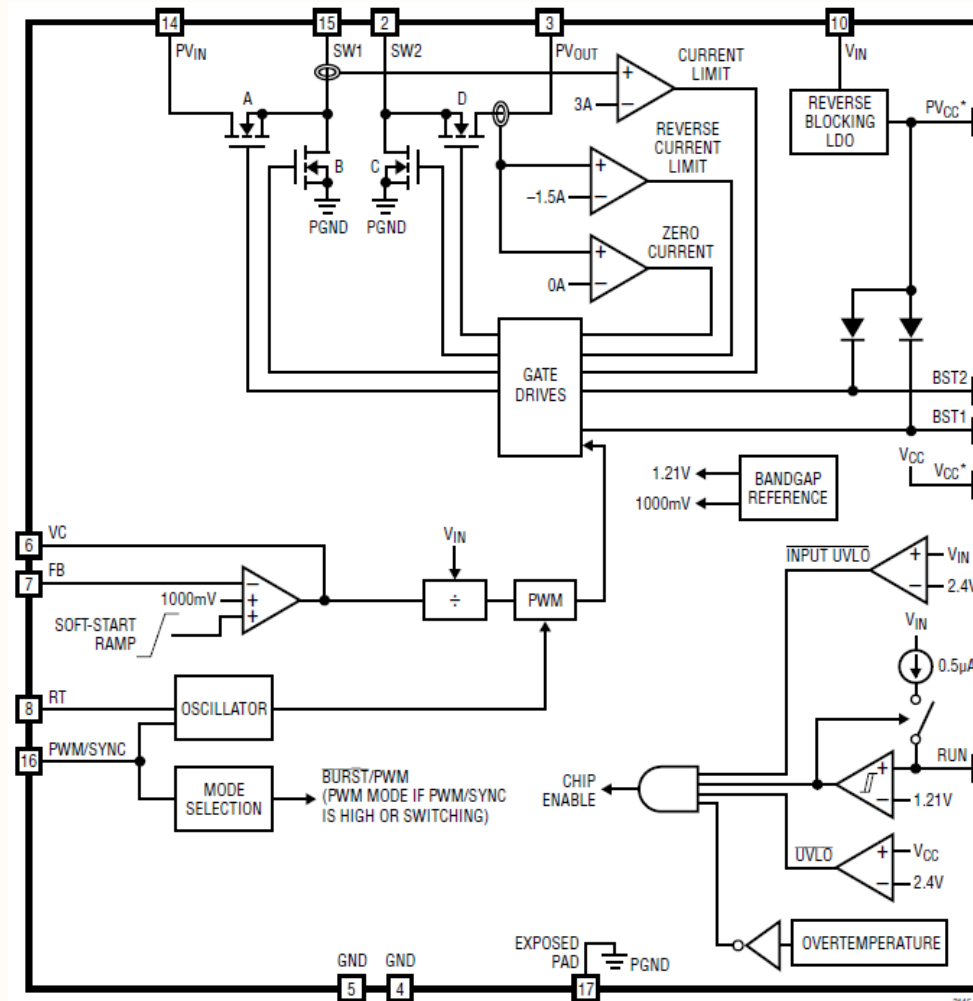
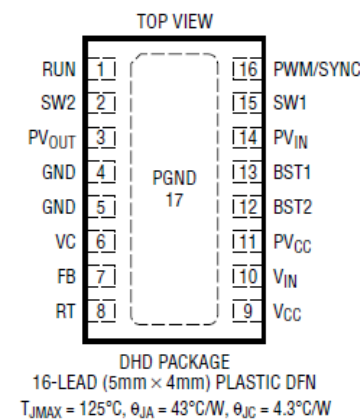
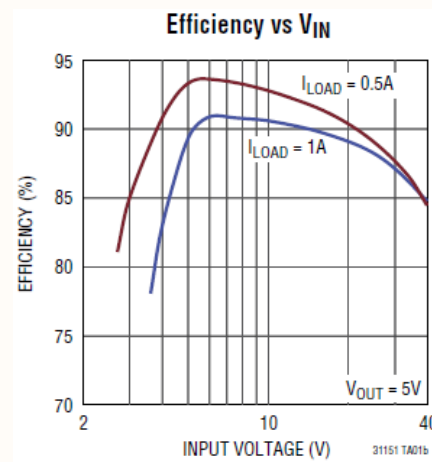
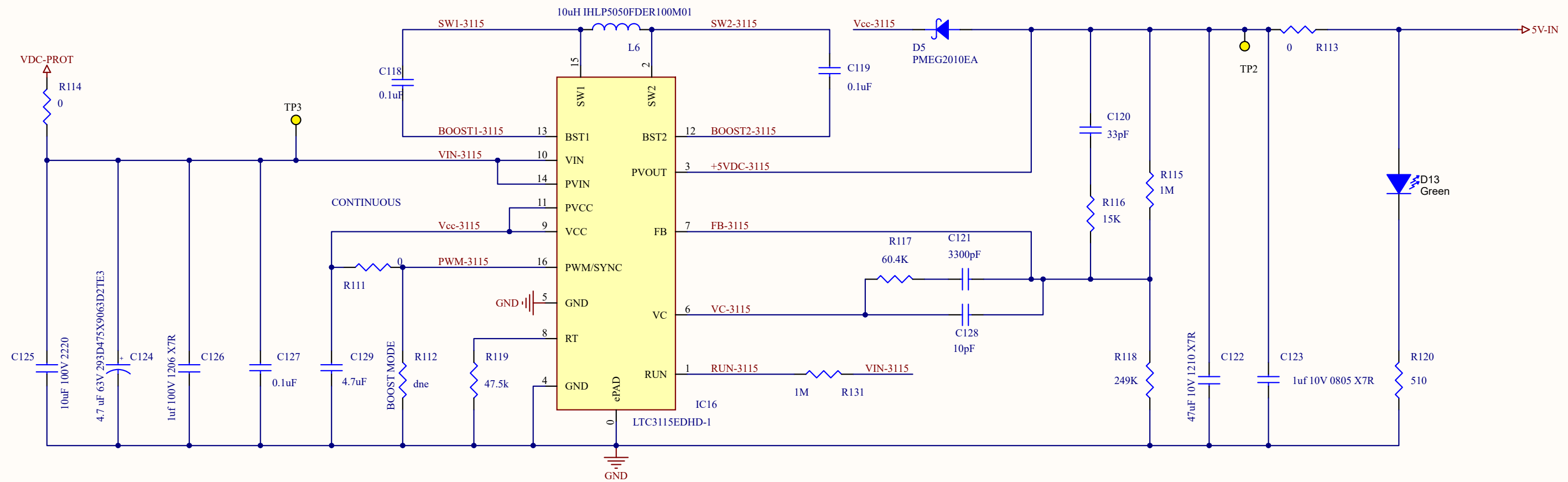


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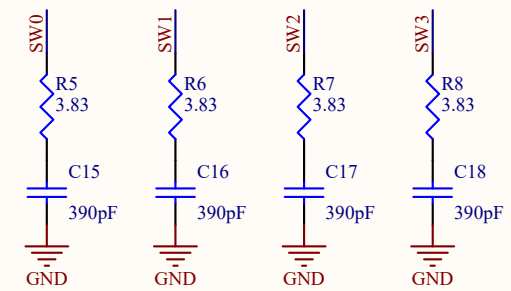
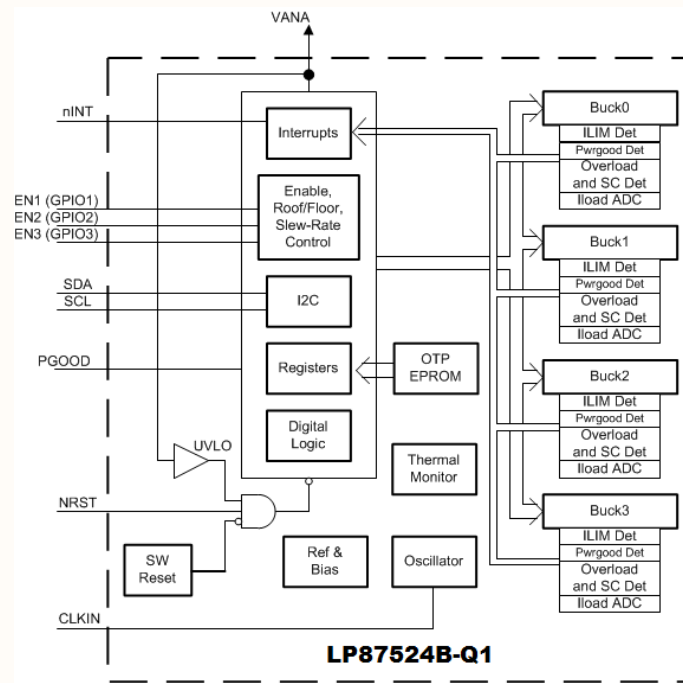
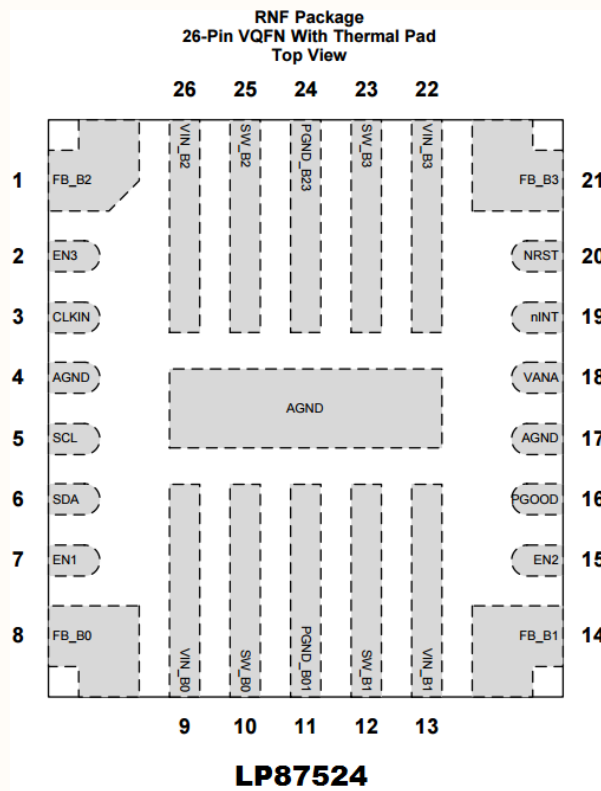
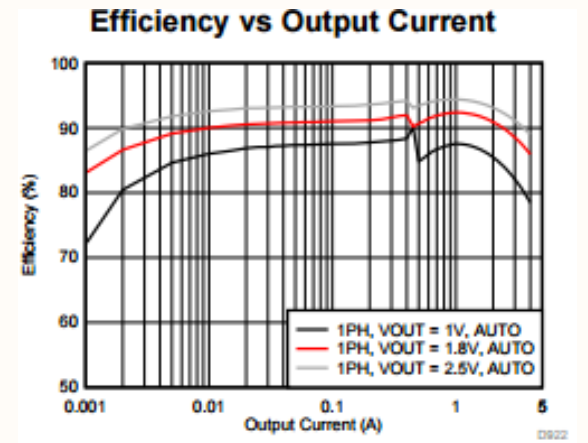
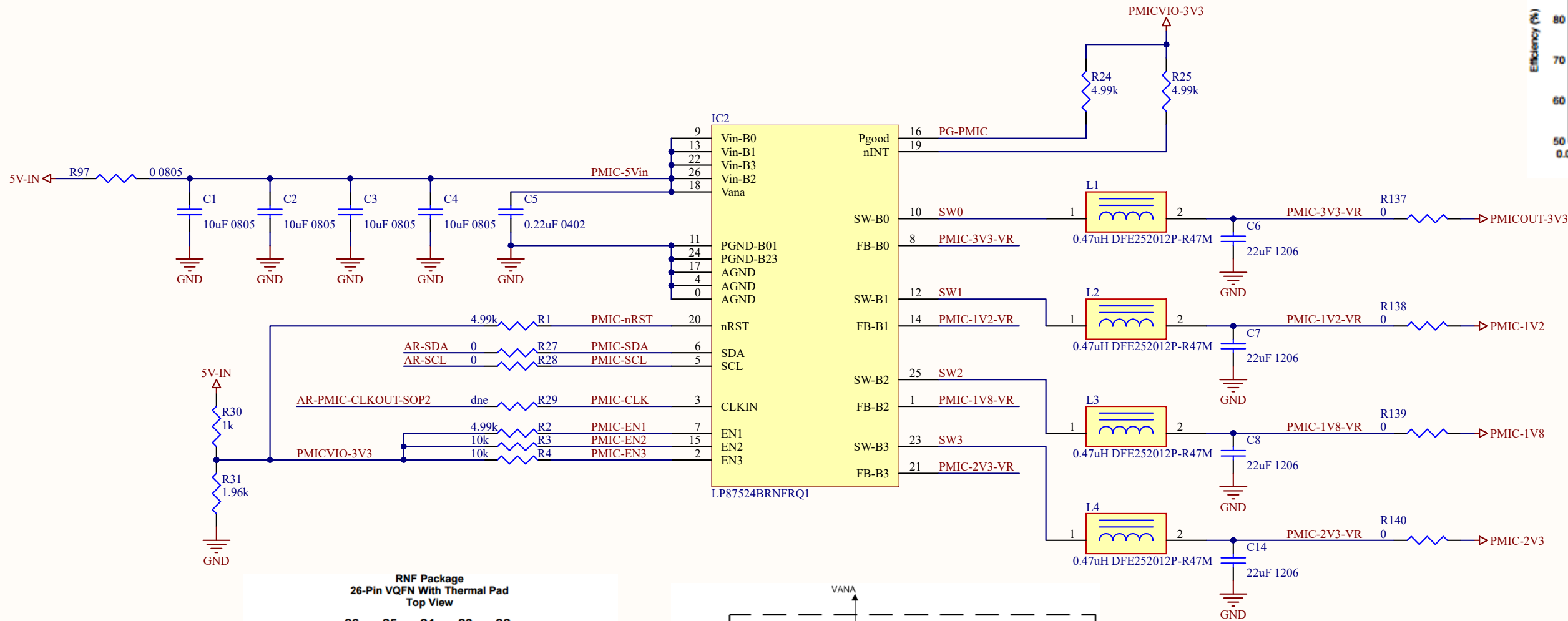
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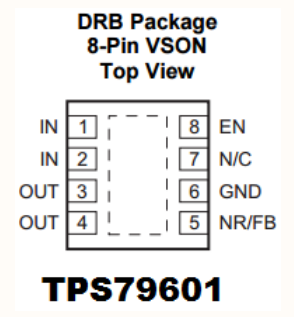
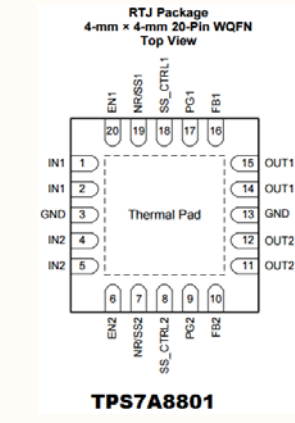
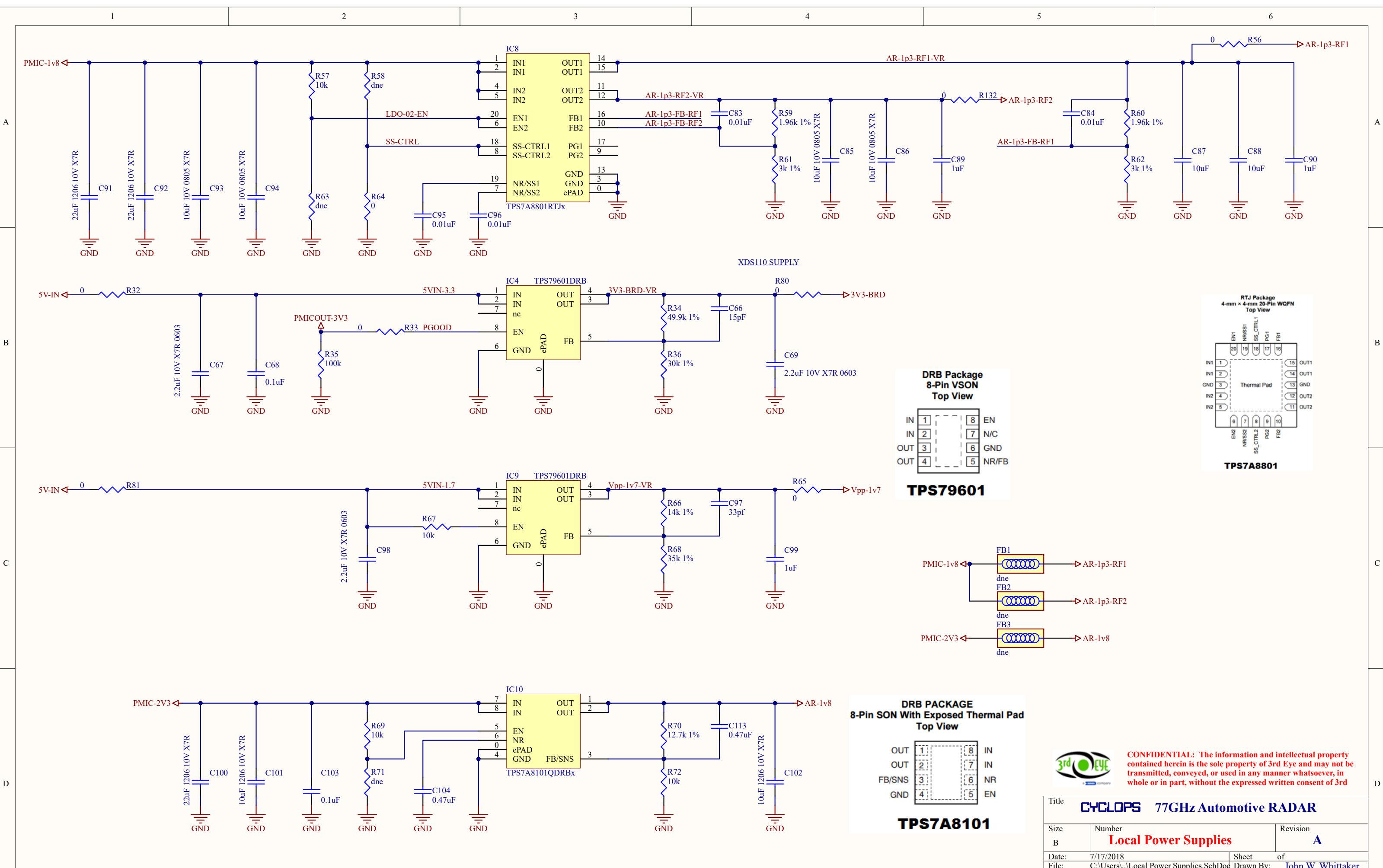
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Date: 7/17/2018	Sheet of	Drawn By: John W. Whittaker
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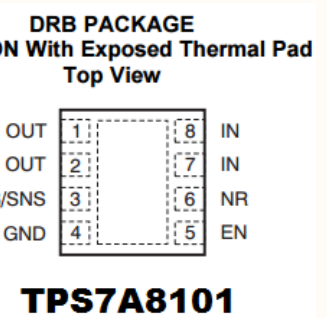


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Size	Number	Revision
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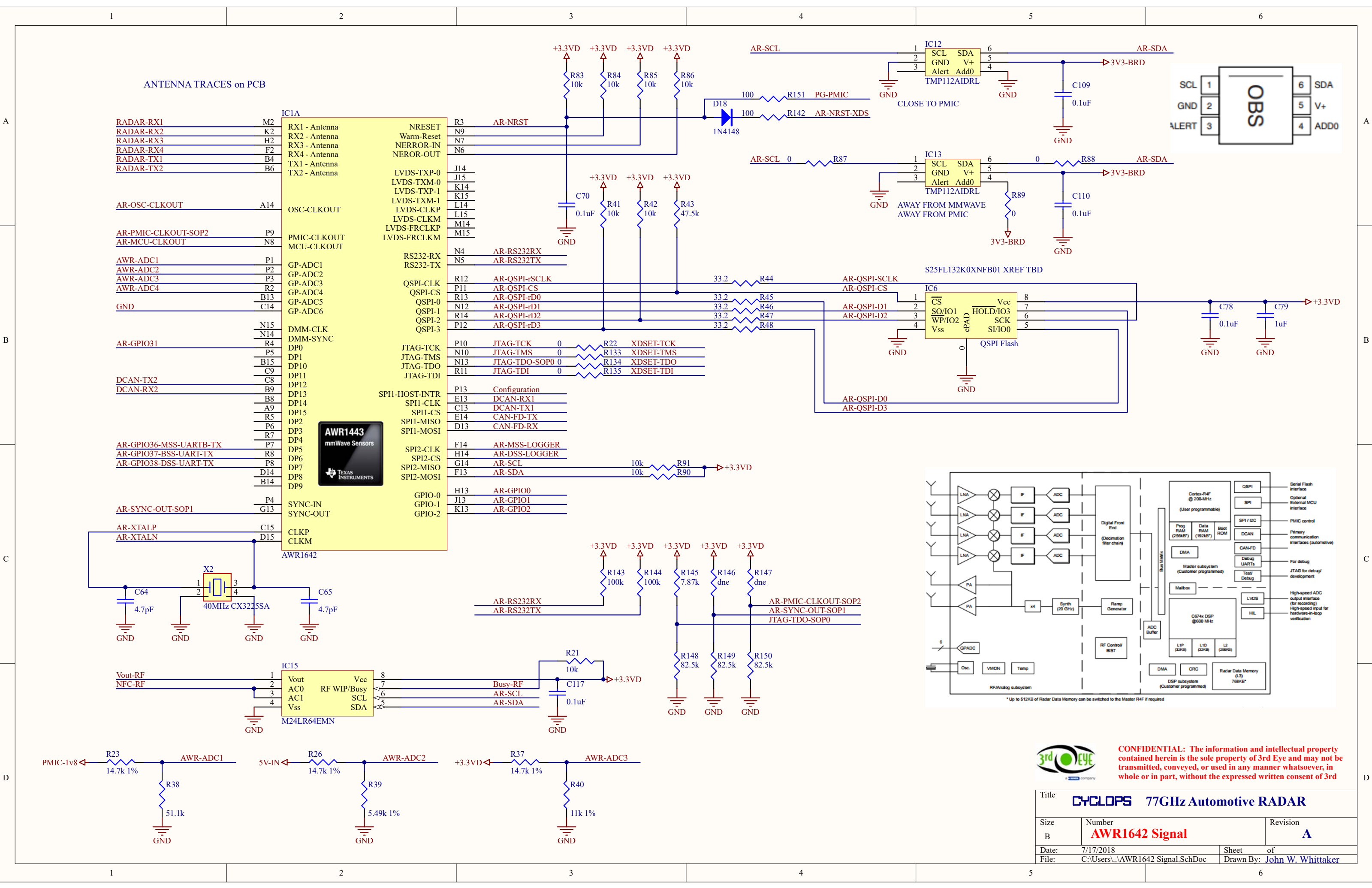
TPS79601



TPS7A8101

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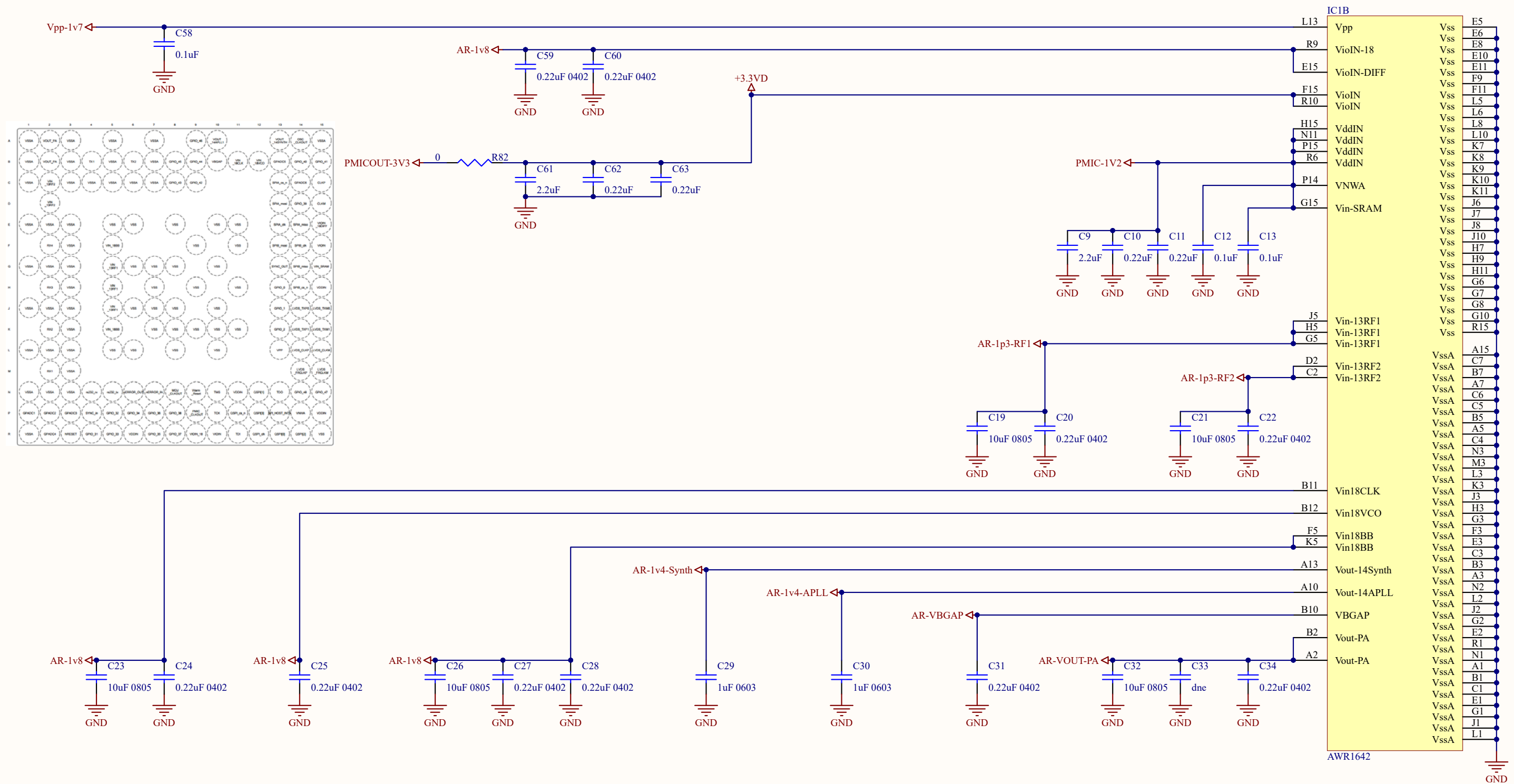
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Size B	Number Local Power Supplies	Revision A
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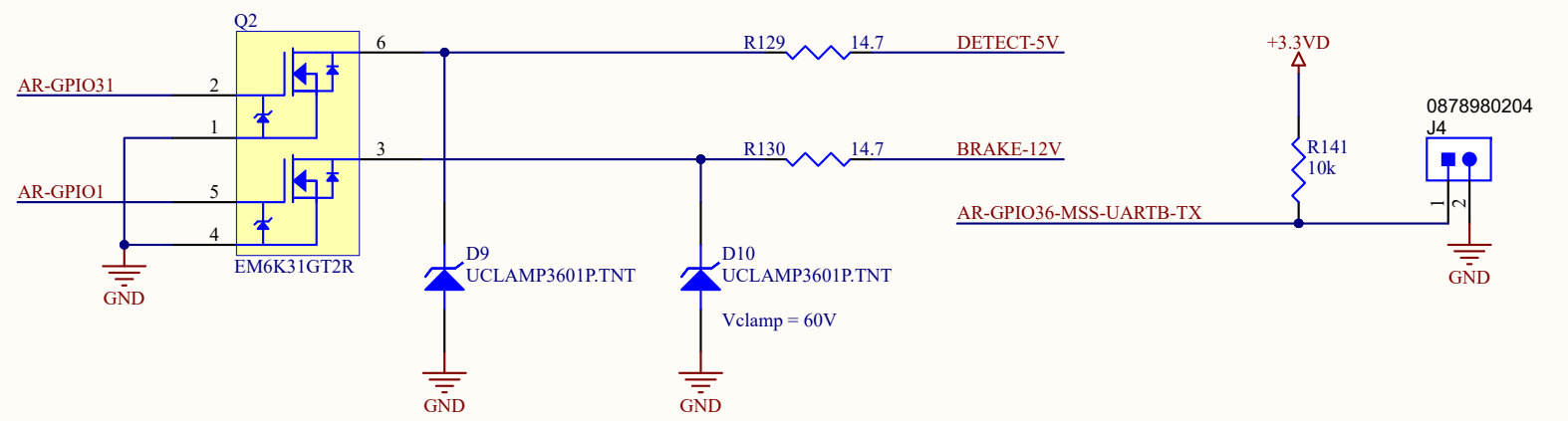
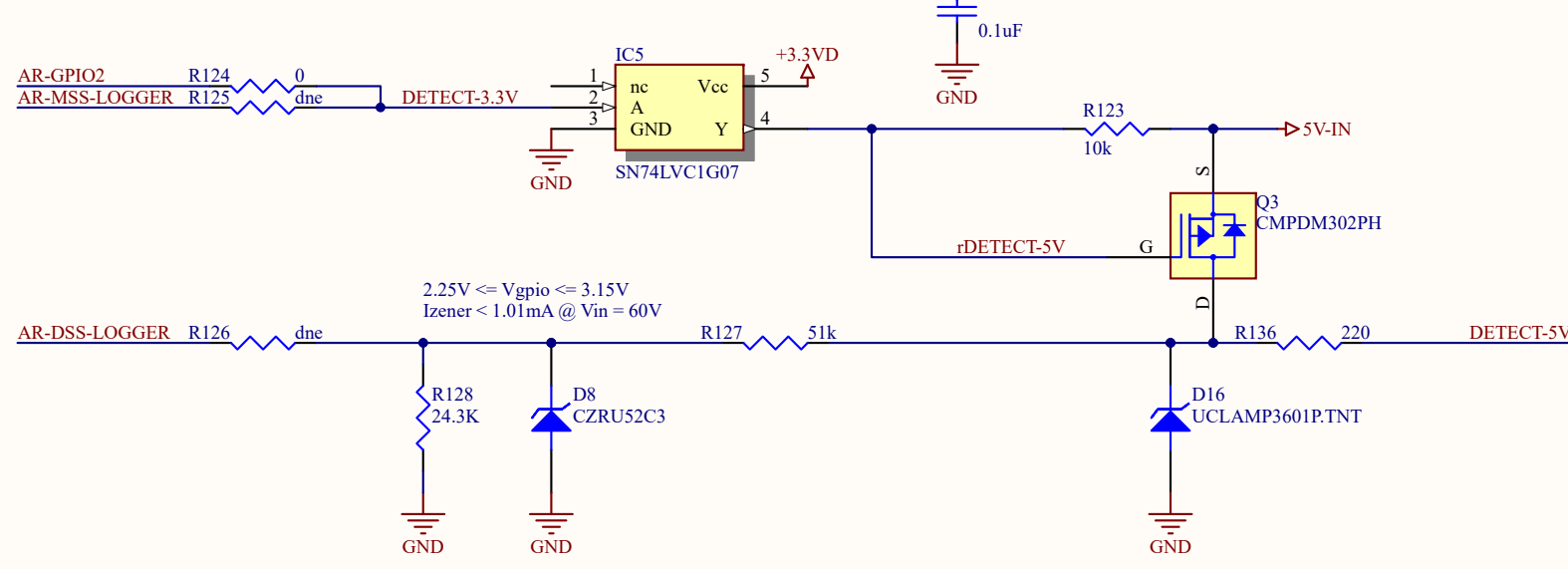
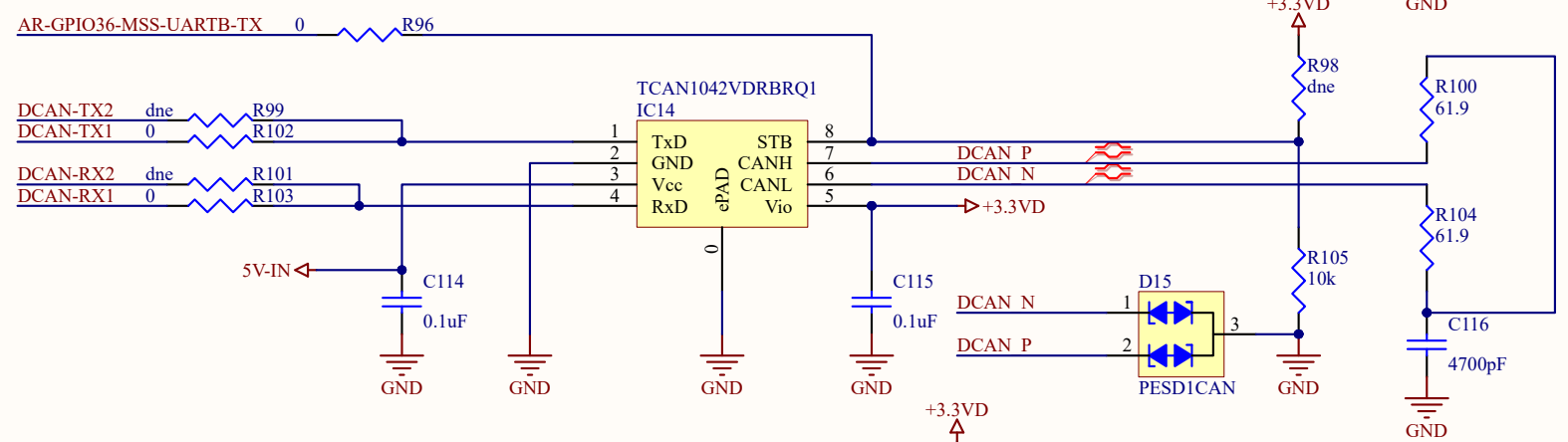
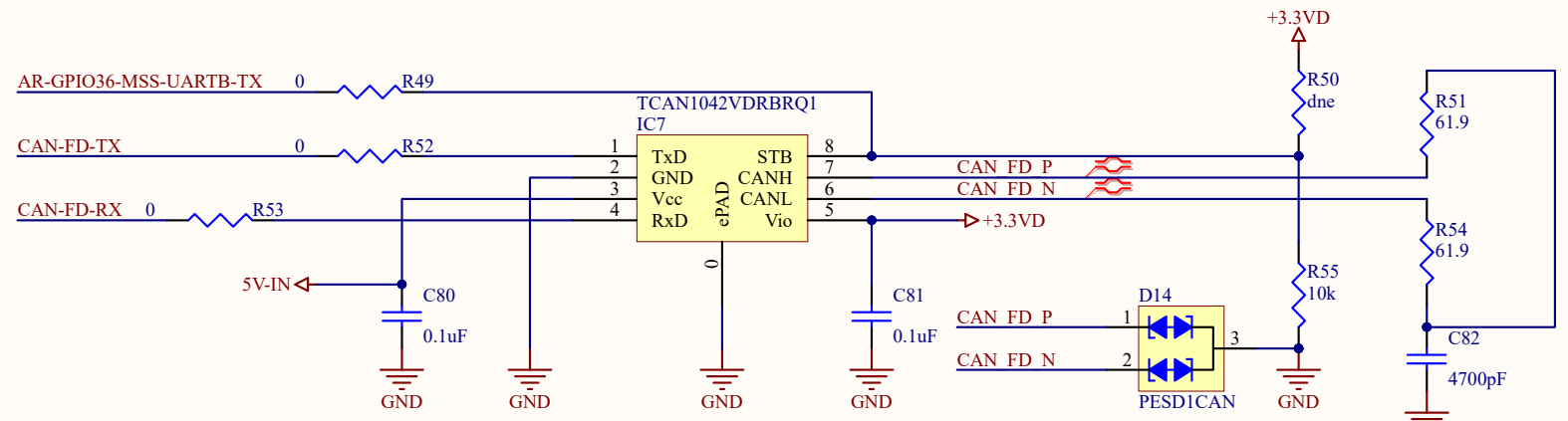
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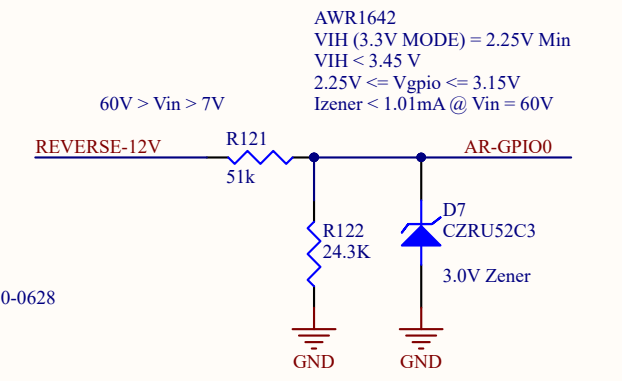
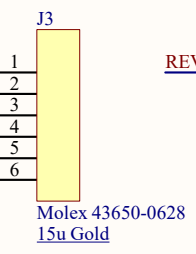


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Size	Number	Revision
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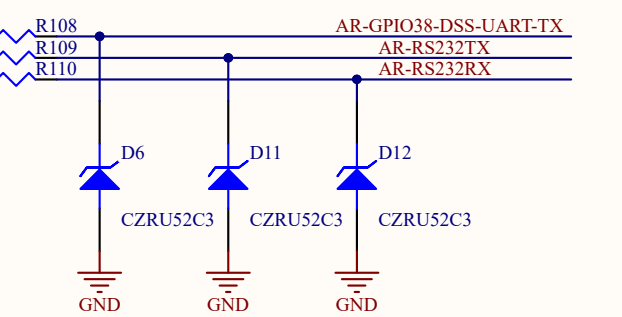


XDSET-1-VBUS	1
XDSET-1-D N	2
XDSET-1-D P	3
XDSET-1-ID	4
GND	5
AR-GPIO37-BSS-UART-TX	6

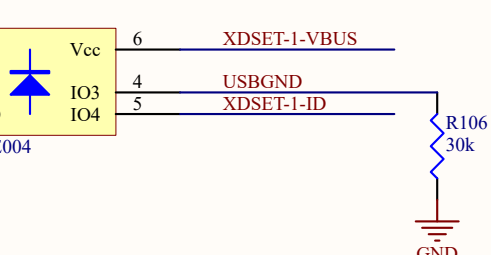


DCAN P	1	12	12	VDC-RAW
DCAN N	2	11	11	GND
AR-RS232TX-3V	3	10	10	DETECT-5V
AR-RS232RX-3V	4	9	9	BRAKE-12V
CAN FD N	5	8	8	REVERSE-12V
CAN FD P	6	7	7	DSS-UART-TX-3V

DSS-UART-TX-3V	51k	R108
AR-RS232TX-3V	51k	R109
AR-RS232RX-3V	51k	R110

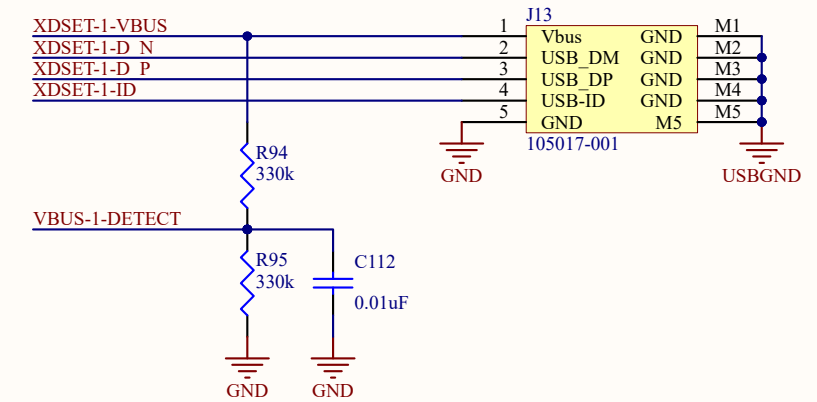
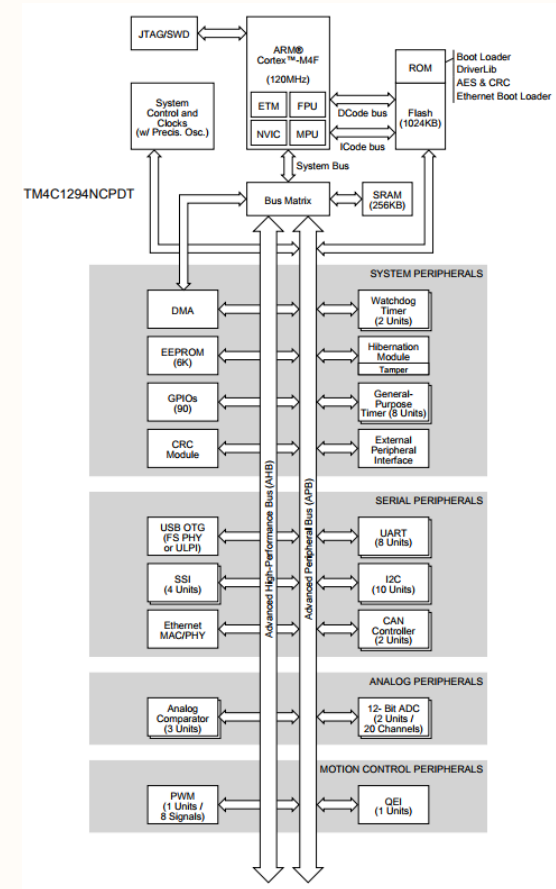
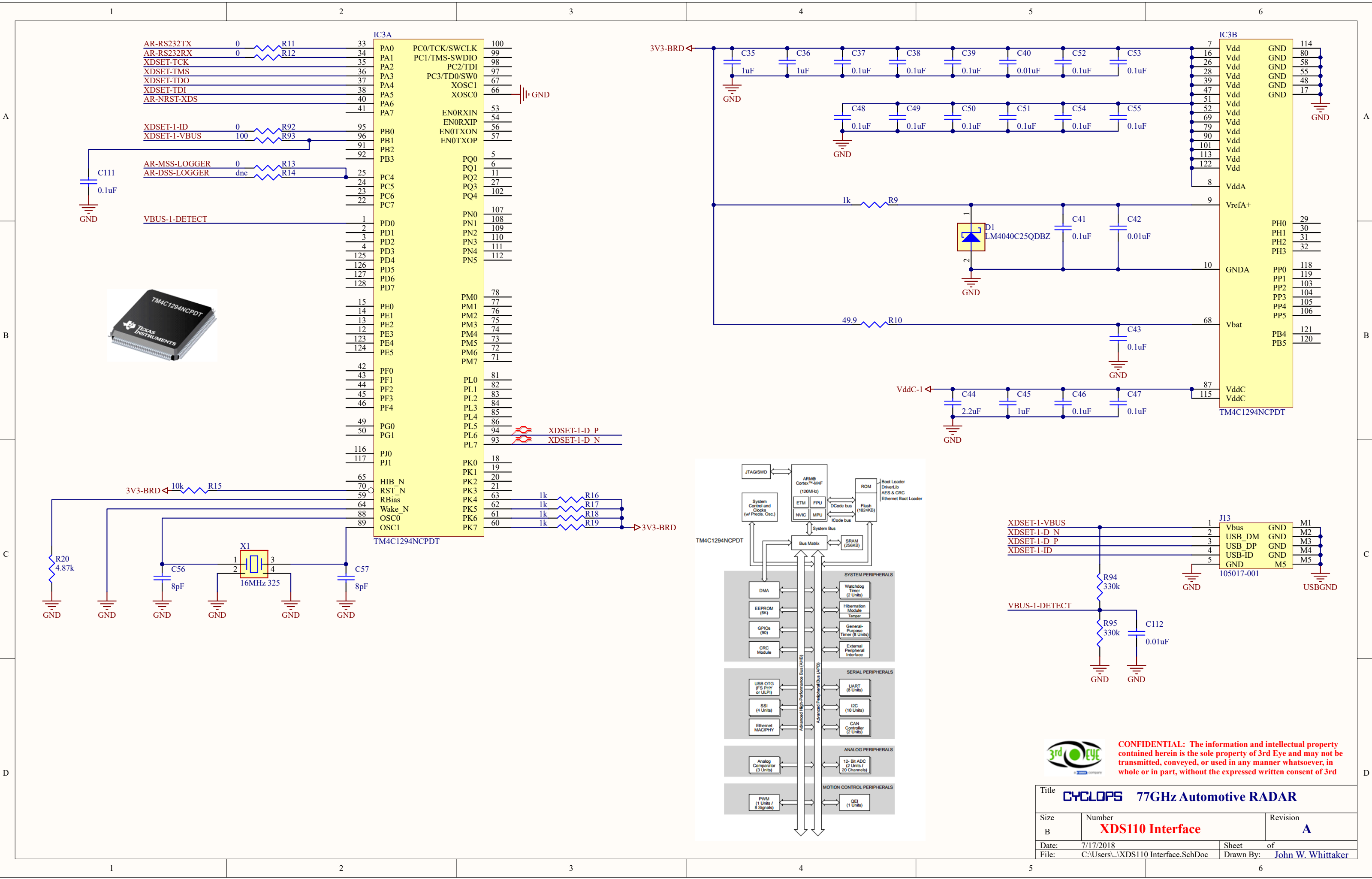


XDSET-1-D N	1
XDSET-1-D P	2
GND	3
IO1	4
IO2	5
IO3	6
IO4	7



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B	Vehicle Interface	A
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B	XDS110 Interface	A
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