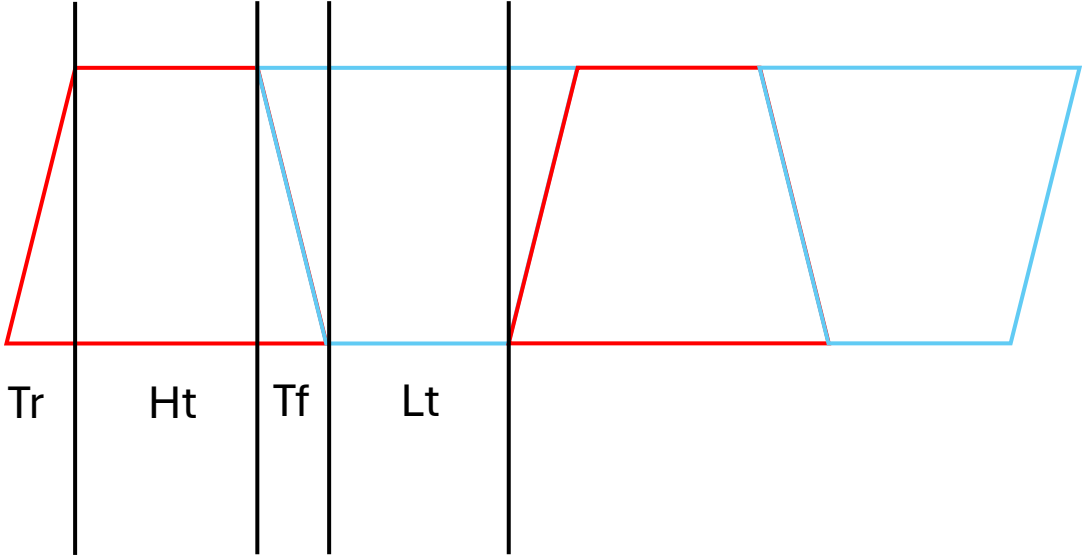
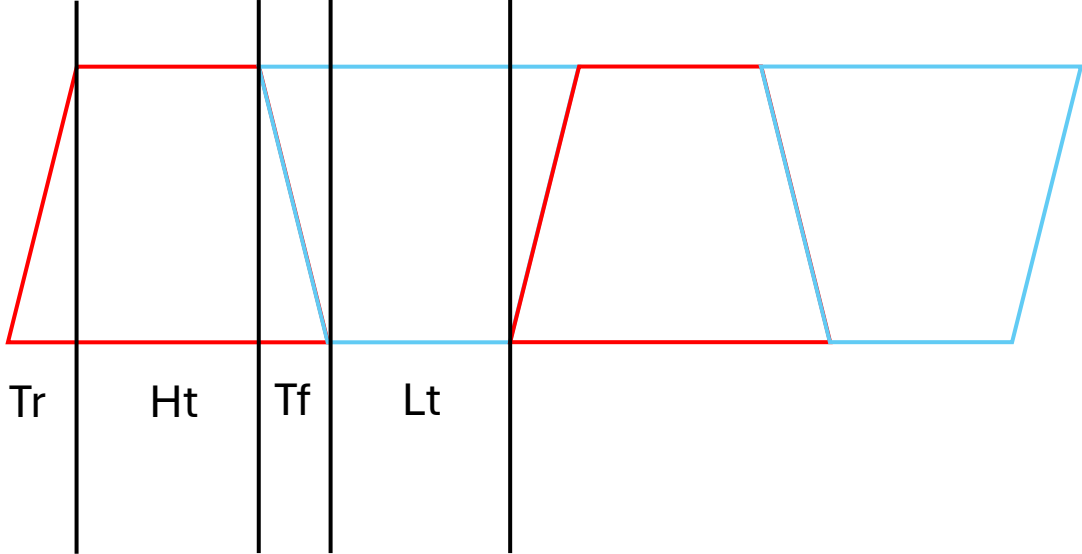


IWRL6432 supports external square wave clock



Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	High: 1.6~1.95	1kHz: -132dBc/Hz
Tr: 2~3	Low: 0~0.2	10kHz: -143dBc/Hz
Tf: 2~3	Tol: -+200ppm	100kHz: -152dBc/Hz
Ht: 8.75	Duty:35~65%	1MHz: -153dBc/Hz
Lt: 8.75		CL: 4.7~12pF

MC2016K40.0000C16ESH



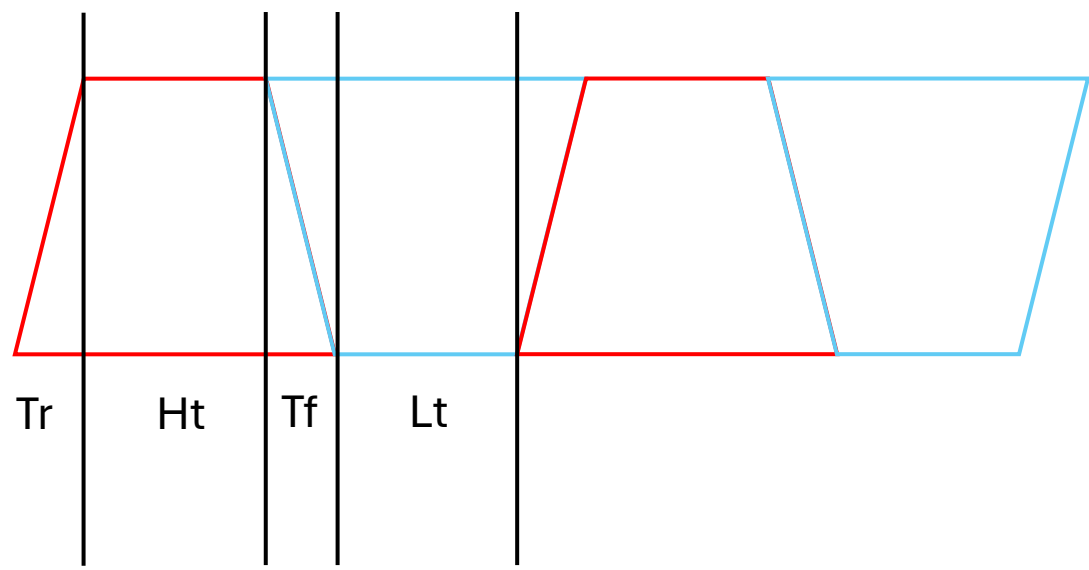
MC2016K40.0000C16ESH

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	Vcc: 1.6~3.63	1kHz: ----dBc/Hz
Tr: 6	High: 0.9*Vcc	10kHz: ----dBc/Hz
Tf: 6	Low: 0.1*Vcc	100kHz: ----dBc/Hz
Ht: 6.5	Tol: -50~50ppm	1MHz: ----dBc/Hz
Lt: 6.5	Duty: 45 ~55%	CL: 15pF

IWRL6432

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	High: 1.6~1.95	1kHz: -132dBc/Hz
Tr: 2~3	Low: 0~0.2	10kHz: -143dBc/Hz
Tf: 2~3	Tol: -+200ppm	100kHz: -152dBc/Hz
Ht: 8.75	Duty:35~65%	1MHz: -153dBc/Hz
Lt: 8.75		CL: 4.7~12pF

ASA2-40.000MHZ-L-T



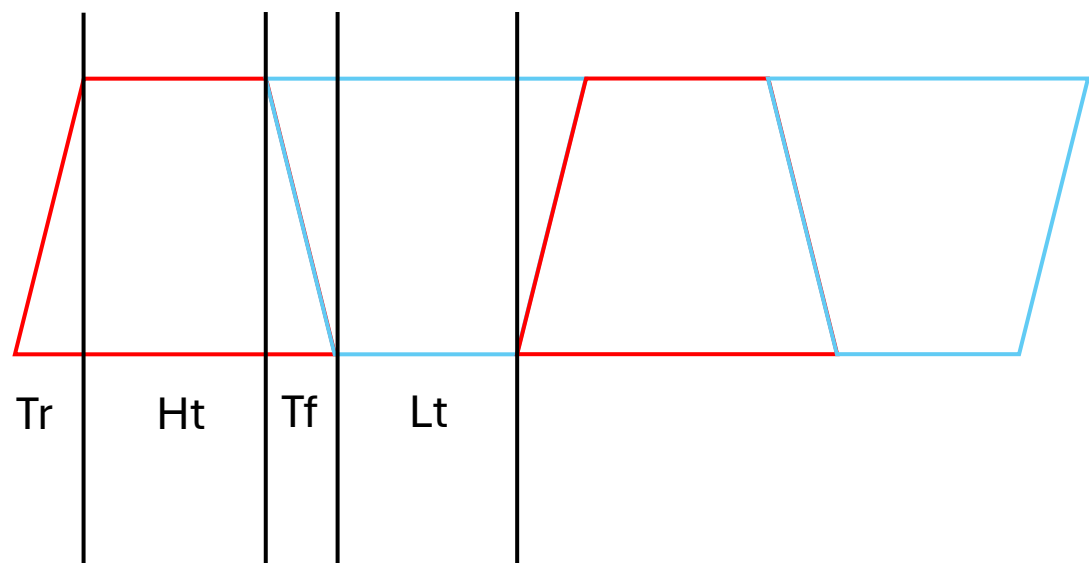
ASA2-40.000MHZ-L-T

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	Vcc: 1.62~1.98	1kHz: ----dBc/Hz
Tr: 10	High: 0.9*Vcc	10kHz: ----dBc/Hz
Tf: 10	Low: 0.1*Vcc	100kHz: ----dBc/Hz
Ht: 2.5	Tol: -50~50ppm	1MHz: ----dBc/Hz
Lt: 2.5	Duty: 45 ~55%	CL: 15pF

IWRL6432

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	High: 1.6~1.95	1kHz: -132dBc/Hz
Tr: 2~3	Low: 0~0.2	10kHz: -143dBc/Hz
Tf: 2~3	Tol: -+200ppm	100kHz: -152dBc/Hz
Ht: 8.75	Duty:35~65%	1MHz: -153dBc/Hz
Lt: 8.75		CL: 4.7~12pF

SG-210STF 40.0000ML0



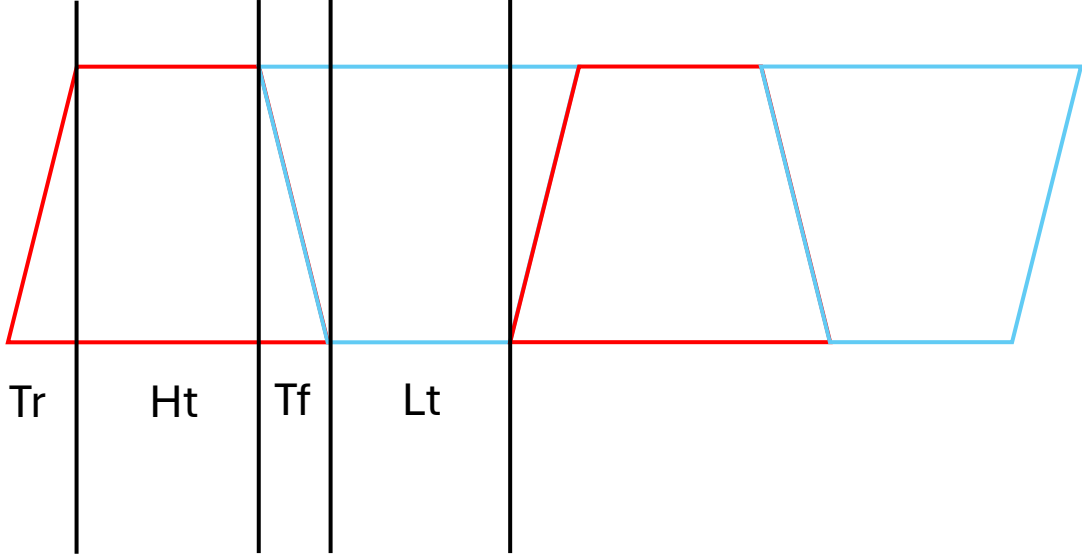
SG-210STF 40.0000ML0

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	Vcc: 1.6~3.63	1kHz: ----dBc/Hz
Tr: 3.5	High: 0.9*Vcc	10kHz: ----dBc/Hz
Tf: 3.5	Low: 0.1*Vcc	100kHz: ----dBc/Hz
Ht: 9	Tol: -50~50ppm	1MHz: ----dBc/Hz
Lt: 9	Duty: 45 ~55%	CL: 15pF

IWRL6432

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	High: 1.6~1.95	1kHz: -132dBc/Hz
Tr: 2~3	Low: 0~0.2	10kHz: -143dBc/Hz
Tf: 2~3	Tol: -+200ppm	100kHz: -152dBc/Hz
Ht: 8.75	Duty:35~65%	1MHz: -153dBc/Hz
Lt: 8.75		CL: 4.7~12pF

CDC6CE040000ADLFR



PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Characteristics						
F_{out}	Output frequency		0.25	200		MHz
V_{OL}	Output low voltage	$I_{OL} = 3.6\text{mA}$, $V_{DD} = 1.8\text{V}$		0.36		V
		$I_{OL} = 5.0\text{mA}$, $V_{DD} = 2.5\text{V}$		0.5		V
		$I_{OL} = 6.6\text{mA}$, $V_{DD} = 3.3\text{V}$		0.66		V
V_{OH}	Output high voltage	$I_{OH} = 3.6\text{mA}$, $V_{DD} = 1.8\text{V}$	$V_{DD} + 0.93$			V
		$I_{OH} = 5.0\text{mA}$, $V_{DD} = 2.5\text{V}$	$V_{DD} + 0.85$			V
		$I_{OH} = 6.6\text{mA}$, $V_{DD} = 3.3\text{V}$	$V_{DD} + 0.85$			V
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 2\text{pF}$, normal mode, $F_{out} = 25\text{MHz}$	0.28	0.65		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 2\text{pF}$, slow mode 1, $F_{out} = 25\text{MHz}$	0.42	0.75		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 5\text{pF}$, normal mode, $F_{out} = 25\text{MHz}$	0.33	0.8		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 5\text{pF}$, slow mode 2, $F_{out} = 25\text{MHz}$	1.11	2.0		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 10\text{pF}$, normal mode, $F_{out} = 25\text{MHz}$	0.44	1.7		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 10\text{pF}$, slow mode 3, $F_{out} = 25\text{MHz}$	1.85	3.1		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 15\text{pF}$, normal mode, $F_{out} = 25\text{MHz}$	0.87	2.2		ns
$t_{r/f}$	Output rise/fall time	20% to 80% of $V_{OH} - V_{OL}$, $C_L = 15\text{pF}$, slow mode 4, $F_{out} = 25\text{MHz}$	2.7	4.0		ns
$t_{r/f}$	Output rise/fall time	10% to 90% of $V_{OH} - V_{OL}$, no load, normal mode, $F_{out} = 25\text{MHz}$	0.42			ns
$t_{r/f}$	Output rise/fall time	10% to 90% of $V_{OH} - V_{OL}$, $C_L = 15\text{pF}$, normal mode, $F_{out} = 25\text{MHz}$	2.05			ns
$t_{r/f}$	Output rise/fall time	10% to 90% of $V_{OH} - V_{OL}$, $C_L = 15\text{pF}$, slow mode 4, $F_{out} = 25\text{MHz}$	3.81			ns
ODC	Output duty cycle		45	50	55	%
P_{N_Floor}	Output phase noise floor ($f_{offset} > 10\text{MHz}$)	$F_{out} = 50\text{MHz}$	-155			dBc/Hz
C_L	Maximum capacitive load	$F_{out} = 50\text{MHz}$	30			pF
C_L	Maximum capacitive load	$F_{out} = 50\text{MHz}$	15			pF
R_{out_high}	Output impedance		50			Ω
Function Pin Characteristics (OE/ST)						
V_{IL}	Input low voltage	$V_{DD} = 1.8\text{V}$	0.45			V
		$V_{DD} = 2.5\text{V}$	0.475			V
		$V_{DD} = 3.3\text{V}$	0.5			V
V_{IH}	Input high voltage		1.3			V
I_{IL}	Input low current	EN = GND	-70			μA
I_{IH}	Input high current	EN = VDD	40			μA
C_{in}	Input capacitance ⁽¹⁾		2			pF
Frequency Tolerance						

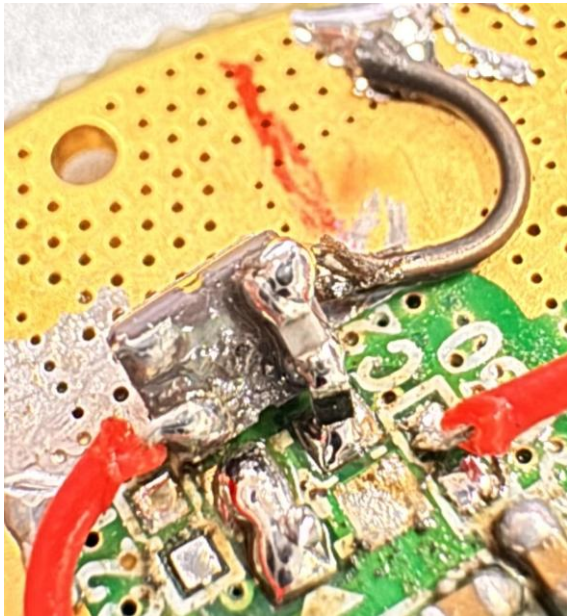
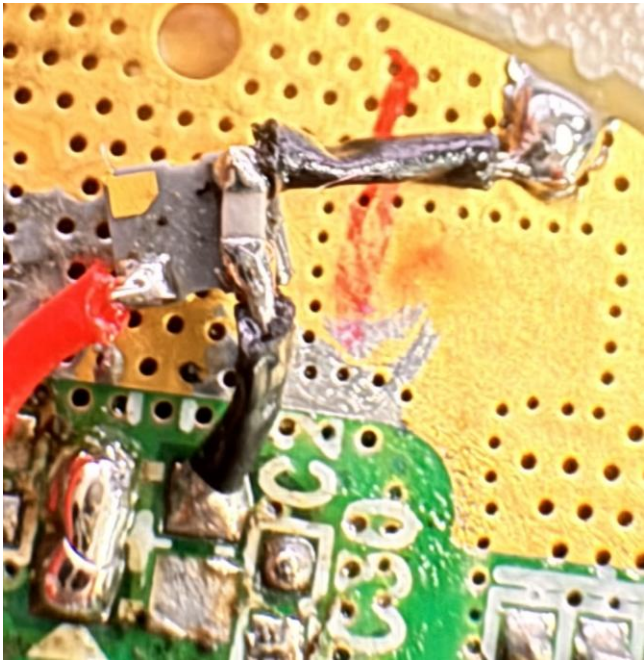
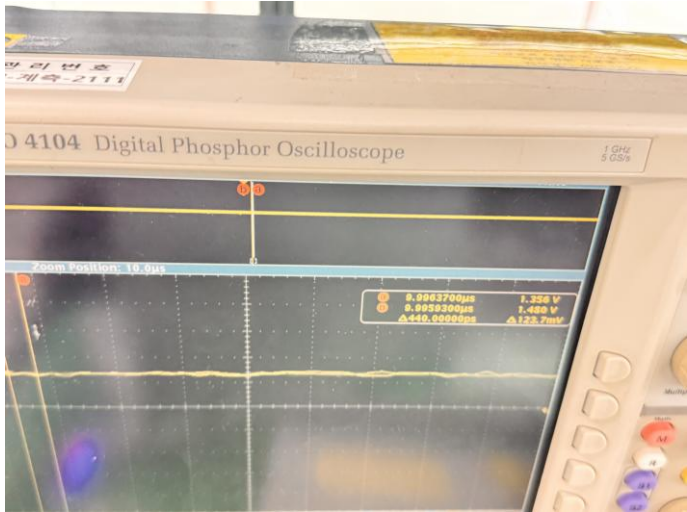
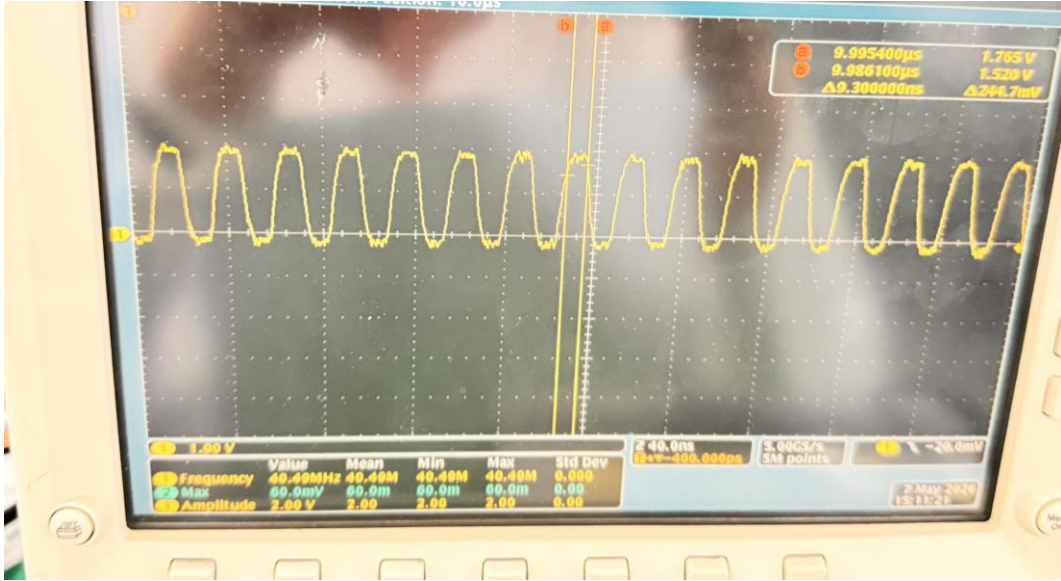
CDC6CE040000ADLFR

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	Vcc: -1.62~3.63	1kHz: -86dBc/Hz
Tr: 2.05	High: 0.88*Vcc	10kHz: -120dBc/Hz
Tf: 2.05	Low: 0.36	100kHz: -138dBc/Hz
Ht: 10.4	Tol: -25~25ppm	1MHz: -143dBc/Hz
Lt: 10.4	Duty: 45 ~55%	CL: 15pF

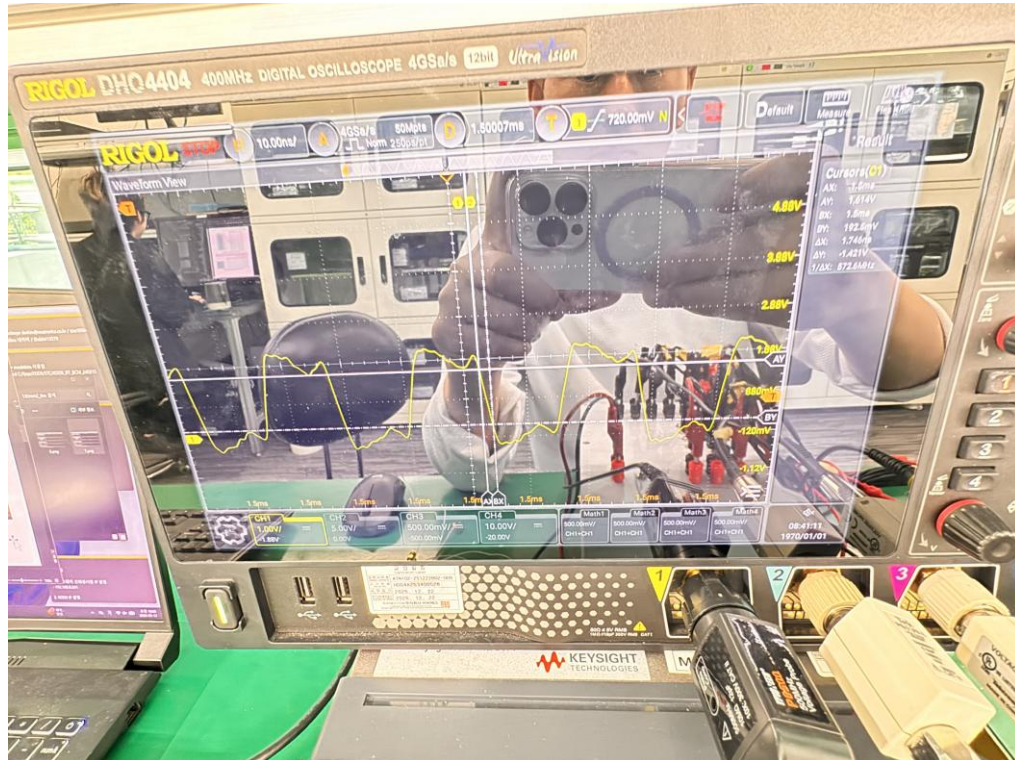
IWRL6432

Clock time (ns)	Voltage (V)	Phase noise
40MHz=25	High: 1.6~1.95	1kHz: -132dBc/Hz
Tr: 2~3	Low: 0~0.2	10kHz: -143dBc/Hz
Tf: 2~3	Tol: -+200ppm	100kHz: -152dBc/Hz
Ht: 8.75	Duty: 35~65%	1MHz: -153dBc/Hz
Lt: 8.75		CL: 4.7~12pF

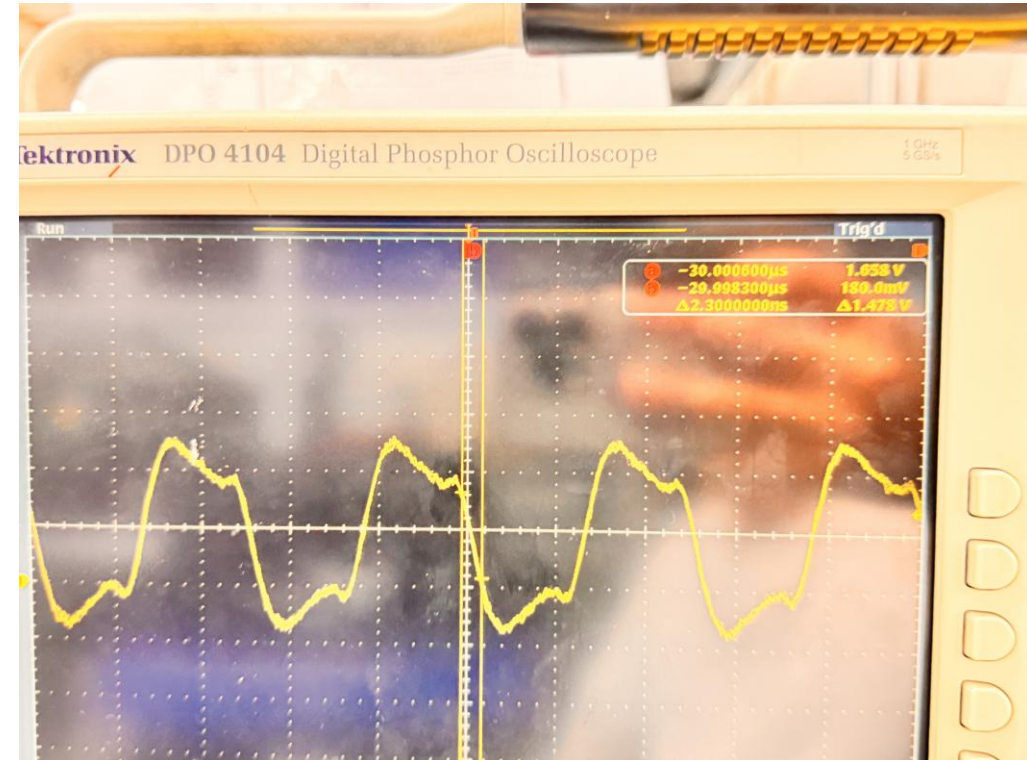
SG-210STF 40.0000MLO CL: 15p



CDC6CE040000ADLFR CL:8pF



CDC6CE040000ADLFR CL:12pF



FW4000044Q C1 and C2: 4.7pF

