Precision, High Speed, Hall-Effect Angle Sensor IC with Integrated Diagnostics for Safety-Critical Applications

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - □ Capable of sensing magnet rotational speeds targeting 12b effective resolution with 900 G field
  - □ Circular Vertical Hall (CVH) technology provides a single channel sensor system supporting operation across a wide range of air gaps
- Developed in accordance with ISO 26262:2011 requirements for hardware product development for use in safety-critical applications (pending assessment)
  - □ Single die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner proscribed in the A1333 Safety Manual
  - □ Dual die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner proscribed in the A1333 Safety Manual
- High diagnostic coverage
  - □ On-chip diagnostics include logic built-in self-test (LBIST), signal path diagnostics, and watchdogs to support safety-critical (ASIL) applications
  - □ 4-bit CRC on SPI
- On-chip EEPROM for storing factory and customer calibration parameters
  - □ Single-bit error correction, dual-bit error detection through the use of error correction control (ECC)

Continued on next page...

DESCRIPTION

The A1333 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic Circular Vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, and motor commutation (UVW) or encoder outputs (A, B, I). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration parameters. The A1333 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), rotary PRNDLs, and throttle systems.

The A1333 supports customer integration into safety-critical applications.

The A1333 is available in a dual-die 24-pin eTSSOP and a single-die 14-pin TSSOP package. The packages are lead (Pb) free with 100% matte-tin leadframe plating.

PACKAGES:

24-pin eTSSOP (Suffix LP) — Dual Independent SoCs

14-pin TSSOP (Suffix LE) — Single SoC

Not to scale

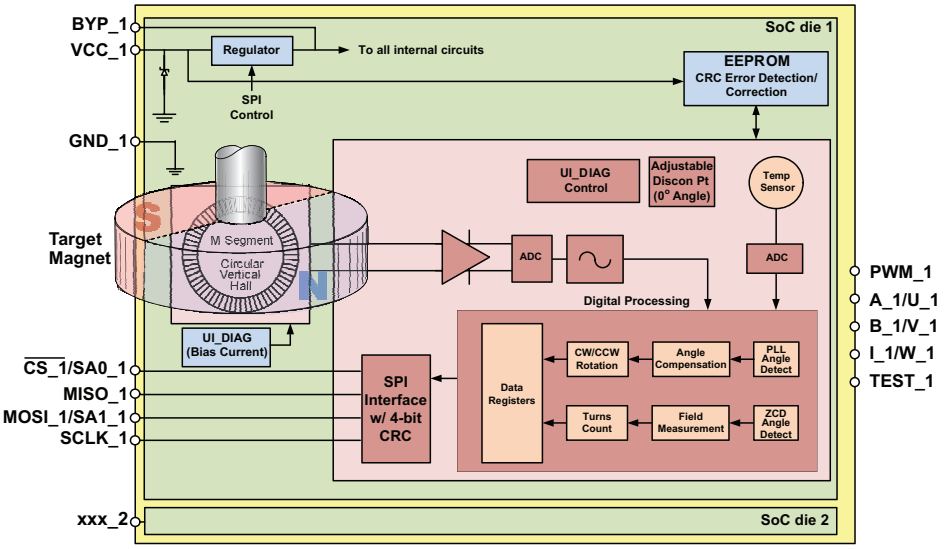


Figure 1: A1333 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Supports harsh operating conditions required for automotive and industrial applications, including direct connection to 12 V battery
  - □ Operating temperature range from –40°C to 150°C
  - □ Operating supply voltage range from 4.0 to 16.5 V
    - ♦ Can support ISO 7637-2 Pulse 5b up to 39 V
- Multiple output formats supported for ease of system integration
  - □ ABI/UVW output provides high resolution, low latency, and PWM for initial position
  - □ 10 MHz SPI for low latency angle and diagnostic information; enables multiple independent ICs to be connected to the same bus
  - □ Output resolution on ABI and UVW are selectable
- Multiple programming / configuration formats supported
  - □ The system can be completely controlled and programmed over SPI, including EEPROM writes
  - □ For system with limited pins available, writing and reading can be performed over VCC and PWM pins. This allows configuring the EEPROM in production line for a device with only ABI/UVW and PWM pins connected.
- Stacked dual die construction to improve die-to-die matching for systems that require redundant sensors
- Reduces magnet misalignment impact on die-to-die matching for a given magnet diameter, relative to “side-by-side” dual die orientation

SELECTION GUIDE

Part Number	System Die	Package	Packing	Interface Voltage
A1333LLPTR-DD-T	Dual	24-pin eTSSOP	4000 pieces per 13-in. reel	3.3 V
A1333LLETR-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	3.3 V

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature [1]	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		170	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] Maximum operational voltage is reduced at high ambient temperatures (T_A). See Operating Characteristics, footnote 2.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP-24 package	69	°C/W
		LE-14 package	82	°C/W

[2] Additional thermal information available on the Allegro website.

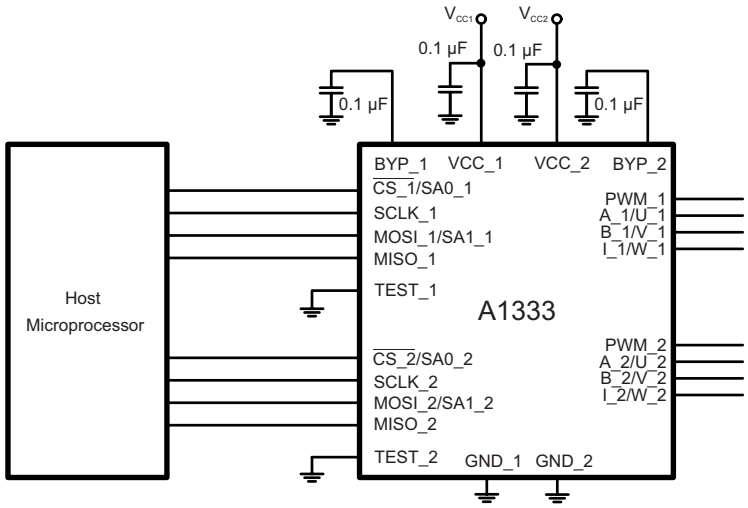


Figure 2: Typical Application Circuit

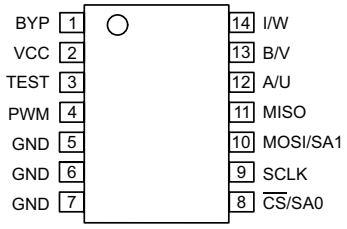
Both die are electrically separate, and may be operated simultaneously using different Power/GND sources.

Table of Contents

PINOUT DIAGRAMS AND TERMINAL LIST TABLES

Pinout Diagram

LE 14-Pin TSSOP

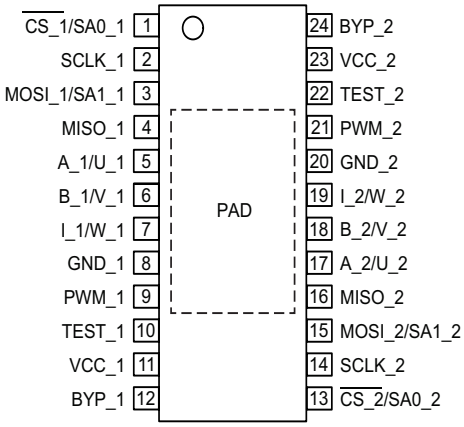


LE 14-Pin TSSOP Terminal List Table

Pin Name	Pin Number	Function
BYP	1	External bypass capacitor terminal for internal regulator
VCC	2	Power Supply / Manchester Input
TEST	3	Test pin; bring to GND
PWM	4	PWM Angle Output / Manchester Output
GND	5, 6, 7	Device ground terminal
$\overline{CS}$ /SA0	8	SPI: Chip Select terminal, active low input Manchester: LSB of ID value. Tie to BYP for “1”, GND for “0”
SCLK	9	SPI Clock terminal input
MOSI/SA1	10	SPI: Master Output, Slave Input Manchester: MSB of ID value. Tie to BYP for “1”, GND for “0”
MISO	11	SPI Master Input / Slave Output
A/U	12	Option 1: Quadrature A output signal Option 2: U (phase 1) output signal
B/V	13	Option 1: Quadrature B output signal Option 2: V (phase 2) output signal
I/W	14	Option 1: Quadrature I (index) output signal Option 2: W (phase 3) output signal

Pinout Diagram

LP 24-Pin eTSSOP



LP 24-Pin eTSSOP Terminal List Table

Pin Name	Pin Number	Function
CS_1 /SA0_1	1	SPI: Chip Select terminal, active low input (die 1) Manchester: LSB of ID value for die 1. Tie to BYP_1 for “1”, GND_1 for “0”
SCLK_1	2	SPI Clock terminal input (die 1)
MOSI_1/SA1_1	3	SPI: Master Output, Slave Input (die 1) Manchester: MSB of ID value for die 1. Tie to BYP_1 for “1”, GND_1 for “0”
MISO_1	4	SPI Master Input / Slave Output (die 1)
A_1/U_1	5	Option 1: Quadrature A output signal signal (die 1) Option 2: U (phase 1) output signal (die 1)
B_1/V_1	6	Option 1: Quadrature B output signal (die 1) Option 2: V (phase 2) output signal (die 1)
I_1/W_1	7	Option 1: Quadrature I (index) output signal (die 1) Option 2: W (phase 3) output signal (die 1)
GND_1	8	Device ground terminal (die 1)
PWM_1	9	PWM Angle Output / Manchester Output (die 1)
TEST_1	10	Test pin; bring to GND (die 1)
VCC_1	11	Power Supply / Manchester Input (die 1)
BYP_1	12	External bypass capacitor terminal for internal regulator (die 1)
CS_2/SA0_2	13	SPI: Chip Select terminal, active low input (die 2) Manchester: LSB of ID value for die 2. Tie to BYP_2 for “1”, GND_2 for “0”
SCLK_2	14	SPI Clock terminal input (die 2)
MOSI_2/SA1_2	15	SPI: Master Output, Slave Input (die 2) Manchester: MSB of ID value for die 2. Tie to BYP_2 for “1”, GND_2 for “0”
MISO_2	16	SPI Master Input / Slave Output (die 2)
A_2/U_2	17	Option 1: Quadrature A output signal (die 2) Option 2: U (phase 1) output signal (die 2)
B_2/V_2	18	Option 1: Quadrature B output signal (die 2) Option 2: V (phase 2) output signal (die 2)
I_2/W_2	19	Option 1: Quadrature I (index) output signal (die 2) Option 2: W (phase 3) output signal (die 2)
GND_2	20	Device ground terminal (die 2)
PWM_2	21	PWM Angle Output / Manchester Output (die 2)
TEST_2	22	Test pin; bring to GND (die 2)
VCC_2	23	Power Supply / Manchester Input (die 2)
BYP_2	24	External bypass capacitor terminal for internal regulator (die 2)
PAD	PAD	Exposed pad for thermal dissipation

OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Customer supply	4.0	–	16.5	V
Supply Current	I_{CC}	One die, sampling angles	–	17	19	mA
Undervoltage Flag Threshold [3]	V_{UVD}	dV/dt = 1 V/ms, A1333 sampling enabled, T_A = 25°C	3.6	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = I_{CC} + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = 18 V, T_A = 25°C	–	–	5	mA
Power-On Time [4]	t_{PO}	Power-on diagnostics disabled	–	15	–	ms
	t_{PO_D}	Power-on time; CVH self-test and LBIST enabled	–	45	–	ms
Bypass Pin Output Voltage [5]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5.0 V interface	4.0	5.0	5.5	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (3.3 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF	2.93	3.3	3.63	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (5.0 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF	4	5	5.5	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [6]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [6]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [6]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [6]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [6]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [6]	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time [6]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [6]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [6]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [6]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	PWM Frequency Min Setting	–	98	–	Hz
		PWM Programmable Options (7 bits)	–	128	–	options
		PWM Frequency Max Setting	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
INCREMENTAL OUTPUT, ABI (UVW) SPECIFICATIONS						
ABI and UVW Output Angular Hysteresis [6]	hys_{ANG}	Programmable via EEPROM (6 bits)	0	–	1.38	degrees
AB Channel Resolution [6]	RES_{AB}	Programmable via EEPROM, 4 bit field. Specified in pulses per revolution, PPR	1	–	2048	PPR
AB Quadrature Resolution [6]	RES_{AB_INT}	Equal to 4 × RES_{AB}, specified in counts per revolution, CPR	4	–	8192	CPR
UVW Pole Pairs [6]	N_{pole}	DC commutation signals. Programmable via EEPROM, 4-bit field.	1	–	16	pole pairs
BUILT-IN SELF TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request. Runs in parallel with CVH self-test (if enabled).	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request. Runs in parallel with LBIST (if enabled).	–	30	–	ms

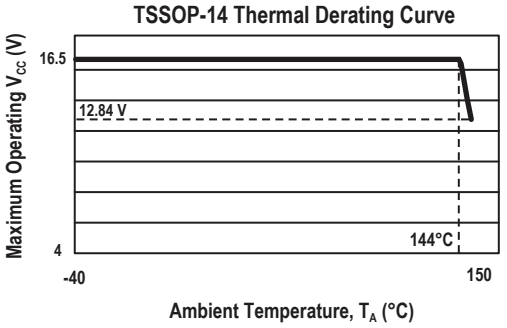
Continued on the next page…

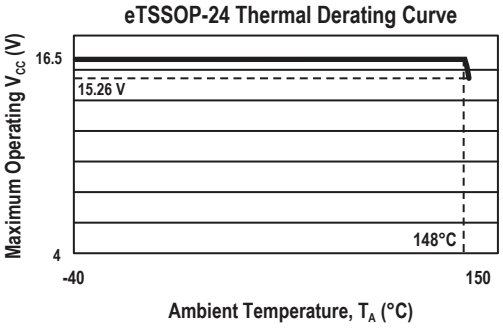
OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	1200	G
ANGLE CHARACTERISTICS						
Output [7]	RES_{ANGLE}	Both 12 and 15 bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [8]	t_{ANG}	ORATE = 0	–	1.0	–	µs
Response Time [6]	$t_{RESPONSE}$	Angular Latency; valid for ABI or UVW interface; ORATE = 0	–	15	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.0	±0.4	+1.0	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	±0.6	+1.3	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G, angle change from 25°C	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G, angle change from 25°C	–	0.9	–	degrees
Angle Noise [9]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Effective Resolution [10]		B = 300 G, T_A = 25°C	–	12.5	–	bits
Angle Drift Over Lifetime [11]	$ANGLE_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).

[2] Maximum operational voltage is reduced at high ambient temperatures (T_A). See plots below.





[3] Undervoltage flag indicates V_{CC} level below expected operational range. Degraded sensor accuracy may result.

[4] During the power-on phase, the A1333 SPI transactions will be valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.

[5] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.

[6] Parameter is not guaranteed at final test. Determined by design.

[7] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.

[8] The rate at which a new angle reading will be ready.

[9] This value represents 3-sigma or three times the standard deviation of the measured samples.

[10] Effective Resolution is calculated using the formula below:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

where σ is the Standard Deviation based on thirty averaged measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.

[11] Maximum observed angle drift following AEC-Q100 stress was 1.37 degrees.

TYPICAL PERFORMANCE CHARACTERISTICS

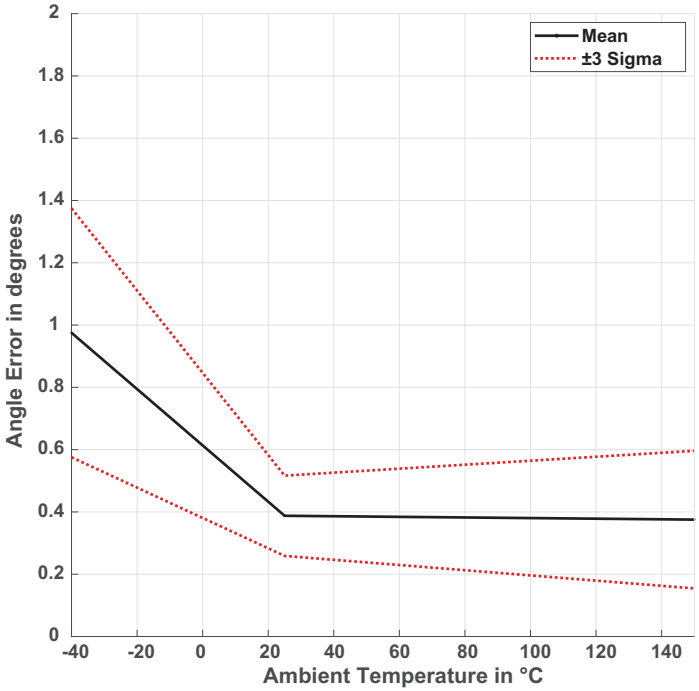


Figure 3: Peak Angle Error over Temperature (300 G)

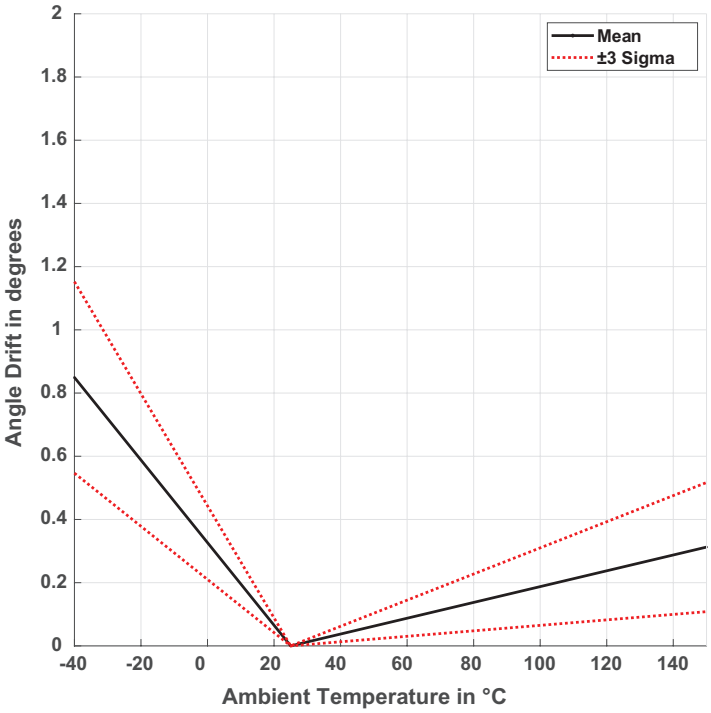


Figure 4: Maximum Absolute Drift from 25°C Reading (300 G)

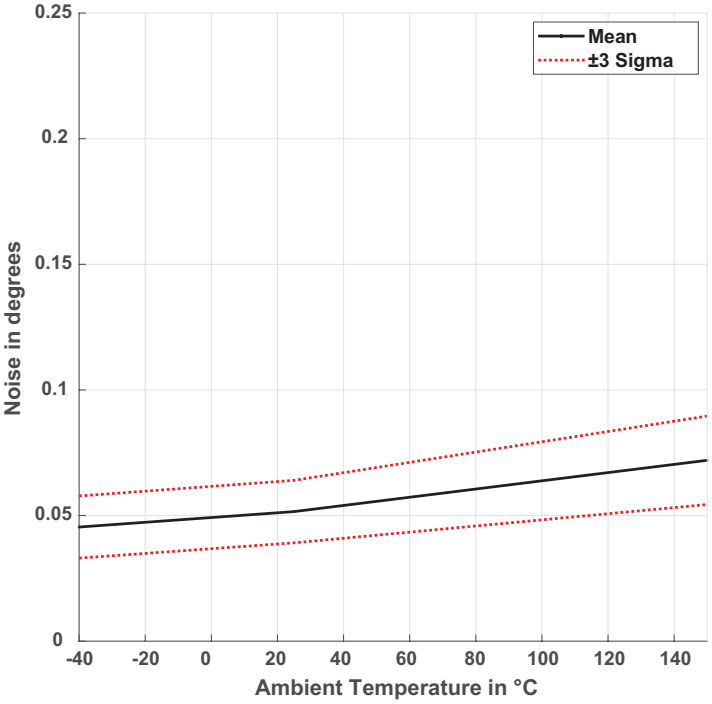


Figure 5: Noise Performance over Temperature (1 Sigma, 300 G)

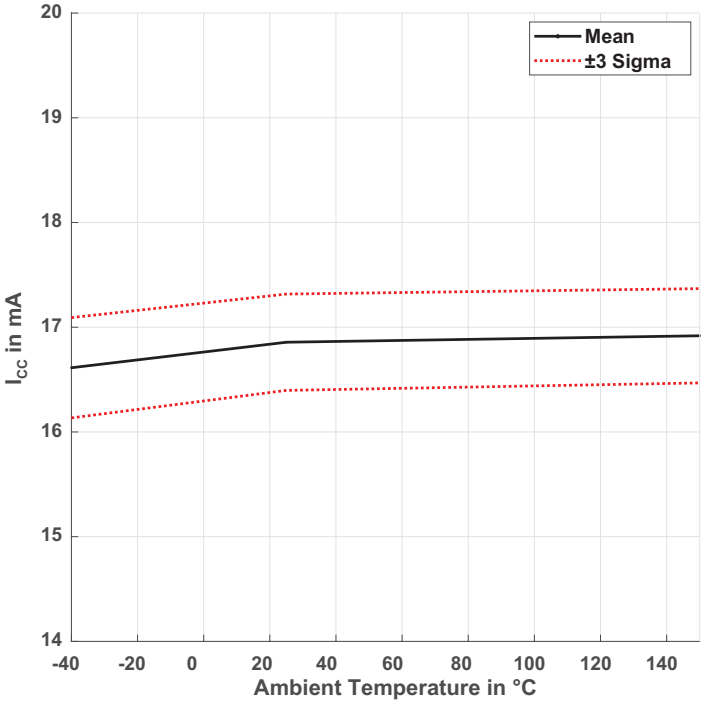


Figure 6: I_{CC} over Temperature (V_{CC} = 16.0 V)

FUNCTIONAL DESCRIPTION

Overview

The A1333 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency and reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a Circular Vertical Hall (CVH) analog front end, a high-speed sampling A-to-D converter, digital filtering, digital signal processing (which includes two separate signal paths), SPI, motor commutation outputs (UVW), and encoder outputs (A, B, I).

Advanced offset and gain adjustment options are available in the A1333. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Angle Measurement

The IC features two digital signal paths. The main signal path uses a PLL to generate high resolution, low latency angle readings. A secondary, lower power signal path (referred to as the "ZCD path") is used for turns counting, magnetic field measurement, and diagnostic comparison.

The A1333 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 15,000 rpm.

The A1333 has a typical refresh rate of 1 MHz.

Angle is represented as either a 12- or 15-bit value, based on the register address accessed.

12 Bit Angle Value; Serial register 0x20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EF	UV	P	angle(11:0)											

15 Bit Angle Value; Serial Register 0x32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	angle(14:0)														

When reading the 12-bit angle value, 3 additional status bits are provided with each packet: a general error flag (EF), undervoltage flag (UV), and a parity bit (P).

PWM output is always resolved to a 12-bit angle value. ABI/UVW operates on a 15-bit angle representation.

The zero degree position may be adjusted by writing to EEPROM.

The sensor readout is processed in various steps. These are detailed in Figure 8.

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values which are presented to the user are latched on the first SCLK edge of the SPI response frame. This results in a variable age of the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$.

Figure 7 shows the update rate and the signal delay of the different angle output paths depending on sensor settings.

The value of the "angle_zcd" (ZCD signal path) register is updated approximately every 32 µs. The field strength reading (register 0x2A) is updated approximately every 128 µs.

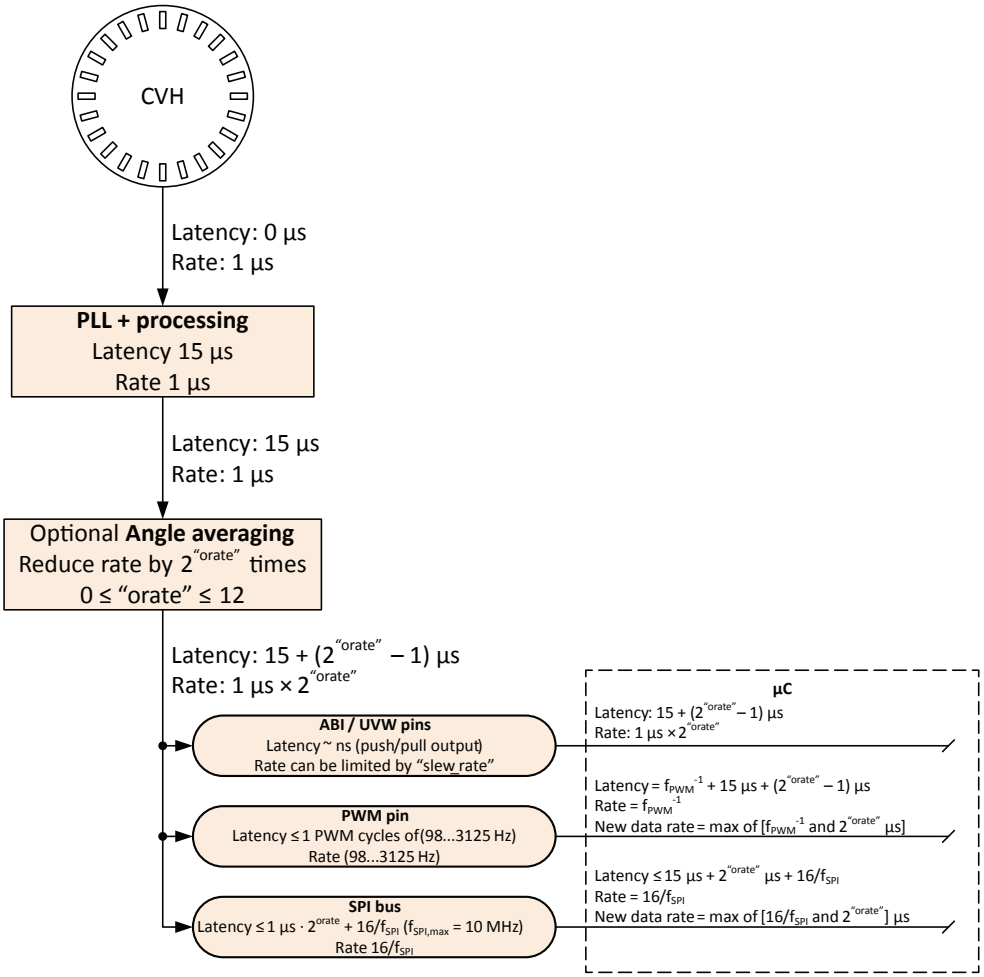


Figure 7: Update Rate and Signal Delay

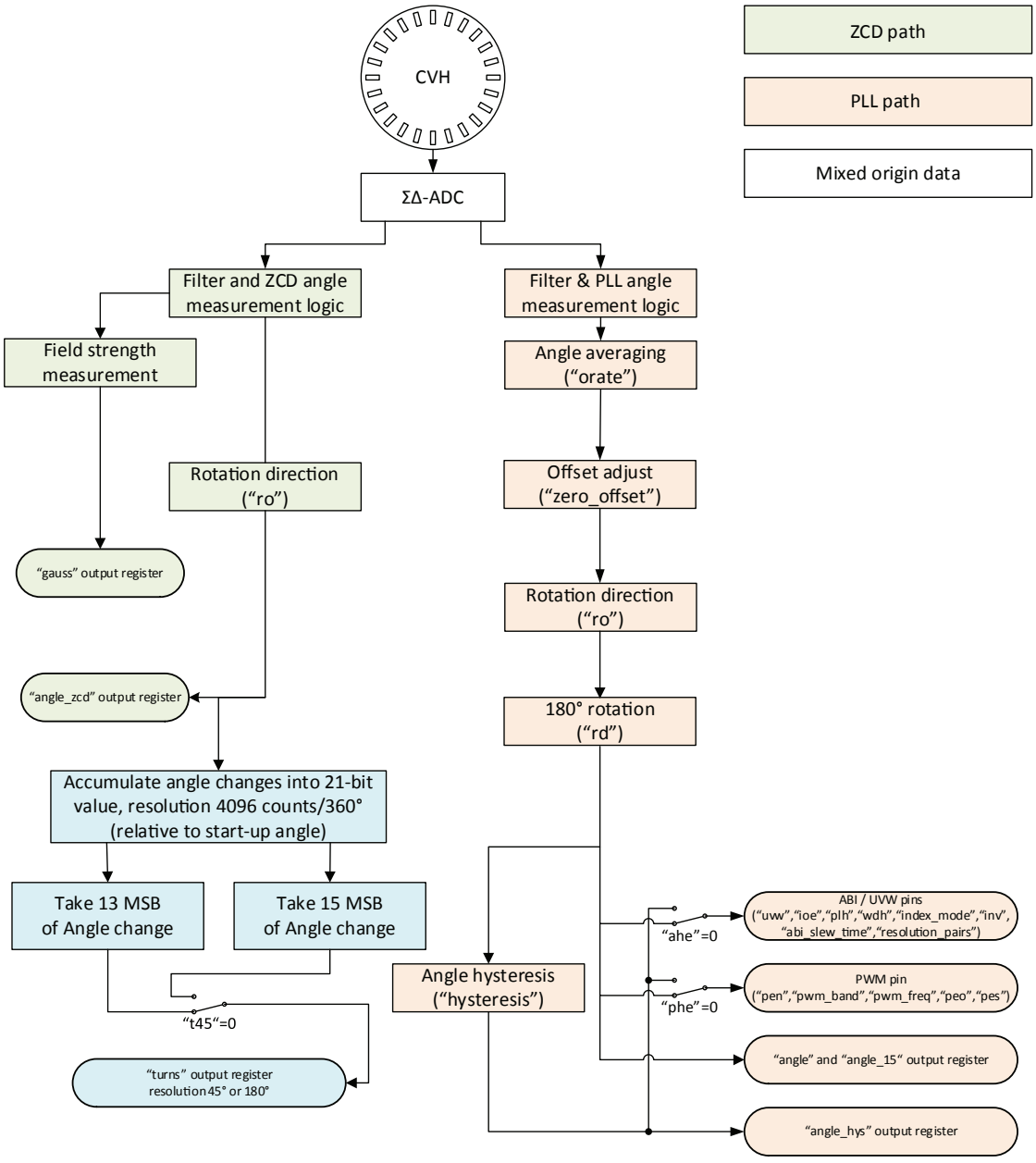


Figure 8: Angle Measurement – Sensor Readout Steps

Names in quotes correspond to EEPROM or serial register fields.

Power-Up

Upon applying power to the A1333, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as Power-On Time, t_{PO}. Regardless of the state of the device before a power cycle, the device will re-power with the shadow memory contents copied from the EEPROM anew, and serial registers in their default states. For example, on every power-up, the device will power with the "zero_offset" that was stored in the EEPROM. The extended write access field "write_adr" will be set back to its default value, zero.

PWM Output

The A1333 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostics purposes. A 5% DC corresponds to 0°; a 95% DC corresponds to 360°.

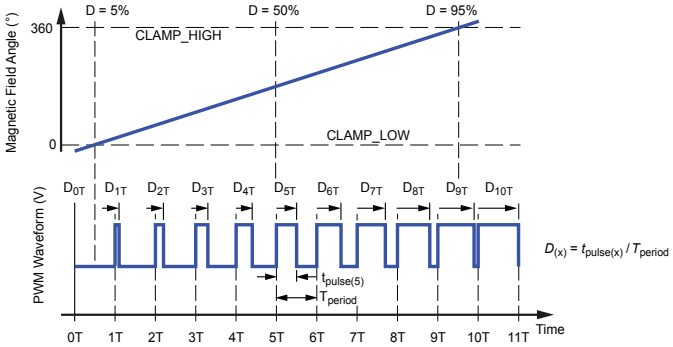


Figure 9: PWM Mode Outputs a Duty-Cycle Proportional To Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of the period. The middle 90% of the period is a linear interpolation of the angle as sampled the start of the PWM period.

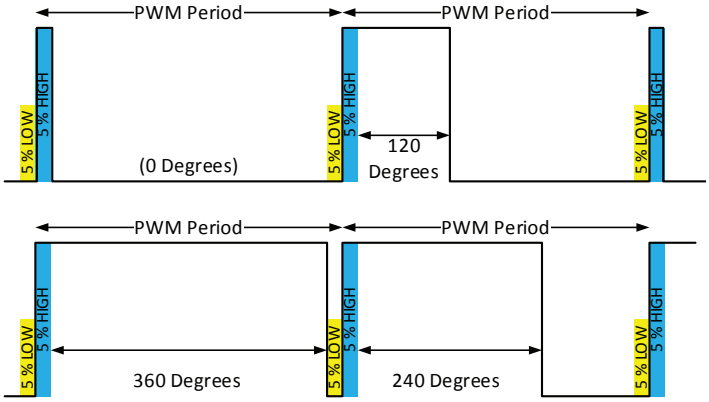


Figure 10: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax (\%)} = (4095 / 4096) \times 90 + 5 .$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together, these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PWM_FREQ	**0**	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

Incremental Output Interface (ABI)

The A1333 offers an incremental output mode in the form of quadrature A/B and Index outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per magnetic revolution, giving a cycle resolution of $(360 / 2^N)$ degrees per cycle. B is offset from A by ¼ of the cycle period. The "I" signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown below:

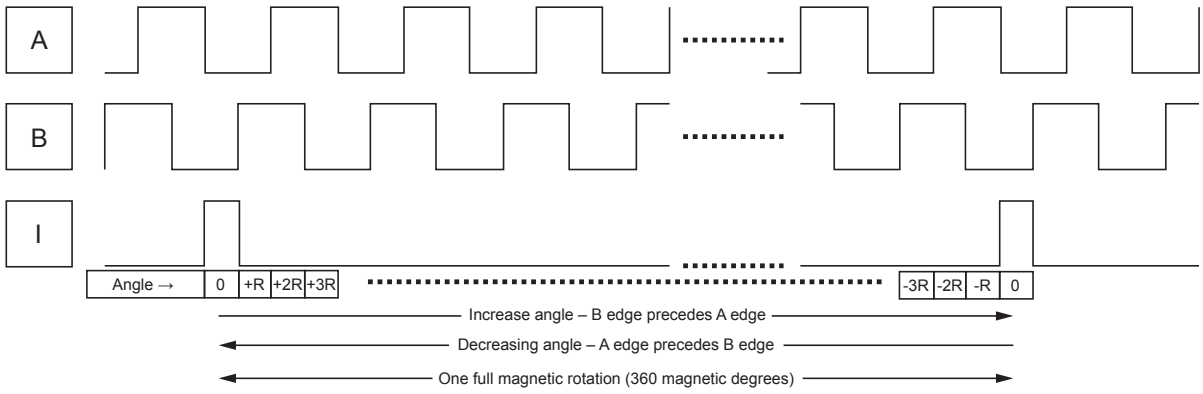


Figure 11: One Full Magnetic Revolution

Since A and B are offset by ¼ of a cycle, they are in *quadrature* and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a grey coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4

Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2 → Q1

The duration of one cycle is referred to as 360 *electrical degrees*, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior. Ideally the A and B cycle would be as shown below for a constant velocity:

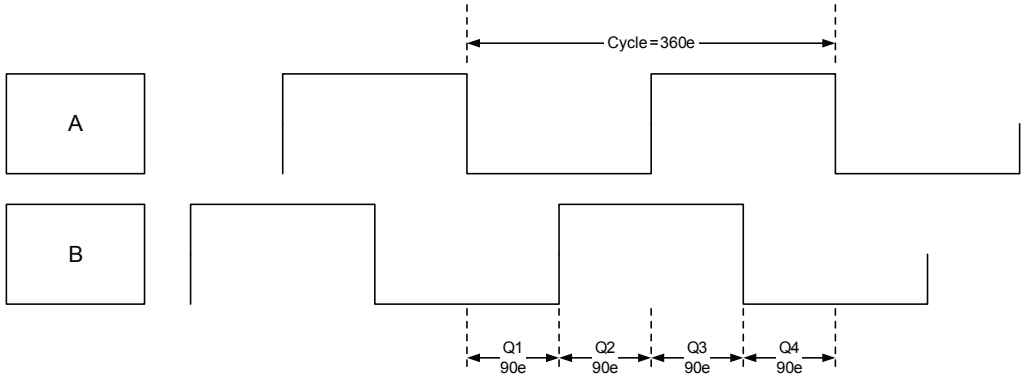


Figure 12: Electrical Cycle

In reality, the edge rate of the A and B signals, and the switching threshold of the receiver I/Os, will affect the quadrature periods:

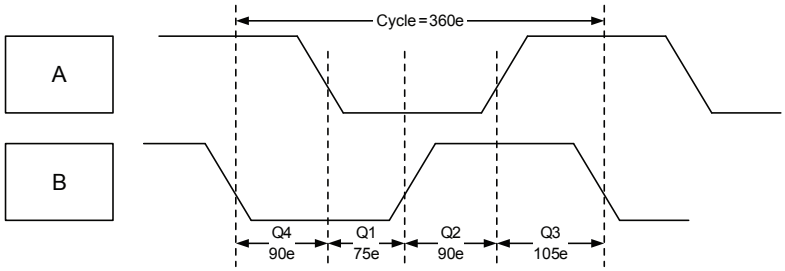


Figure 13: Electrical Cycle

Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

ABI RESOLUTION

The A1333 supports the following ABI output resolutions. This is set via the "resolution_pairs" field in EEPROM and shadow (EEPROM 0x19, bits 3:0).

ABI INVERSION

The logic levels of the ABI pins may inverted by setting the ABI.inv bit within EEPROM. This also applies if using the UVW output logic.

Table 2: ABI Output Resolution

EEPROM Resolution Field	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0	Factory Use Only					
1	Factory Use Only					
2	Factory Use Only					
3	11	13	2048	8192	0.176	0.044
4	10	12	1024	4096	0.352	0.088
5	9	11	512	2048	0.703	0.176
6	8	10	256	1024	1.406	0.352
7	7	9	128	512	2.813	0.703
8	6	8	64	256	5.625	1.406
9	5	7	32	128	11.250	2.813
10	4	6	16	64	22.500	5.625
11	3	5	8	32	45.000	11.250
12	2	4	4	16	90.000	22.5
13	1	3	2	8	180.0	45.0
14	0	2	1	4	360.0	90.0
15	n/a	n/a	n/a	n/a	n/a	n/a

INDEX PULSE

The index pulse I (or Z in some descriptions) marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the 'I' pulse has four widths, defined by the INDEX_MODE EEPROM field, as shown below:

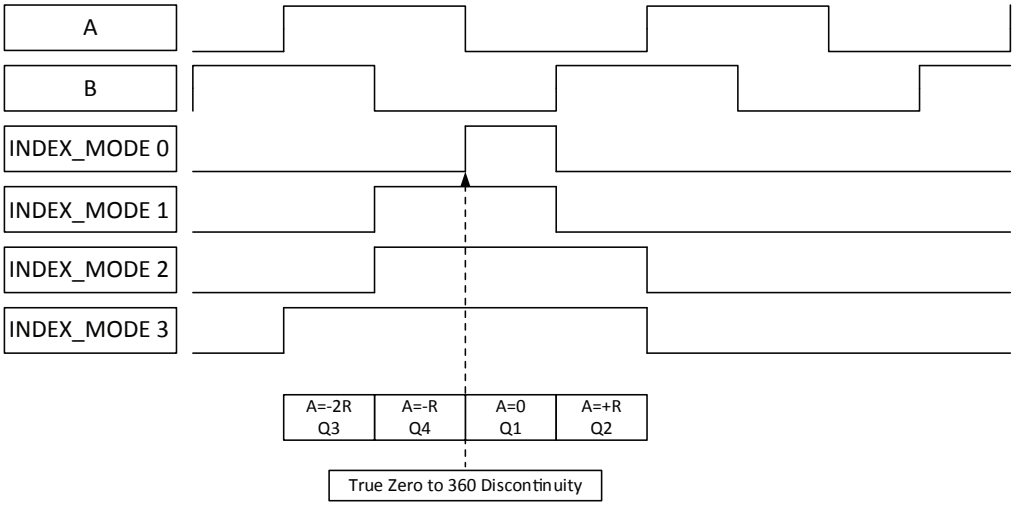


Figure 14: Index Pulse

The edge of the index pulse corresponding to the "Zero" position, as observed by the sensor, will change based on rotation direction, as shown in Figure 15.

With the magnet rotating such that the observed angle is increasing, the 0° position will be indicated by the rising edge of the Index pulse. If the magnet is rotated in the opposite direction (or the RO bit is changed in EEPROM) to produce a decreasing angle value, the 0° position will be represented by the falling edge of the Index pulse.

The ABI resolution and I pulse mode selection (described above) determine the width of the Index pulse and the corresponding shift in zero position indication.

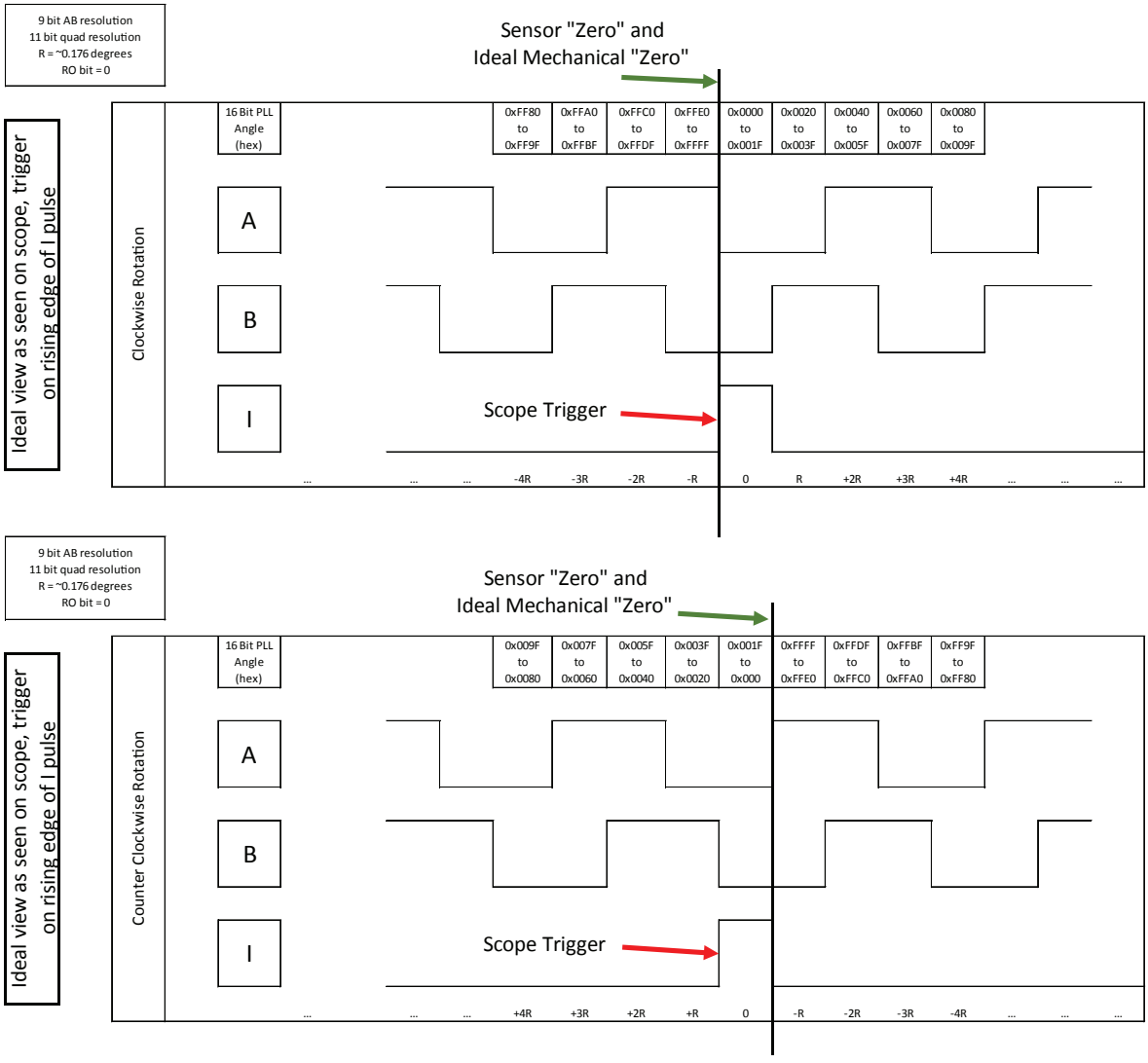


Figure 15: Index Pulse Corresponding to "Zero" Position

SLEW RATE LIMITING FOR ABI

Slew rate limiting is enabled when the "abi_slew_limit" field is non-zero. This option separates the sample update rate from the ABI output rate, and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby "skipping" one or more quadrature states. In this case, the slew rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output "catches up" with the angle samples, at which point the normal sample rate output resumes. This skipping will most likely occur either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs. The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation would not on average require ABI transitions greater than the angle sample rate.

In both cases, the ABI output will correctly track the rotation position; however, the speed of the ABI edges will be accomplished at the slew rate limit set in EEPROM. Whenever slew rate limiting occurs, the SRW flag in the WARN serial register will assert informing the system of the occurrence.

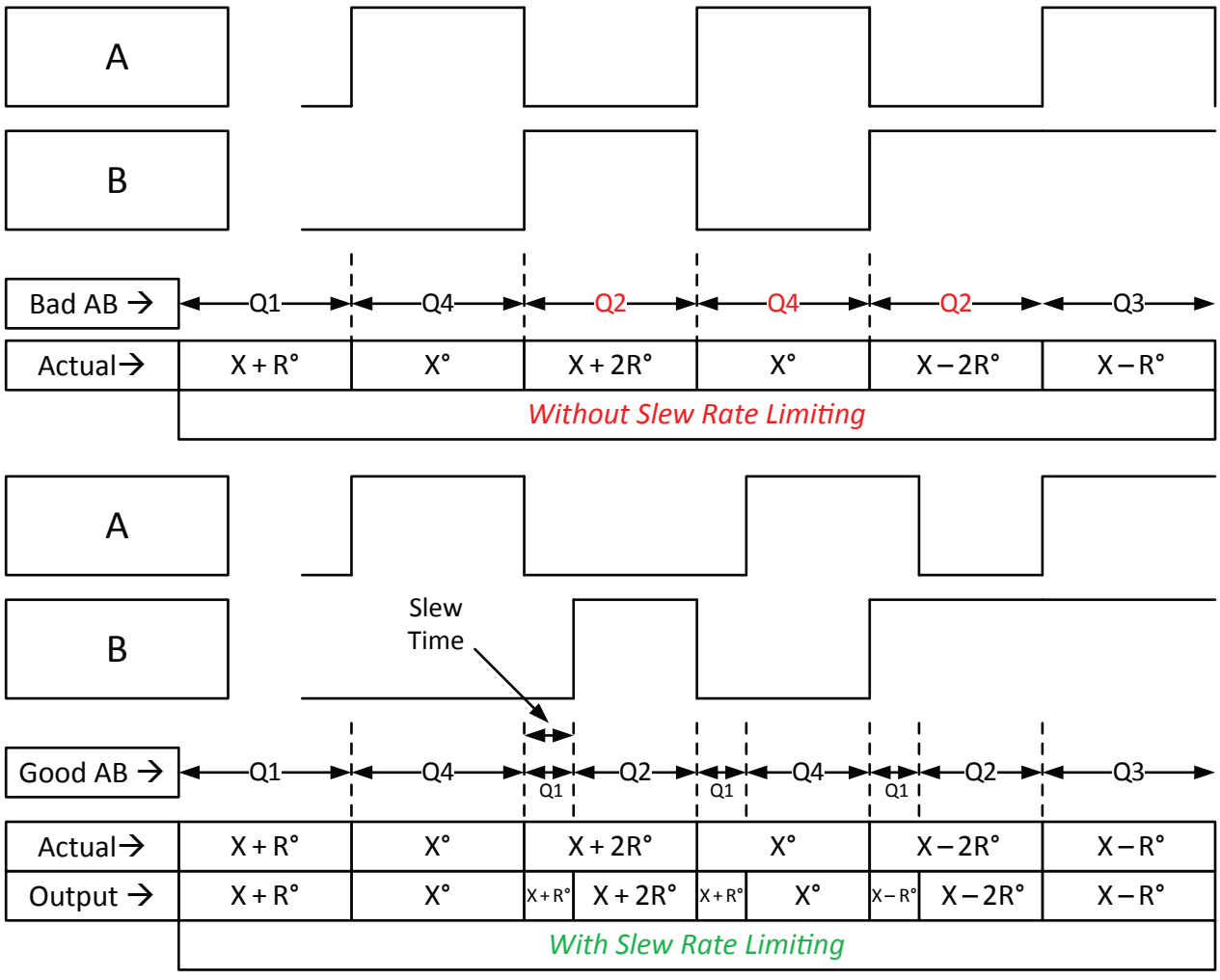


Figure 16: Slew Rate Limiting

Brushless DC Motor Output (UVW)

The A1333 offers U, V, and W signals for stator commutation of brushless DC (BLDC) motors. The device is mode-selectable for 1 to 16 pole-pairs. The BLDC signals (U, V, and W), are generated based on the quantity of pole-pairs and on angle information from the angle sensor. The U, V, and W outputs switch when the measured mechanical angle crosses the value where a change should occur. If hysteresis is used, then the output update method is different. The output behavior when hysteresis is enabled is described in the Angle Hysteresis section. Figure 17 and Figure 18 below show the UVW waveforms for three and five pole-pair BLDC motors.

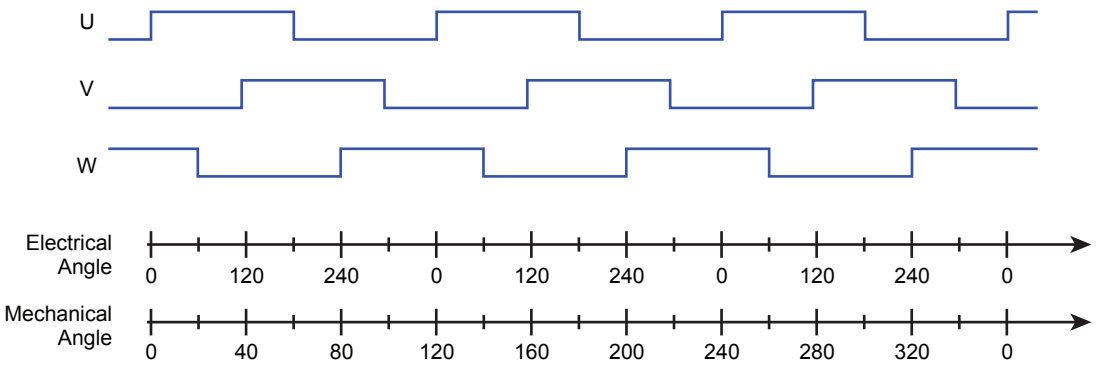


Figure 17: U, V, W Outputs for Three Pole-Pair BLDC Motor

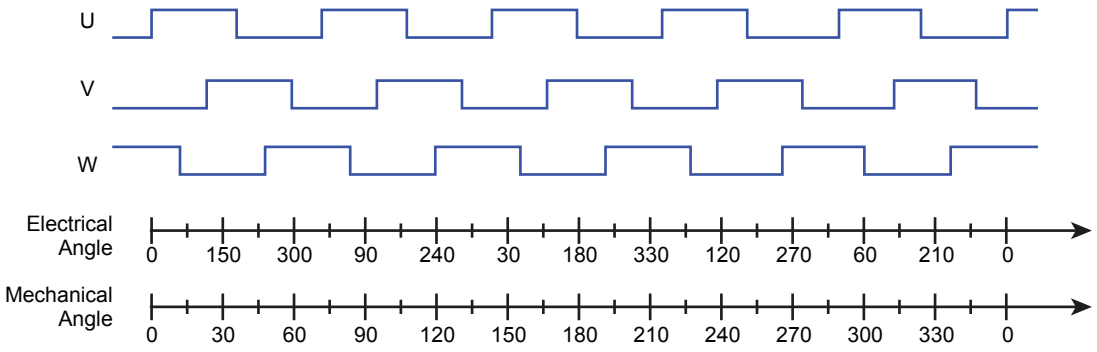


Figure 18: U, V, W Outputs for Five Pole-Pair BLDC Motor

Table 3: UVW Pole Pair Settings

Quantity of Poles ("resolution_pairs")	Quantity of Pole-Pairs	Conversion from Electrical Degrees to Mechanical Degrees	
		Electrical (°)	Mechanical (°)
0000	1	90	90
0001	2	90	45
0010	3	90	30
0011	4	90	22.5
0100	5	90	18
0101	6	90	15
0110	7	90	12.857…
0111	8	90	11.25
1000	9	90	10
1001	10	90	9
1010	11	90	8.1818…
1011	12	90	7.5
1100	13	90	6.9231…
1101	14	90	6.4286…
1110	15	90	6
1111	16	90	5.625

Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A1333, the hysteresis field (ANG.hysteresis) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$HYSTERESIS \times (360 / 16384) \text{ degrees} \quad ,$$

HYSTERESIS is a 6-bit wide EEPROM field, allowing a range of 0 to 1.384 degrees of hysteresis to be applied.

The hysteresis-compensated angle can be routed to the ABI or UVW interface by setting the AHE bit in EEPROM to a 1 (bit 12 of address 0x19). On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.angle_hys) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 19. The current angle position as measured by the sensor is at the "head" of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle will be the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the "head" was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or "head" for the purposes of hysteresis, is viewable via the STA.rot bit, where 0 is increasing angle direction and 1 is in decreasing angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle will skip consecutive resolution steps.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle will tend to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current "head") rather than to the average position of the jitter.

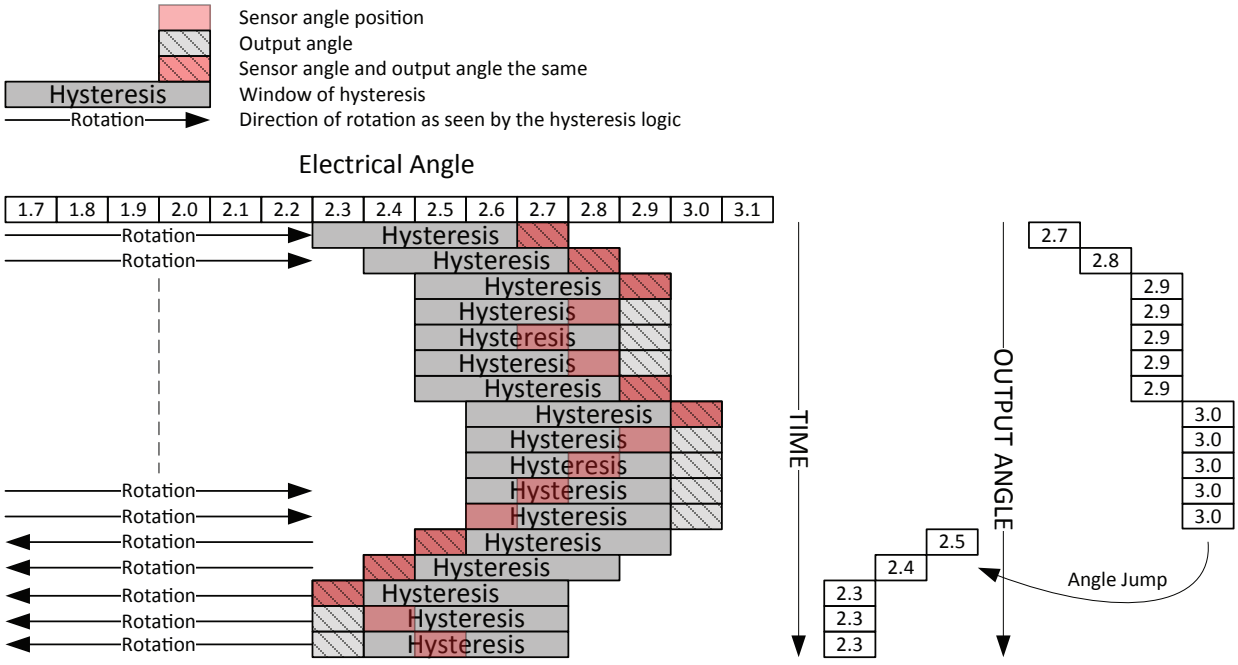


Figure 19: Effect of Hysteresis

Note: The rotation direction resets to 0, or increasing angle direction. At power-up or after LBIST, the hysteresis window will always be behind the initial angle position, so if hysteresis is enabled a decreasing angle direction of rotation will not register until the hysteresis window is past.

Turns Counting

The A1333 uses a secondary, lower power signal path (called the "ZCD" path) to track rotation turns. The turns counter logic tracks the turns in either 45 or 180 degree increments, based on the T45 register field. The signal path which tracks total turns does not implement the same angle compensation as the primary signal path. Because of this, the turns count value will not precisely match the primary angle output.

The turns counter saturates at +2047 and –2048 in the 45-degree mode and +511 and –512 in the 180-degree mode. If this happens, the Turns Count Warning Flag (bit 0 of serial register 0x26) will assert and stay asserted until the turns counter is reset via the Control register (serial register 0x1E). (see Primary Serial Interface Registers Reference section).

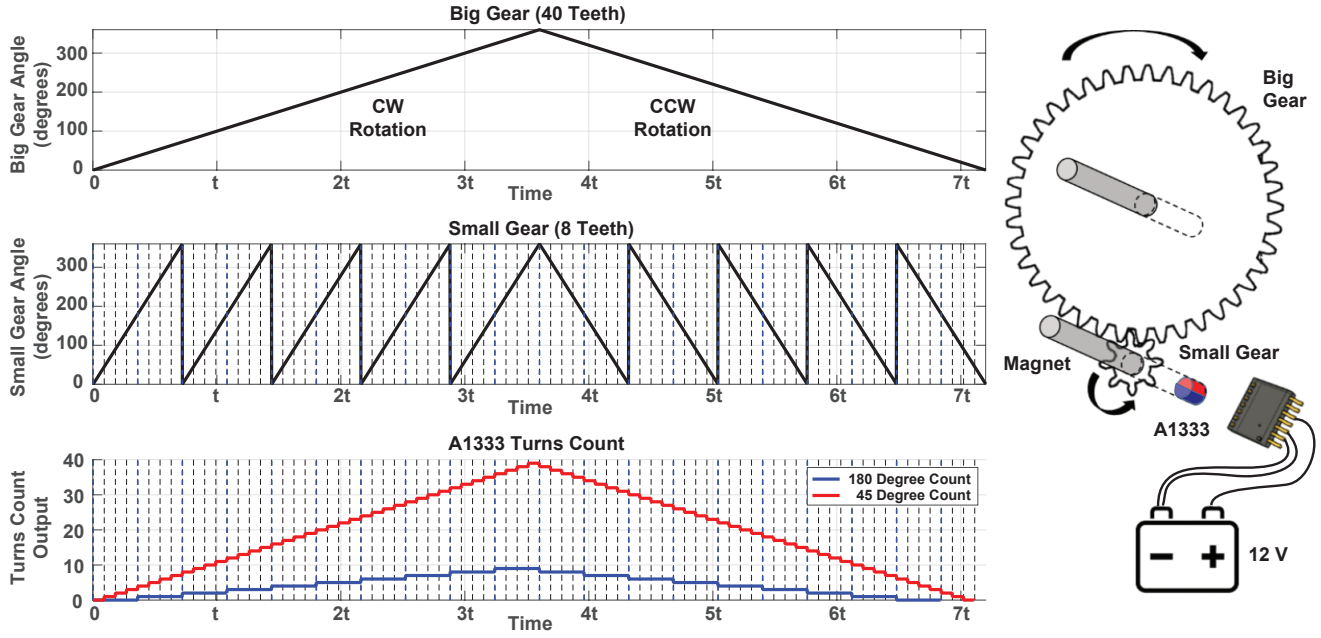


Figure 20: Example of a Turns Counting Application

INVOKING A TURNS COUNTER RESET

Resetting the turns counter is a command invoked using the "special" field of the CTRL register (Register address 0x1E, see Primary Serial Interface Reference). Following a reset, turns are tracked relative to that point, as measured by the signal path (ZCD).

DEVICE PROGRAMMING INTERFACES

The A1333 can be programmed in two ways:

- Using the *SPI interface* for input and output, whilst supplying the VCC pin with normal operating voltage
- Using a *Manchester protocol* on the supply pin for input, and the PWM pin for output.

The A1333 features an internal charge pump, and unlike earlier Allegro sensors, it does not require high-voltage pulses to write EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. Locking the EEPROM from one will lock EEPROM write access from both protocols.

A separate setting to completely disable the Manchester interface is available in the PWI.dm field of the EEPROM. Using this setting will cause the sensor to ignore any commands entered using Manchester protocol. The SPI interface will not be disabled by disabling the Manchester interface.

For details regarding the programming procedures, contact your Allegro representative.

SPI

The A1333 provides a full-duplex 4-pin SPI interface for each die using SPI mode 3 (CPOL =1, CPHA = 1). The sensor responds to commands received on the corresponding MOSI (Master-Out Slave-In), SCLK (Serial Clock), and CS (Chip Select) pins, and outputs data on the MISO (Master-In Slave-Out) pin.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE SPECIFICATIONS (for 3.3 V SPI Mode)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, 5 V compliant	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5.0 V SPI Mode) (*Contact Allegro for 5 V SPI ordering information*)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, 5 V compliant	4	5	5.5	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [1]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [1]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [1]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [1]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [1]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [1]	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time [1]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [1]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [1]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [1]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

[1] Parameter is not guaranteed at final test. Determined by design.

SPI Timing

The SPI interface operates in pure Slave mode, with the Master controlling the SCLK, MOSI, and CS lines. The Master can maximize data throughput, up to f_{SCLK}(max) of 10 MHz.

Figure 22 shows the timings of the Write and Read cycles.

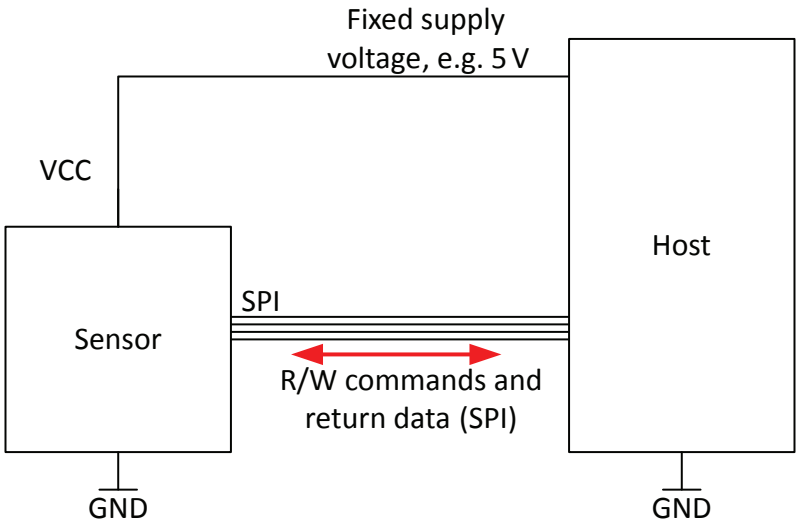


Figure 21: SPI Interface Programming Setup

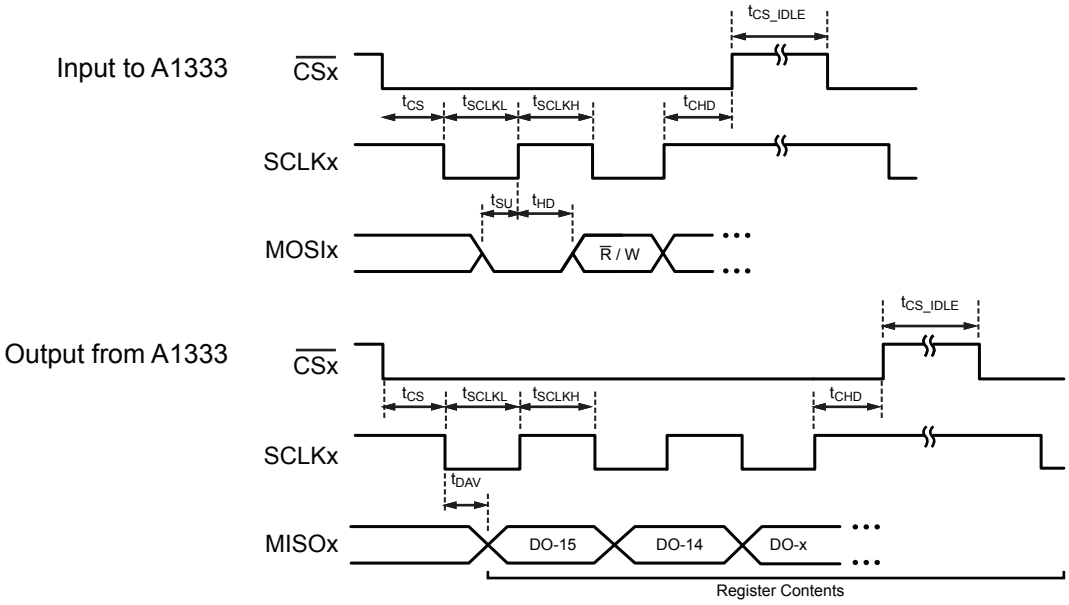


Figure 22: A1333 SPI Interface Timings: (upper) input and (lower) output

SPI Message Frame Size

A SPI transaction is a minimum of 16 bits in length. An extended 20-bit SPI packet allows 4 bits of CRC to accompany every data packet. The 4-bit CRC is automatically generated and placed on the MISO line once a 17th SCLK edge is detected by the A1333. The incoming CRC on the MOSI line is ignored unless the PWI.SC bit is set within EEPROM (0x1B bit 0). When enabled, a SPI packet with an incorrect CRC will be discarded, and the CRC error flag set (bit 10 of Serial registers 0x26:0x27).

SPI Output Voltage Levels

The A1333 can operate in either 3.3 or 5.0 V SPI mode. Contact Allegro MicroSystems for more information.

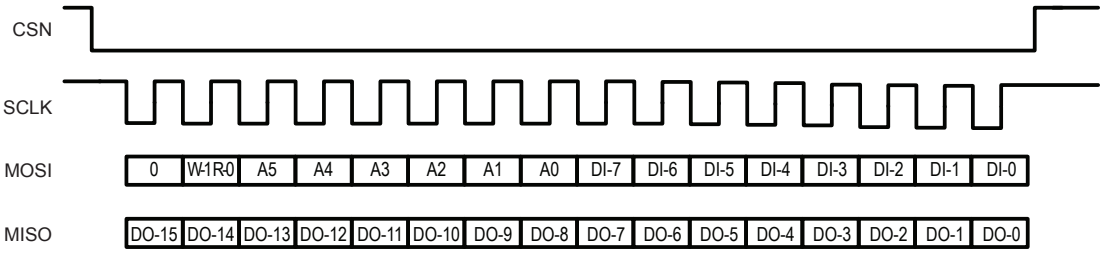


Figure 23: Sixteen Bit SPI Transaction

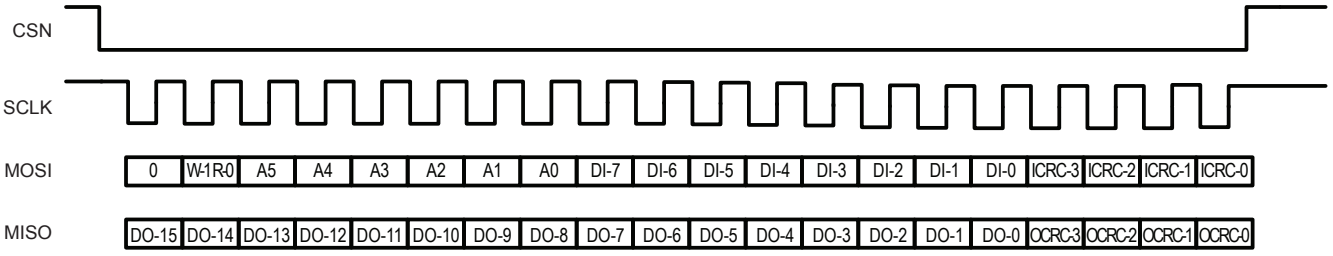


Figure 24: Twenty Bit SPI Transaction

SPI CRC

A 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The CRC is based on the polynomial $x^4 + x + 1$ with the LFSR preset to all 1s. The 16-bit packet is shifted through from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in the following figure. Example “C” code to calculate the CRC is included in Appendix A.

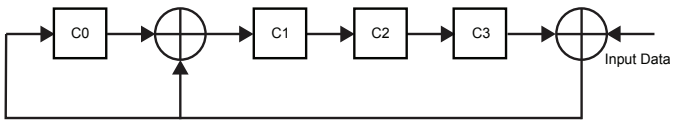


Figure 25: SPI CRC

Write Cycle Overview

Write cycles consist of a 1-bit low, a 1-bit R/W asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16 bit serial register, two Write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the Master-generated SCLK signal. The complete SPI packet is latched on the rising edge of the Master-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet. Including 16 data bits and 4 optional CRC bits, automatically included if a 17th SCLK edge is detected. The data bits correspond to the register contents selected during the previous read command. In the case where no previous read command was issued, the MISO line will transmit all zeros.

During periods where the Chip Select line is high the SCLK line must also be kept high.

Read Cycle Overview

Read cycles have two stages: a Read command, selecting a serial register address, followed by another SPI command to transmit the data from the selected register. Both commands consist of a 1-bit sync (low), a 1-bit R/W, 6 address bits identifying the target register, and 8 data bits (all zeros because no data is being written).

In the first stage, as with the Write command, Read command MOSI bits are clocked-in on the rising edge of the Master generated SCLK signal, and input data latched on the rising edge of the ($\overline{CS}$) signal. During the first Read stage, the simultaneous MISO signal output is the contents of the SPI read data from the previous Read command cycle.

In the second stage, the Read command continues on the next falling edge of the Master-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, latched on the falling edge of $\overline{CS}$. The MISO bits transmit on the falling edges of the SCLK signal, such that the Master can sample them on the SCLK rising edges.

Because a SPI Read command can transmit 16 data bits at one time, and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame (See Table 3 for Serial Register format). This is accomplished by providing an even serial address value. If an odd value address is sent, only the contents of the single byte will be returned, with the eight most significant bits within the SPI packet set to zero.

Example: To read all 16 bits of the Error register (0x24:0x25), a SPI read request with the address bits set to 0x24 should be sent. If only the 8 LSBs are desired, the address 0x25 should be used.

Figure 26 shows examples of both a SPI write and a SPI read request, using a 16-bit SPI message frame.

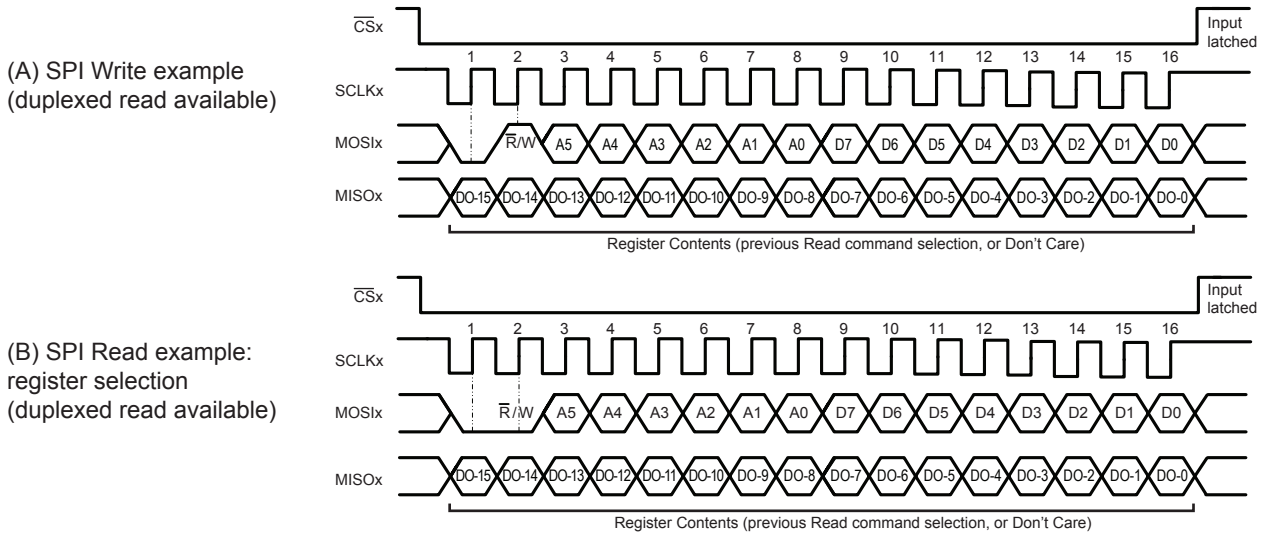


Figure 26: SPI Read and Write Pulse Sequences

MANCHESTER SERIAL INTERFACE

To facilitate addressable device programming when using the unidirectional ABI or UVW protocols, with no need for additional wiring, the A1333 incorporates a serial interface on the VCC line. (Note: The A1333 may be programmed via the SPI, with additional wiring connections). This interface allows an external controller to read and write registers in the A1333 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication with up to four A1333 die is possible.

To prevent any undesired programming of the A1333, the serial interface can be disabled by setting the Disable Manchester bit (PWI.DM EEPROM address 0x1B bit 3) to a 1. With this bit set, the A1333 will ignore any Manchester input on VCC.

Entering Manchester Communication Mode

Provided the Disable Manchester bit is not set in EEPROM, the A1333 continuously monitors the VCC line for valid Manchester commands. The part takes no action until a valid Manchester Access Code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and specify the output format used during Read operations:

1. **Manchester Access Code:** Enters Manchester Communication Mode; Manchester code output on the PWM pin.
   A. Manchester Access Code: 0x62D2 to register address 0x3F.
2. **Manchester Exit Code:** Returns the PWM pin to normal (angle data) output format.
   A. Manchester Exit Code: Any valid Manchester write to address 0x3F, not equal to the Manchester Access Code.

Once the Manchester Communication Mode is entered, the PWM output pin will cease providing angle data, interrupting any data transmission in progress. Both the Access and Exit code must be written to address 0x3F (address field of all 1's).

Transaction Types

As shown in Figure 27, the A1333 receives all commands via the VCC pin, and responds to Read commands via the PWM pin.This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line.

Each transaction is initiated by a command from the controller; the A1333 does not initiate any transactions. Two commands are recognized by the A1333: Write and Read.

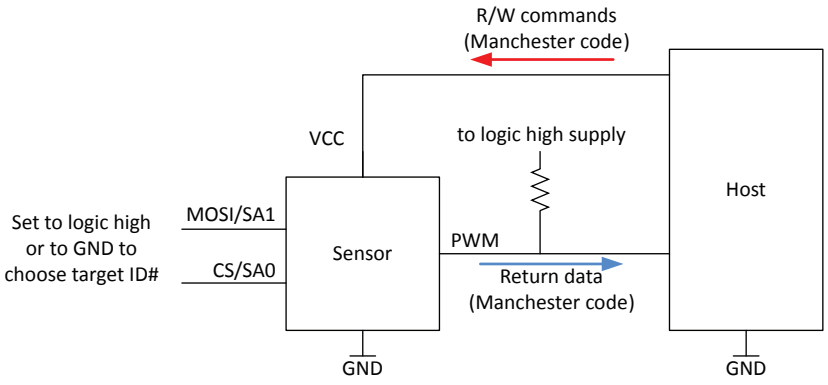


Figure 27: Manchester Interface Programming Setup

Table 4: EEPROM Value for Serial Communication

Address	Bits	Parameter Name	Description
0x1B	3	Disable Manchester (DM)	When set (logic 1) the A1333 ignores any Manchester input on the VCC line

Manchester Message Structure

The general format of a command message frame is shown in Figure 28. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

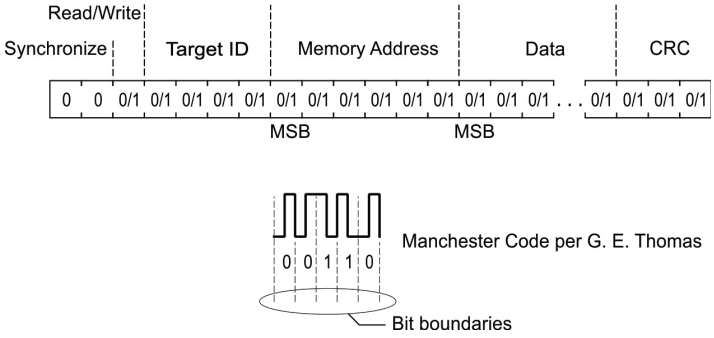


Figure 28: General Format for Serial Interface Commands

A brief description of each bit is provided in Table 5.

Table 5: Manchester Command General Format

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Target ID	0/1	Used to select a set of target chips/die, based on ID value.
6	Address	0/1	[Read/Write] Serial address
16	Data	0/1	Requested serial register contents (Write operation only)
3	CRC	0/1	Incorrect value indicates errors

The Die ID value is determined by the state of the SA0 and SA1 pins.

Table 6: Pin Values

MOSI/SA1	CS/SA0	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the Target ID field, die can be selected via their ID value, allowing up to four die to be individually addressed and providing for different group addressing schemes. If the Target ID is all zeros the Manchester command is treated as a broadcast and the ID is ignored.

Example: If Target ID = 1010, all die with ID3 or ID1 will be selected.

Table 7: Target ID

Target ID			
ID3	ID2	ID1	ID0

Reading Data Using Manchester Encoding

A Read command with the desired register number is sent from the controller to the A1333. The device responds with a Read Response frame using the Manchester protocol.

In addition to the contents of the requested memory location, a Return Status field is included with every Read Response. This field provides the ID used to communicate with the part and any errors which may have occurred during the previous transaction. These bits are:

- **ID** – ID (SA1/SA0) unless BC = 1 (ID will be 00)
- **BC** – Broadcast; ID field was zero
- **AE** – Abort Error; edge detection failure after sync detect
- **OR**– Overrun Error; a new Manchester command has been received before the previous request could be completed
- **CS** – Checksum error; a prior command had a checksum error

Table 8: Return Status Bits

Return Status Bits (5 bits)					
5	**4**	**3**	**2**	**1**	**0**
ID		BC	AE	OR	CS

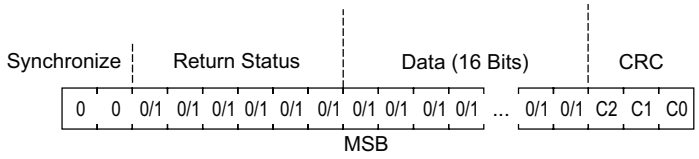


Figure 29: Manchester Read Response

Error Checking

The serial Manchester interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1 \ ,$$

and the calculation is represented graphically in Figure 30.

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. Example “C” code to calculate the CRC is included in Appendix A.

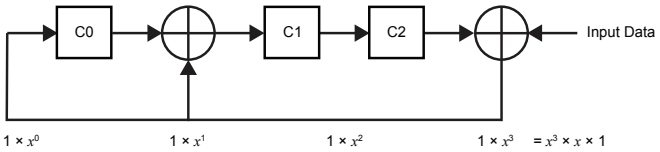


Figure 30: Manchester CRC Calculation

Manchester Interface Reference

Table 9: Manchester Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Bit Rate		Defined by the input message bit rate sent from the external controller	2.2	–	40	kbps
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Read Delay	t_{START_READ}	Delay from the end of the final bit cell of a Read command to beginning of the first sync bit of the Read acknowledge frame	$-¼ \times t_{bit}$	–	$¼ \times t_{bit}$	µs
INPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.8	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	5.7	V
OUTPUT SIGNAL VOLTAGE (APPLIED ON PWM LINE)						
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{pullup} = 5 kΩ	$0.9 \times V_S$	–	–	V
		Maximum R_{pullup} = 50 kΩ	$0.7 \times V_S$	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.1	V

[1] Determined by design.

The following command messages can be exchanged between the device and the external controller:

- Manchester Access Code
- Manchester Exit Code
- Read
- Read Response
- Write

For EEPROM address information, refer to the EEPROM Structure section. For serial address locations, refer to the serial register map.

Table 10: Manchester Access Code

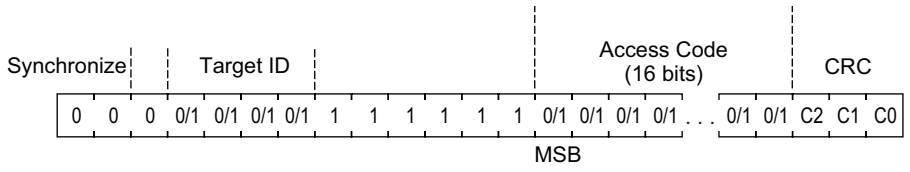
Function	Transmits the Access Code to the A1333. Enters Serial Communication mode with the desired output protocol.
Syntax	Sent by the external controller on the A1333 VCC pin.
Related Commands	Related command: Serial Exit Code
Pulse Sequence	
Options	Access Codes: Manchester Access Code = 0x62D2 Selects Manchester output on the PWM pin.
Examples	The Manchester Access Code operates as a broadcast pulse, meaning the Target ID field is inconsequential. For example, if two A1333s configured with ID0 and ID1 respectively are sharing a common V_{CC} line, a Manchester Access Code with a Target ID Value of 0x1 results in both sensors entering Manchester Serial Communication mode.

Table 11: Manchester Exit Code

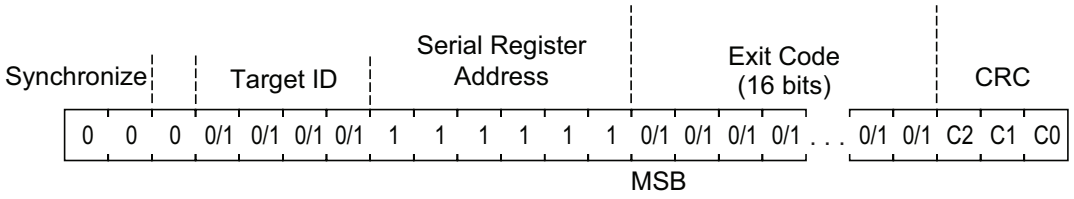
Function	Returns the A1333 to normal operation.
Syntax	Sent by the external controller on the A1333 VCC pin. Manchester Exit Code = Any value other than 0x62d2
Related Commands	Manchester Access Codes
Pulse Sequence	
Options	None
Examples	Similiar to the Manchester Access code, acts as a broadcast pulse. To exit the serial communication mode, the Exit Code can be any value besides the Access Code (such as 0x0000).

Table 12: Manchester Read

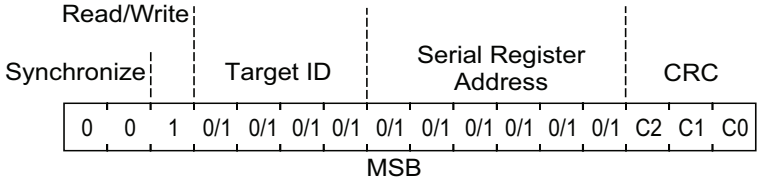
Function	Determines the serial address within the A1333, from which the next Read Response will transmit data. The A1333 must first receive a Manchester Access Code before responding to a read command.
Syntax	Sent by the external controller on the A1333 VCC pin.
Related Commands	Read Response
Pulse Sequence	
Options	None
Examples	

Table 13: Manchester Read Response

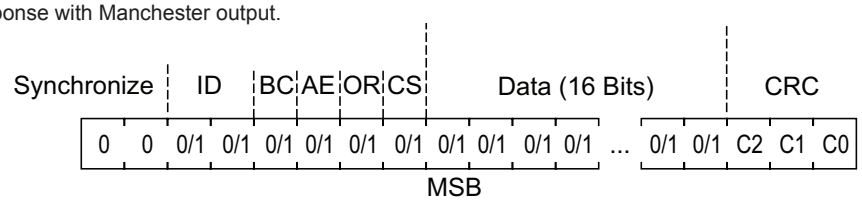
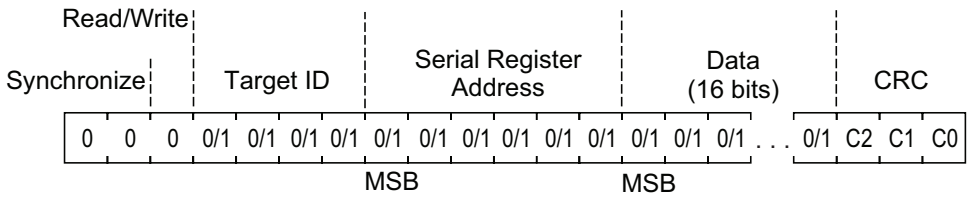
Function	Transmits to the external controller data retrieved from the A1333 serial register in response to the most recent Read command.
Syntax	Sent by the A1333 on the PWM pin. Sent after a Read command.
Related Commands	Read
Pulse Sequence	Read Response with Manchester output. 
Options	Read from an Even address returns Even byte [15:8] and Odd byte [7:0]. Read from an Odd address returns Odd byte [7:0] only. Data bits [15:8] will be zeroes.
Examples	–

Table 14: Manchester Write

Function	Transmits to the A1333 data prepared by the external controller.
Syntax	Sent by the external controller on the A1333 VCC pin.
Related Commands	
Pulse Sequence	
Options	Data is written to Address and Address+1 if Even address (16-bit write). If Odd address, only 8 bits are written (LSB of 16-bit data field).
Examples	

EEPROM AND SHADOW MEMORY USAGE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of Shadow Memory is substantially faster than accessing EEPROM. In situations where many parameter need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register, and will return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and Shadow locations may be read without unlocking. The mapping of bits from registers addresses in EEPROM to their corresponding register addresses in SHADOW is shown in the EEPROM table (See chapter “EEPROM table”).

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM, shadow registers, and registers for additional status and diagnostics. All extended registers are up to 32 bits wide.

Read Transaction from EEPROM (or Shadow Memory)

Invoking an extended read access is a three-step process:

1. Load the ERA register (using SPI or Manchester direct access) with the target extended address. ERA is the 8-bit extended address that determines which extended memory address will be accessed.
2. Invoke the extended access by writing the direct ERCS register EXR bit with ‘1’. The ERA address is then read, and the data is loaded into the ERD registers.
3. Read the ERD registers (using SPI or Manchester direct access) to get the extended data. This will take multiple packets to obtain all 32 bits.

EEPROM read accesses may take up to 2 µs to complete. The RDN bit in the ERCS register can be polled to determine if the read access is complete before reading the data. Shadow and AUX register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, as it could change during the serial access and the data will be inconsistent. It is also possible that a SPI CRC error will be detected if the data changes during the serial read via the SPI interface.

For example, to read location 0x1F in the EEPROM:

- Write 0x1F to lower 8 bits of ERA (0x1F to ERA+1, Address 0x0B)
- Write 0x80 to ERCS
- Read ERCS+1 until bit 0 (RDN) is set (or wait enough time)
- Read ERD (upper 16 bits of read data)
- Read ERD+2 (lower 16 bits of read data)

Write Transaction to EEPROM (or Shadow Memory)

Invoking an extended write access is a three-step process:

4. Load the EWA register (using SPI or Manchester direct access) with the target extended address.
5. Load the EWD registers (using SPI or Manchester direct access) with the data to be written to the target. This will take four SPI writes or 2 Manchester packets to load all 32 bits of data.
6. Invoke the extended access by writing the direct EWCS register EXW bit with ‘1’.

The EWA address is then written with the 32-bit EWD data.

The WDN bit in the EWCS register can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can take up to 24 ms to complete. Shadow register writes complete immediately in one system clock cycle after synchronization.

For example, to write location 0x1F in the EEPROM with 0x00A45678:

- Write 0x1F to lower 8 bits of EWA register (0x1F to EWA+1 Address 0x03)
- Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, 0x78 to EWD+3)
- Write 0x80 to EWCS
- Read EWCS+1 until bit 0 (WDN) is set (or wait enough time)

If an access violation occurs (address not unlocked), the transaction will be terminated and the corresponding RDN or WDN bit set, and the XEE warning bit will assert. The XEE bit in the ERR register will also set if the EEPROM write aborts.

Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, one must address to the Shadow Extended addresses, which are located at an offset of 0x40 above the EEPROM. Refer to the EEPROM table for all addresses.

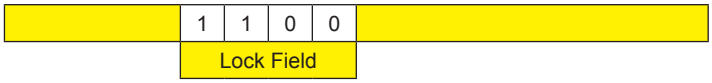
EEPROM Locking

The A1333 uses two types of "locks" to control access to EEPROM.

1. **KeyCode:**
   Entered via SPI or Manchester. This code permits write access to EEPROM, dependent on the state of the EEPROM lock field. The keycode is written to the KEYCODE field within serial registers (bits 15:8 of Address 0x3C:3D).
   A. KeyCode = 0x0027811F77, written using five separate write operations
2. **EEPROM Lock Fields:**
   A 4-bit word within EEPROM, which controls access to EEPROM and Shadow. Once word is written and the part is repowered, that section of EEPROM cannot be overwritten.

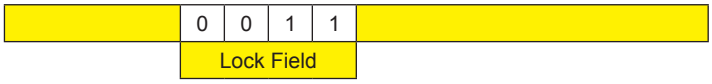
Lock Field Example:

A lock field of 1100_2 means:



EEPROM writes are disabled, but Shadow memory may still be changed.

A lock field of 0011_2 means:



EEPROM and shadow register writes are disabled.

The lock patterns 1100_2 and 0011_2 are picked to minimize the likelihood of accidental EEPROM locking.

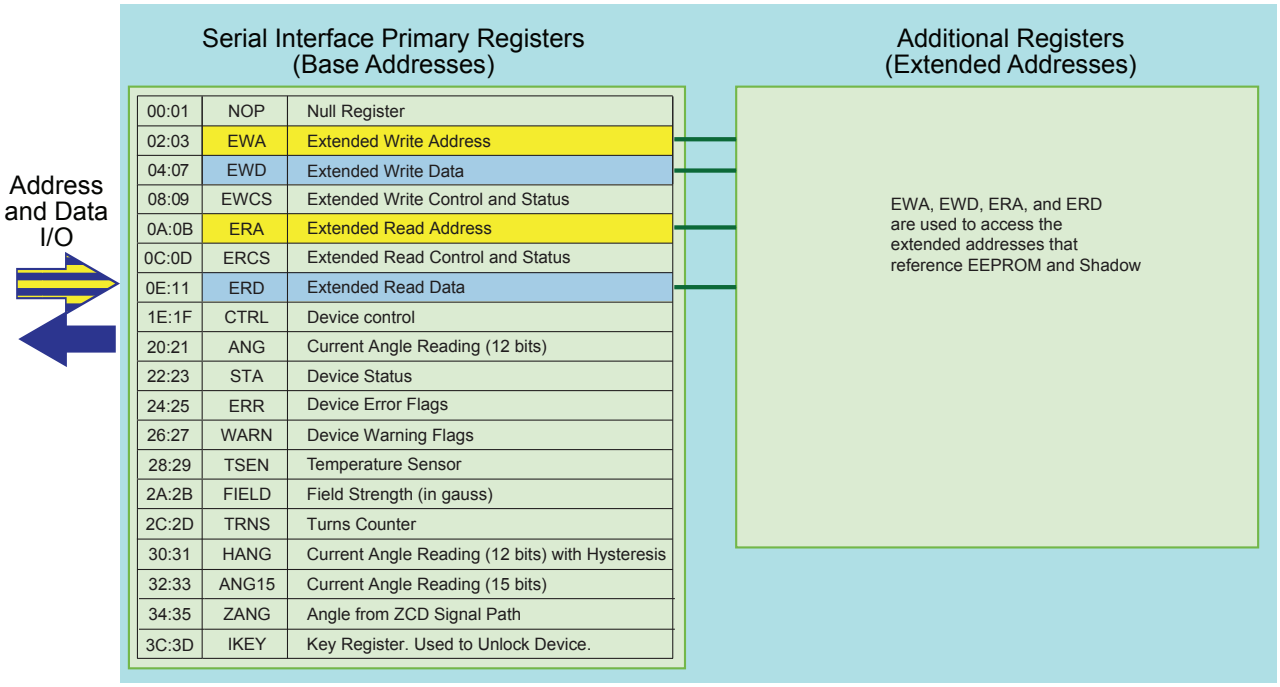
Interface Structure

The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information. All forms of communication operate through these registers, whether it be SPI or Manchester. These registers also provide a data and address location for accessing extended memory (EEPROM and Shadow).

Table 15: Primary Serial Interface Registers (Reserved Registers Not Shown)

Address* (Hex)	Name	Usage
00:01	NOP	Null Register
02:03	EWA	Extended Write Address
04:07	EWD	Extended Write Data
08:09	EWCS	Extended Write Control and Status
0A:0B	ERA	Extended Read Address
0C:0D	ERCS	Extended Read Control and Status
0E:11	ERD	Extended Read Data
12:1D	Unused	Unused
1E:1F	CTRL	Device Control
20:21	ANG	Current Angle reading (12 bits)
22:23	STA	Device Status
24:25	ERR	Device Error Flags
26:27	WARN	Device Warning Flags
28:29	TSEN	Temperature Sensor
2A:2B	FIELD	Field Strength (in Gauss)
2C:2D	TRNS	Turns Counter
2E:2F	Unused	Unused
30:31	HANG	Current Angle reading (12 bits), with hystersis
32:33	ANG15	Current Angle reading (15 bits)
34:35	ZANG	Angle from ZCD signal path
36:3B	Unused	Unused
3C:3D	IKEY	Key register. Used to unlock device

*Addresses that span multiple bytes are addressed by the most significant byte (lower address in the address range corresponds to the most significant byte).



00:01	NOP	Null Register
02:03	EWA	Extended Write Address
04:07	EWD	Extended Write Data
08:09	EWCS	Extended Write Control and Status
0A:0B	ERA	Extended Read Address
0C:0D	ERCS	Extended Read Control and Status
0E:11	ERD	Extended Read Data
1E:1F	CTRL	Device control
20:21	ANG	Current Angle Reading (12 bits)
22:23	STA	Device Status
24:25	ERR	Device Error Flags
26:27	WARN	Device Warning Flags
28:29	TSEN	Temperature Sensor
2A:2B	FIELD	Field Strength (in gauss)
2C:2D	TRNS	Turns Counter
30:31	HANG	Current Angle Reading (12 bits) with Hysteresis
32:33	ANG15	Current Angle Reading (15 bits)
34:35	ZANG	Angle from ZCD Signal Path
3C:3D	IKEY	Key Register. Used to Unlock Device.

Figure 31: Serial Registers allow access to extended memory (EEPROM and Shadow)

PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 16: Primary Serial Interface Registers Bits Map

Address* (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (MSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	nop	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x01
0x02	ewa	RW	0	0	0	0	0	0	0	0	write_adr								0x03
0x04	ewdh	RW	write_data_hi																0x05
0x06	ewdl	RW	write_data_lo																0x07
0x08	ewcs	WO/RO	exw	0	0	0	0	0	0	wip	0	0	0	0	0	0	0	wdn	0x09
0x0A	era	RW	0	0	0	0	0	0	0	0	read_adr								0x0B
0x0C	ercs	WO/RO	exr	0	0	0	0	0	0	rip	0	0	0	0	0	0	0	rdn	0x0D
0x0E	erdh	RO	read_data_hi																0x0F
0x10	erdl	RO	read_data_lo																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	ctrl	RW/WO	special				0	cls	clw	cle	initiate_special								0x1F
0x20	ang	RO	0	ef	uv	p	angle												0x21
0x22	sta	RO	1	0	0	0	0	0	dieid		rot	0	sdn	bdn	lbr	cstr	bip	aok	0x23
0x24	err	RO	1	0	1	0	war	stf	avg	abi	plk	zie	eue	ofe	uvd	uva	msl	rst	0x25
0x26	warn	RO	1	0	1	1	ier	crc	0	srw	xee	tr	ese	sat	tcw	bsy	msh	tov	0x27
0x28	tsen	RO	1	1	1	1	temperature												0x29
0x2A	field	RO	1	1	1	0	gauss												0x2B
0x2C	turns	RO	1	1	0	p	turns												0x2D
0x2E	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2F
0x30	hang	RO	0	ef	uv	p	angle_hys												0x31
0x32	ang15	RO	0	angle_15															0x33
0x34	zang	RO	0	ef	uv	p	angle_zcd												0x35
0x36 0x38 0x3A	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x37 0x39 0x3B
0x3C	ikey	WO/RO	keycode								0	0	0	0	0	0	0	cul	0x3D
0x3E	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x3F

*Addresses that span multiple bytes are addressed by the most significant byte.

Address 0x00:0x00 (NOP) – Null Register

Address	0x00								0x01							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address 0x02:0x03 (EWA) – Extended Write Address

Address	0x02								0x03							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	WRITE_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_ADDR[7:0]:

Address to be used for an extended write. Address ranges:
0x00 - 0x1F: EEPROM (requires ≈ 24 ms following execution of a write)
0x40 - 0x5F: Shadow

Address 0x04:0x05 (EWDH) – Extended Write Data High

Address	0x04								0x05							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRITE_DATA_HI															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_HI[15:0]:

Upper 16 bits of data for an extended write operation.

Address 0x06:0x07 (EWDL) – Extended Write Data Low

Address	0x06								0x07							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRITE_DATA_LO															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_LO[15:0]:

Lower 16 bits of data for an extended write operation.

Address 0x08:0x09 (EWCS) – Extended Write Control and Status

Address	0x08								0x09							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXW[15]:

Initiate extended write by writing with '1'. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP[8]:

Write in progress when '1' .

RDN[0]:

Write done when '1', clears when EXR set to '1'.

Address 0x0A:0x0B (ERA) – Extended Read Address

Address	0x0A								0x0B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	READ_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

READ_ADDR[7:0]:

Address to be used for an extended read. Address ranges:
0x00 - 0x1F: EEPROM (requires ≈2 µs)
0x40 - 0x5F: Shadow

Address 0x0C:0x0D (ERCS) – Extended Read Control and Status

Address	0x0C								0x0D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXR[15]:

Initiate extended read by writing with '1'. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP[8]:

Read in progress when '1' .

RDN[0]:

Read done when '1', clears when EXR set to '1'.

Address 0x0E:0x0F (ERDH) – Extended Read Data High

Address	0x0E								0x0F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	READ_DATA_HI															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_HI[15:0]:

Upper 16 bits of data from extended read operation, valid when ERCS. RDN set to '1' .

Address 0x10:0x11 (ERDL) – Extended Read Data Low

Address	0x10								0x11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	READ_DATA_LO															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_LO[15:0]:

Lower 16 bits of data from extended read operation, valid when ERCS. RDN set to '1'.

Address 0x1E:0x1F (CTRL) – Device Control

Address	0x1E								0x1F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPECIAL				0	CLS	CLW	CLE	INITIATE_SPECIAL							
R/W	R/W	R/W	R/W	R/W	R	R/W	W	W	W	W	W	W	W	W	W	W

SPECIAL[15:12]:

Defines specific actions to be taken by the IC. Many actions will only be invoked after the CTRL.INITIATE_SPECIAL field is written with the correct value. Aside from EEPROM margining, this field will return 0x00 on completion.

Value	Description
0000	No action.
0001	Enable EEPROM low voltage margin. IC must be unlocked. Initiate with 0xA5.
0010	Enable EEPROM high voltage margin. IC must be unlocked. Initiate with 0xA5.
0100	Turns counter reset. Initiate with 0x46.
0101	Reload EEPROM. Requires IC to be unlocked. Initiate with 0xA5.
0110	No action.
0111	Hard reset. Requires unlock of part. Initiate with 0xA5.
1001	Run CVH self-test. Initiate with 0xB9.
1010	Run Logic BIST. Initiate with 0xB9.
1011	Run both CVH self-test and Logic BIST. Tests are run in parallel. Initiate with 0xB9.

CLS[10]:

Clear Status register bits “SDN” and “BDN”, when set to “1”.
STA.SDN indicates that a “special access” task (i.e. CVH self-test) is completed.
STA.BDN indicates the IC has booted properly and completed any start-up self-tests.

CLW[9]:

Clear warning (WARN) register when set to “1”.
Clears bits that were previously read from the WARN (register 0x26:0x27).
Write-only, always returns 0.

CLE[8]:

Clear error (ERR) register when set to “1”.
Clears bits that were previously read from the ERR (register 0x24:25).
Write-only, always returns 0.

INITIATE_SPECIAL[7:0]:

Write after setting certain CTRL.SPECIAL bits to initiate the selected action(s).
Always returns 0’s.

Value	Description
0xB9	Initiate self-tests.
0x46	Initiate turns counter reset.
0x5A	Initiate hard reset.
0xA5	Initiate EEPROM margin or reload.

Address 0x20:0x21 (ANG) – Current Angle Reading (12 bits)

Address	0x20								0x21							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF[14]:

Error Flag. Will be “1” if any unmasked bit in ERR or WARN is set.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV[13]:

Undervoltage Flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are realtime, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P[12]:

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE). Result is that there should always be an odd number of 1’s in this 16 bit word.

ANGLE[11:0]:

Angle from PLL after processing.
Angle in degrees is 12-bit value × (360/4096).

Address 0x22:0x23 (STA) – Device Status

Address	0x22								0x23							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	0	0	0	0	DIE_ID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:12]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1000	Register ID value

DIE_ID[9:8]:

DIE ID, loaded from EEPROM (for multi-die packages). Used for identification purposes only. No impact on sensor functionality. Set in factory by Allegro.

ROT[7]:

Indicates observed rotation direction, based on the hysteresis logic. Valid only if Hysteresis is enabled (see EEPROM 0x1C).

Value	Description
0	Increasing angles
1	Decreasing angles

SDN[5]:

Special access (from CTRL register) done. Clears to 0 when a “special command” is triggered, set 1 when complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	“Special” command in progress, unless cleared previously
1	“Special” command completed

BDN[4]:

Boot complete. EEPROM loaded and any startup self-tests are complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	Boot not complete, unless cleared previously.
1	Boot complete

LBR[3]:

Logic BIST (LBIST) running.

Value	Description
0	LBIST not running
1	LBIST running

CSTR[2]:

CVH Self-test running.

Value	Description
0	CVH self-test not running
1	CVH self-test running

BIP[1]:

Boot in progress. Output values may not be valid.

Value	Description
0	Boot not in progress
1	Sensor is undergoing its boot sequence

AOK[0]:

Angle output is OK. Indicates the PLL is locked and stat-up sequence has completed.

Value	Description
0	Angle is not valid
1	PLL is locked, angle value is valid

Address 0x24:0x25 (ERR) – Device Error Flags

This is the error register. All errors are latched, meaning they will remain high after they occurred. Errors need to be read and then cleared in order to remove them. It is important that the user clears errors so that subsequent errors become visible. This is especially important for the “RST” error flag (reset), which is always enabled after power on. Not removing it means that an unexpected reset cannot be discovered afterwards.

Address	0x24								0x25							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	1	0	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:12]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1010	Register ID value

WAR[11]:

Warning. An unmasked bit within the WARN register is asserted. May be masked by setting MSK.WAR bit in EEPROM.

Value	Description
0	No unmasked flag set in the WARN register (0x26:27)
1	Unmasked flag set in the WARN register

STF[10]:

Self-test failure. Indicates either LBIST or CVH self-test failed.

Value	Description
0	No self-test failure
1	Self-test failure

AVG[9]:

Angle averaging error. Indicates the ORATE value is too high for the rotation velocity, and the averaged angle value is corrupted.
The ORATE setting allows multiple angle values to be averaged together, for improved precision. This reduces the response time of the sensor, and can result in corrupted angle values is the velocity is too high.

Value	Description
0	No Averaging error
1	Averaging error

ABI[8]:

ABI integrity fault. The quadrature integrity of the ABI could not be maintained.

Value	Description
0	No ABI integrity fault
1	ABI integrity fault

PLK[7]:

PLL lost lock. This indicates the PLL is not tracking the incoming angle properly. Angle value is corrupt.

Value	Description
0	No PLL lock.
1	PLL lost lock. Angle value invalid.

ZIE[6]:

Zero crossing integrity error—a zero crossing did not occur within the maximum time expected, likely indicating missing magnet, or extreme rotation.

Value	Description
0	No Zero crossing error
1	Zero crossing error

EUE[5]:

EEPROM uncorrectable error. A multi-bit EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (i.e. power-up or reset).

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

OFE[4]:

Oscillator Frequency Error. One of the oscillator watchdogs circuits, monitoring the high frequency and low frequency oscillators has tripped.

Value	Description
0	No oscillator error
1	Oscillator watchdog error

UVD[3]:

VCC Undervoltage detector tripped. Will continue to set until fault goes away (and ERR register is cleared). This is the VCC input pin voltage.

Value	Description
0	No VCC voltage error
1	VCC undervoltage error detected

UVA[2]:

Undervoltage detector tripped. Will continue to set until fault goes away (and ERR register is cleared). This is the analog regulator output.

Value	Description
0	No voltage error
1	Voltage error on the analog regulator output

MSL[1]:

Magnetic sense low fault. Magnetic sense was below the low limit threshold.
Low limit threshold is set via the COM.MAG_THRES_LO field in EEPROM.
By default this is set to ≈200 G.

Value	Description
0	No magnetic field low fault
1	Magnetic field lower than threshold

RST[0]:

Reset condition. Sets on power-on reset or hard reset. Does not set on LBIST. Indicates volatile registers have been re-initialized.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are re-initialized.

Address 0x26:0x27 (WARN) – Device Warning Flags

This is the warning register. All warnings are latched, meaning they will remain high after they occurred. Warnings need to be read and then cleared in order to remove them. Warnings indicate either communication type conditions or conditions that may result in a degradation of the angle accuracy, but are less likely than errors to indicate a corruption of the angle.

Address	0x26								0x27							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	1	1	IER	CRC	0	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:12]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1011	Register ID value

IER[11]:

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = '1'. Packet was discarded.
Also indicates a Manchester error.

Value	Description
0	No Interface Error
1	Interface Error

CRC[10]:

Incoming SPI CRC error. Packet was discarded.
Incoming CRC is only checked if the PWI.SC bit in EEPROM is set.

Value	Description
0	No incoming SPI CRC error
1	Incoming SPI CRC is bad

SRW[8]:

Slew rate warning. This warning is asserted if the ABI slew rate limiting is enabled and a condition that requires the limiting to be applied has occurred.
Purpose of Slew Rate Limiting is to prevent an ABI integrity error.

Value	Description
0	Slew rate limiting is not active.
1	Slew rate limiting is active. ABI output is incrementing at the designated slew rate.

XEE[7]:

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute Error

TR[6]:

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature will saturate at those limits.

Value	Description
0	Temperature sensor in range
1	Sensed temperature is below -60° or above 180°C

ESE[5]:

EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset).

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error detected and corrected

SAT[4]:

Aggregate saturation flag. Shows that any internal signals have saturated, likely to have been cause by extremely strong or weak fields.

Value	Description
0	No saturation detected within the signal chain.
1	Saturation conditions detected within the signal chain.

TCW[3]:

Turns counter warning. Over 135° of angle change between turns count updates.

Value	Description
0	No turns count warning
1	Angle difference between two successive samples

BSY[2]:

Extended access overflow. An Extended write or Extended read was initiated before previous was done.

Value	Description
0	No extended access error
1	extended access error

MSH[1]:

Magnetic sense high fault. Magnetic sense was above the high limit threshold.
High limit threshold is set via the COM.MAG_THRES_HI field in EEPROM.
By default this is set to ≈1200 G.

Value	Description
0	No magnetic field high fault
1	Magnetic field above threshold

TOV[0]:

Turns Counter Overflow Error.
The turns counter surpassed its maximum value of +255/-256 full rotations.
This is equivalent to an Turns register value of ±511/-512 or +2047/-2048, depending on the resolution (180° or 45°).
Must be cleared with a turns count reset (See special commands in the CTRL register description, 0x1E).

Value	Description
0	No turns count overflow error
1	Turns count overflow error

Address 0x28:0x29 (TSEN) – Temperature Sensor

Address	0x28								0x29							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	1	TEMPERATURE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:12]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1111	Register ID value

TEMPERATURE[11:0]:

Current junction temperature from internal temperature sensor relative to room temperature (signed value, 2's complement). Value is in 1/8 of a degree. Temperature °C ≈ (TSEN.TEMPERATURE / 8) + 25.0.

Address 0x2A:0x2B (FIELD) – Field Strength (in gauss)

Address	0x2A								0x2B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	0	GAUSS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:12]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1110	Register ID value

GAUSS [11:0]:

Measured field strength in gauss. Updated every 128 µs.

Address 0x2C:0x2D (TURNS) – Turns Counter

Address	0x0C								0x0D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	0	P	TURNS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC[15:13]:

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
110	Register ID value

P[12]:

Parity bit. Odd parity is calculated across all bits. Result is that there should always be an odd number of 1's in this 16-bit word.

TURNS [11:0]:

Signed 2's complement value. Indicates total number of turns relative to angle observed on power-up. Turns resolution set via EEPROM to either 180° or 45°.
The A1333 is capable of tracking up to 256 full mechanical rotations, independent of the resolution selected.

Bit Value	Turns in 180° mode (Actual mechanical full rotations)	Turns in 45° mode (Actual mechanical full rotations)
0000 0000 0000	0 (0)	0 (0)
0000 0000 0001	+1 (+1/2)	+1 (+1/8)
0001 1111 1111	+511 (255.5)	+511 (+63.875)
0010 0000 0000	N/A	+512 (+64)
0111 1111 1111	N/A	+2047(+255.875)
1111 1111 1111	-1 (-1/2)	-1 (-1/8th)
1110 0000 0000	-512 (-256)	-512 (-64)
1000 0000 0000	N/A	-2048 (-256)

Address 0x30:0x31 (HANG) – Hysteresis Angle Value (12 bits)

Address	0x30								0x31							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_HYS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF[14]:

Error Flag. Will be “1” if any unmasked bit in ERR or WARN is set.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV[13]:

Undervoltage Flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are realtime, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P[12]:

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_HYS). Result is that there should always be an odd number of 1’s in this 16 bit word.

ANGLE_HYS[11:0]:

Angle from PLL after hysteresis processing.
Angle in degrees is 12-bit value × (360/4096).

Address 0x32:0x33 (ANG15) – Current Angle Reading (15 bits)

Address	0x32								0x33							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	ANGLE_15														
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_15[14:0]:

15-bit compensated angle (not rounded).
Angle in degrees is a 15-bit value × (360/32768)

Address 0x34:0x35 (ZANG) – ZCD Angle

Angle from the ZCD signal path is used for turns counting. This angle is not compensated over temperature and will not exactly match the PLL angle value.

Address	0x34								0x35							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_ZCD											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF[14]:

Error Flag. Will be “1” if any unmasked bit in ERR or WARN is set.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV[13]:

Undervoltage Flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are realtime, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P[12]:

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_ZCD). Result is that there should always be an odd number of 1’s in this 16 bit word.

ANGLE_ZCD[11:0]:

Angle from the ZCD signal path. Not compensated.
Angle in degrees is 12-bit value × (360/4096).

Address 0x3C:0x3D (KEY) – Key Register

Address	0x3C								0x3D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYCODE								0	0	0	0	0	0	0	CUL
R/W	W	W	W	W	W	W	W	W	R	R	R	R	R	R	R	R

KEYCODE[15:8]:

Unlock code is entered here. Once unlocked EEPROM and Shadow registers may be written. In addition some “special” commands require a device unlock.
Unlocking requires five successive writes to the KEYCODE field, following the unlock sequence shown below.
The CUL indicates a successful unlock.

Write #	Code
1	0x00
2	0x27
3	0x81
4	0x1F
5	0x77

CUL[0]:

Indicates the device is unlocked.

Value	Description
0	Device is not unlocked
1	Device is unlocked

EEPROM/SHADOW MEMORY TABLE

The EEPROM/Shadow register bitmap is shown below.

All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires device unlock.

Table 17: EEPROM / Shadow Memory Map

EEPROM Address	Shadow Memory Address	Register Name	Bits																										
			31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x18	0x58	PWE	ECC	–	–	–	–	–	–	–	–	–	–	–	–	–	TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
0x19	0x59	ABI	ECC	–	–	–	–	ABI_SLEW_TIME						INV	-X-	-X-	AHE	–	–	INDEX_MODE		WDH	PLH	IOE	UVW	RESOLUTION_PAIRS			
0x1A	0x5A	MSK	ECC	–	–	IER	CRC	-X-	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
0x1B	0x5B	PWI	ECC	–	–	PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	–	–	–	–	–	–	–	–	DM	–	S17	SC
0x1C	0x5C	ANG	ECC	–	–	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
0x1D	0x5D	LPC	ECC	–	–	T45	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
0x1E	0x5E	COM	ECC	–	–	LOCK				LBE	CSE	–	–	–	–	DST	DHR	MAG_THRES_HI						MAG_THRES_LO					
0x1F	–	CUS	ECC	–	–	Customer EEPROM Space																							

Address 0x18 (PWE) – PWM Error Enable

This address space contains the PWM error enable bits. When set to "1", the PWM output will respond to errors, as set via the PWI.PEO and PWI.PES bits.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–	–	–	–	TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
Default	–	–	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0	0	0	0	0	0	0

TOV[12]:

PWM turns counter overflow error enable.
Duty cycle 72.5%, if PWI.PEO and PWI.PES are "1".

Value	Description
0	PWM does not respond to a TOV error
1	PWM output respond to a TOV error

MSH[10]:

PWM magnetic sense high error enable.
Duty cycle 61.25%, if PWI.PEO and PWI.PES are "1".

Value	Description
0	PWM does not respond to a MSH error
1	PWM output respond to a MSH error

TR[11]:

PWM Temperature out of range error enable.
Duty cycle 66.875%, if PWI.PEO and PWI.PES are "1".

Value	Description
0	PWM does not respond to a TR error
1	PWM output respond to a TR error

SAT[9]:

PWM saturation error enable.
Duty cycle 55.625%, if PWI.PEO and PWI.PES are "1".

Value	Description
0	PWM does not respond to a SAT error
1	PWM output respond to a SAT error

ESE[8]:

PWM EEPROM soft error enable.
Duty cycle 50%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a ESE error
1	PWM output respond to a ESE error

MSL[7]:

PWM magnetic sense low error enable.
Duty cycle 44.375%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a MSL error
1	PWM output respond to a MSL error

UV[6]:

PWM undervoltage error enable.
Duty cycle 38.75%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to an UV error
1	PWM output respond to a UV error

AVG[5]:

PWM averaging error enable.
Duty cycle 33.125%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a AVG error
1	PWM output respond to a AVG error

ZIE[4]:

PWM zero crossing error enable.
Duty cycle 27.5%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a ZIE error
1	PWM output respond to a ZIE error

PLK[3]:

PWM PLL lost lock error enable.
Duty cycle 21.875%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a PLK error
1	PWM output respond to a PLK error

STF[2]:

PWM Self test error enable.
Duty cycle 16.25%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a STF error
1	PWM output respond to a STF error

EUE[1]:

PWM EEPROM uncorrectable error enable.
Duty cycle 10.625%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a EUE error
1	PWM output respond to a EUE error

OFE[0]:

PWM Oscillator frequency error enable.
Duty cycle 5%, if PWI.PEO and PWI.PES are “1”.

Value	Description
0	PWM does not respond to a OFE error
1	PWM output respond to a OFE error

Address 0x19(ABI) – ABI Control

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	ABI_SLEW_TIME						INV	-X-	-X-	AHE	–	–	INDEX_MODE		WDH	PLH	IOE	UVW	RESOLUTION_PAIRS			
Default	–	–	0	0	1	0	0	0	0	–	–	1	0	0	0	0	0	0	1	0	0	1	0	0

ABI_SLEW_TIME[20:16]:

ABI slew time rate. “0” disables slew limiting.
Minimum edged-to-edge time for ABI output is defined by:

$$(N + 1) \times 125\ ns$$

where “N” is the value of ABI_SLEW_TIME.
This limits the maximum ABI velocity. Reducing the ABI resolution can be used to counteract this.

Value	Description
00 0000	Slew limiting disable
00 0001	250 ns of slew control
…	…
11 1111	8 µs of slew control

INV[15]:

Invert ABI/UVW signals.

Value	Description
0	ABI/UVW signals behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Value	Description
1	ABI/UVW signals are inverted and behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	1	1
Q2	1	0
Q3	0	0
Q4	0	1

AHE[12]:

ABI hysteresis enable. When “1” hysteresis is applied to the ABI angle.

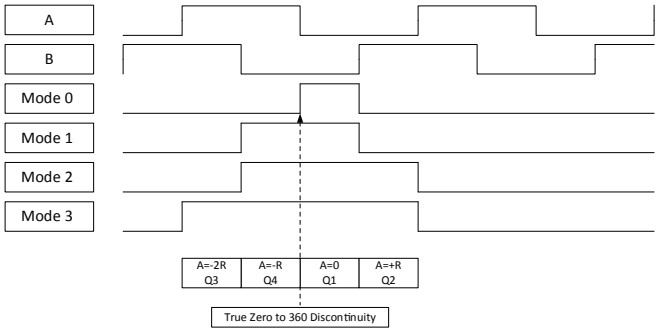
Value	Description
0	Hysteresis is not applied to ABI
1	Hysteresis applied to ABI outputs

INDEX_MODE[9:8]:

Defines the width and placement of the “I” pulse in ABI.

Value	Description
0	“I” pulse is set only at 0° to +R
1	“I” pulse set between –R to +R
2	“I” pulse set between –R to +2R
3	“I” pulse set between -2R and +2R

“R” indicates the ABI quadrature resolution.



WDH[7]:

Enable ABI all high (before inversion) as error mode if oscillator frequency watchdog error trips.

Value	Description
0	ABI pins do not respond to an OFE Flag
1	ABI outputs go high if an OFE is detected

PLH[6]:

Enable ABI all high (before inversion) as error mode if a PLL loss of lock is detected.

Value	Description
0	ABI pins do not respond to an PLK Flag
1	ABI outputs go high if the PLK flag is set

IOE[5]:

Incremental output enable.

Value	Description
0	ABI/UVW pins are not active
1	ABI/UVW pins are active. Behavior defined by ABI.UVW bit

UVW[4]:

Define behavior of the ABI/UVW pins. If ABI.IOE = 1.

Value	Description
0	ABI active
1	UVW active

RESOLUTION_PAIRS[3:0]:

Defines resolution of ABI/UVW outputs.
In ABI mode, cycle resolution = $2^{(14-n)}$ where “n” is the RESOLUTION_PAIRS value.
In UVW mode, the number of pole pairs is n + 1.

Value	AB Cycles per Rev	UVW Pole Pairs
0000	N/A	1
0001	N/A	2
0010	N/A	3
0011	2^{11} = 2048	4
0100	2^{10} = 1024	5
…	…	…
1110	2^{0} = 1	15
1111	N/A	16

Address 0x1A (MSK) – Mask Bits

This address range contains error mask bits. When set, the applicable error condition will not assert the “EF” bit in the various angle and turns count registers.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	CRC	-X-	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
Default	0	0	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IER[23]:
Masks the IER flag from setting the “EF” bit.

CRC[22]:
Masks the CRC flag from setting the “EF” bit.

SRW[20]:
Masks the SRW flag from setting the “EF” bit.

XEE[19]:
Masks the XEE flag from setting the “EF” bit.

TR[18]:
Masks the TR flag from setting the “EF” bit.

ESE[17]:
Masks the ESE flag from setting the “EF” bit.

SAT[16]:
Masks the SAT flag from setting the “EF” bit.

TCW[15]:
Masks the TCW flag from setting the “EF” bit.

BSY[14]:
Masks the BSY flag from setting the “EF” bit.

MSH[13]:
Masks the MSH flag from setting the “EF” bit.

TOV[12]:
Masks the TOV flag from setting the “EF” bit.

WAR[11]:
Masks the WAR flag from setting the “EF” bit.

STF[10]:
Masks the STF flag from setting the “EF” bit.

AVG[9]:
Masks the AVG flag from setting the “EF” bit.

ABI[8]:
Masks the ABI flag from setting the “EF” bit.

PLK[7]:
Masks the PLK flag from setting the “EF” bit.

ZIE[6]:
Masks the ZIE flag from setting the “EF” bit.

EUE[5]:
Masks the EUE flag from setting the “EF” bit.

OFE[4]:
Masks the OFE flag from setting the “EF” bit.

UVD[3]:
Masks the UVD flag from setting the “EF” bit.

UVA[2]:
Masks the UVA flag from setting the “EF” bit.

MSL[1]:
Masks the MSL flag from setting the “EF” bit.

RST[0]:
Masks the RST flag from setting the “EF” bit.

Address 0x1B (PWI) – PWM Interface Control

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	–	–	–	–	–	–	–	–	DM	–	S17	SC
Default	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

PEN[23]:

PWM Enable.

Value	Description
0	PWM pin tri-stated
1	PWM enabled

PWM_BAND[22:20]:

PWM frequency band. Defines the PWM carrier frequency when combined with PWM_FREQ.

PWM_FREQ[19:16]:

PWM frequency select. Defines the PWM carrier frequency when combined with PWM_BAND.

Table 18: Nominal PWM Carrier Frequencies

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

PHE[14]:

PWM Hysteresis enable.

Value	Description
0	No hysteresis applied to PWM output
1	Hysteresis settings applied to PWM output

PEO[13]:

PWM Error Output Enable. If “1” PWM will respond to errors, as defined by the PES bit.

Value	Description
0	PWM output does not respond to error flags
1	PWM output will respond to errors, as defined by the PWI. PES field.

PES[12]:

PWM Error Select, if PEO = 1.

Value	Description
0	PWM output tri-states for all enabled error conditions (See PWE address space).
1	For all enabled errors the PWM carrier frequency is halved and the highest priority error is identified by a specific duty cycle. See the PWE address space description.

DM[3]:

Disable Manchester Interface.

Value	Description
0	Manchester functions normally
1	A1333 will no longer respond to Manchester command on the V_{CC} line

S17[1]:

A1333 ignores the 17th SPI clock. Allows negative edge sampling at the MCU (host).

SC[0]:

A1333 monitors the incoming CRC.

Value	Description
0	No monitoring of the incoming CRC
1	A1333 monitors incoming CRC. Discards packet if corrupt.

Address 0x1C (ANG)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
Default	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ORATE[23:20]:

Reduces the output rate by averaging samples. 2^{ORATE} samples will be averaged. ORATE values above 12 are reduced to 12 in the logic, meaning that up to 4096 samples = 4 ms can be selected as averaging time.

Value	Description
0000	1 sample. 1 µs update rate.
0001	2 samples. 2 µs update rate.
0010	4 samples. 4 µs update rate.
…	…
1100	4096 samples. ≈4 ms update rate.

RD[19]:

Rotates die. Rotates final angle 180°. Last step in the angle algorithm. This is a convenient setting to adjust one die in a dual die package for conformance to the other die. Occurs after the Zero_offset and RO adjustments.

Value	Description
0	No rotation applied
1	180° added to final angle

RO[18]:

Rotation Direction. If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction. Occurs after the Zero_offset adjust and prior to the RD manipulation.

Value	Description
0	Output angle increases with a clockwise rotation (when viewed from above the magnet and device)
1	Output angle increases with a counter-clockwise rotation (when viewed from above the magnet and device)

HYSTERESIS[17:12]:

Angle Hysteresis threshold. In 14bit resolution. Provides ≈0 to 1.384° of hysteresis.

Value	Description
00 0000	No Hysteresis
00 0001	≈0.022° of Hysteresis
…	…
11 1111	≈1.384° of Hysteresis

ZERO_OFFSET[11:0]:

Post-compensation zero offset (or DC adjust), at 12-bit resolution. This value is subtracted from the measured angle value. Operation occurs prior to the RD and RO manipulations.

Address 0x1D (LPC)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	T45	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Default	1	–	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1	1	1	1

T45[23]:

Defines the resolution of the turns counter.

Value	Description
0	Turns counter measures 180° of rotation
1	Turns counter measures 45° of rotation

Address 0x1E (COM)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK				LBE	CSE	–	–	–	–	DST	DHR	MAG_THRES_HI						MAG_THRES_LO					
Default	0	0	0	0	1	1	–	–	–	–	0	0	1	0	0	1	0	1	0	0	1	1	0	1

LOCK[23:20]:

EEPROM and Shadow memory lock.
Permanent lock.

Value	Description
1100	Writing to EEPROM is locked
0011	Writing to EEPROM and Shadow memory is locked

LBE[19]:

Power-up Logic BIST enable.
LBIST requires ≈30 ms to run.

Value	Description
0	LBIST isn't run on power-up
1	LBIST is run on power-up

LBIST and CVH self-test are run in parallel. Therefore if both are enabled on power-up, power-on time is ≈30 ms.

CSE[18]:

Power-up CVH self-test enable.
CVH self-test requires ≈30 ms to run.

Value	Description
0	CVH is not run on power-up
1	CVH is run on power-up

LBIST and CVH self-test are run in parallel. Therefore, if both are enabled on power-up, power-on time is ≈30 ms.

DST[13]:

Disable Self-test initiation from the serial register.

Value	Description
0	Self-tests may be initiated via a "special" serial register command.
1	Prevents running either LBIST or CVH self-test from the CTRL register.

DHR[12]:

Disable Hard reset from the serial register.

Value	Description
0	A Hard reset may be initiated via a "special" serial register command.
1	Prevents initiating a Hard reset from the CTRL register.

MAG_THRES_HI[11:6]:

Magnetic threshold high value. Determine set-point of the MSH flag. When set to 0, check is disabled.
Limit increases in 32 G increments.

Value	Description
00 0000	High field flag disabled
00 0001	32 G
00 0010	64 G
…	…
10 0101	1184 G
…	…
11 1111	2016 G

MAG_THRES_LO[5:0]:

Magnetic threshold low value. Determine set-point of the MSL flag. When set to 0, check is disabled.
Limit increased in 16 G increments.

Value	Description
00 0000	Low field flag disabled
00 0001	16 G
00 0010	32 G
…	…
00 1101	208 G
…	…
11 1111	1008 G

Address 0x1F (CUST)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Customer EEPROM Space																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CUSTOMER[23:0]:

Customer EEPROM space.

SAFETY AND DIAGNOSTICS

The A1333 was developed in accordance with the ASIL design flow (ISO 26262) and incorporates several internal diagnostics as well as error/warning/status flags enabling the host microntroller to assess the operational status of the die.

A short summary of the A1333 diagnostics is provided below. A complete listing and discussion of the A1333 safety features may be found in the "A1333 Safety Manual", which is available upon request.

Built-In Self-Tests

The A1333 features two built-in-self-tests (BISTS) which may be configured to run at power-up and may also be initiated at any time by the system microcontroller via a serial register write. A failure of any one of the self-tests will assert the Self-Test Failure Flag, STF, within the Error register.

CVH SELF-TEST

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and for integration debug. The CVH self-test is implemented by changing the switch configuration from the normal operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device.

CVH self-test typically takes 30 ms to run (when run in parallel with LBIST, entire test time is 30 ms).

LOGIC BUILT-IN SELF-TEST (LBIST)

Logic BIST is implemented to verify the integrity of the A1333 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudo-random data. The output of the scan chains are fed back into a multiple input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST takes ≈30 ms to complete (when run in parallel with CHV self-test, the entire test time is ≈30 ms).

Status, Error, and Warning Flags

The A1333 features many flags used to detect faulty external or internal conditions. Table 19 briefly describes a selection.

All flags may be read through the serial registers via SPI or Manchester communication. All unmasked error flags will assert the "General Error" flag which is included in the angle register (0x20), providing a "snapshot" of the sensor's status.

Error reporting when using PWM or ABI is more limited and discussed later on.

Table 19: Status and Error Flags

Fault Condition	Description	Sensor Response
$V_{CC} < V_{UVD}$	Indicates V_{CC} is below expected level.	UVD flag set in ERR register UV flag set in ANG register EF flag set in ANG register
Field > High Threshold	Sensor monitors field level in case of mechanical failure. High Level is programmable from 0-2016 G in 32 G steps.	MSH flag set in WARN register EF flag set in ANG register
Field < Low Threshold	Sensor monitors field level in case of mechanical failure. Low Level is programmable from 0-1008 G in 16 G steps.	MSL flag set in ERR register EF flag set in ANG register
$T_A < –60°C$ or $T_A > 180°C$	Ambient temperature beyond maximum detectable value.	TR flag set in WARN register EF flag set in ANG register
Oscillator Frequency Discrepancy	The A1333 cross-checks the high and low frequency oscillators for proper functionality.	OFE flag set in ERR register EF flag set in ANG register
Single Bit EEPROM Error (correctable)	Detects and corrects single bit EEPROM errors.	ESE bit set in WARN register EF flag set in ANG register
Multi-Bit EEPROM failure (uncorrectable)	Detects multi-bit EEPROM errors.	EUE bit set in ERR register EF flag set in ANG register
Signal Path Failure	Multiple comparisons and checks within the signal path: • Main signal path output compared to the ZCD signal path • PLL lock status monitored • Main signal path is checked for saturation	PLK or ZIE set within the ERR register EF flag set within the ANG register
Loss of V_{CC}	Determines if system power was lost. Indicates all volatile registers have been reset (such as turns count).	RST bit set in ERR register EF flag set in ANG register
ABI Integrity Fault	Excessive noise or excessive rotational velocity for a given ABI resolution. IC monitors state of ABI and flags skipped states.	ABI bit set in ERR register EF flag set in ANG register
Analog regulator drift	IC monitors output of analog regulator, ensuring transducer is supplied with proper voltage.	UVA bit set in ERR register UV flag set in ANG register EF flag set in ANG register
Excessive magnet travel	Sensor detects when > 256 rotations have occurred, indicating the turns counter has saturated.	TOV bit set in WARN register EF flag set in ANG register
Excessive magnet velocity for turns counting	If the sensor detects > 135° travel between successive turns count updates.	TCW bit set in WARN register EF flag set in ANG register
Excessive magnet velocity for a given ORATE setting	Indicates the angle reading spanned more than 2 quadrants during the ORATE sample period, therefore the average may be incorrect. Can occur under extreme velocity and high averaging, or with no magnetic field and the samples out of the CVH are random.	AVG bit set in ERR register EF flag set in the ANG register
Incoming SPI Packet Corruption	IER error detects an invalid number of SCLKs, or a ‘1’ in the MSB on MOSI. If using 20-bit SPI packets and incoming CRC validation is enabled (SC bit in EEPROM 0x1B), the CRC flag will assert.	Depending on implementation and amount of corruption: IER bit set in WARN register CRC bit set in WARN register EF flag set in ANG register

ERROR REPORTING IN PWM

The PWM output can be configured to change state if certain errors occur. There are three options:

- No error reporting
- Tristate the PWM
- Halve the carrier frequency and represent the error via different duty cycles

Two EEPROM bits, “PEO” and “PES” control how errors are reported in PWM mode, both of which are in the PWS address row of EEPROM:

Table 20: PWM Error Output Enable Option (PEO)

Code	Description
0	PWM does not respond to errors.
1	PWM output responds to errors as selected with the PES field.

Table 21: PWM Error Select (PES)

Code	Description
0	PWM tristates on an error.
1	PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

The error priority and corresponding duty cycle are shown in Table 22 below, with the high priority error dictating the PWM duty cycle.

Each error code must be enabled via EEPROM. This prevents losing the PWM output due to a spurious error.

The enable bits can be found within the PWE (0x18) EEPROM row.

Table 22: PWM Error Duty Cycle and Priority

Error	Priority	Duty Cycle %	Description / Persistence
OFE	1 (highest)	5	Watchdog error. Permanent.
EUE	2	10.625	EEPROM uncorrectable error. Permanent.
STF	3	16.25	Self-test failure. Permanent.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists until goes away.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength higher than low threshold.
ESE	9	50	EEPROM correctable error. Outputs once then clears.
SAT	10	55.625	Persists until no saturation warnings.
MSH	11	61.25	Persists until field strength lower than high threshold.
TR	12	66.875	Persists until temperature within range.
TOV	13 (lowest)	72.5	Turns counter overflow. Persists until cleared via CTRL register.

ERROR REPORTING IN ABI/UVW

Error reporting when using ABI/UVW requires the transmission of angle information to be interrupted. As a result, only the two most severe errors are allowed to interrupt the pulse stream, preventing potential spurious errors from interrupting the primary mission of the IC.

As further insurance against undesired ABI/UVW interruption, error reporting must be individually enabled in EEPROM. The error conditions which may be reported are:

- Oscillator Frequency Error
- PLL Loss of Lock Error

When enabled, and an error occurs, all three ABI lines will be brought high (prior to inversion, if enabled). This is an undefined state in both ABI (if using default I mode width) and UVW.

Error reporting is enabled via the following two EEPROM bits, housed within address row 0x19.

WDH[7]:

Enable ABI all high (before inversion) as error mode if oscillator frequency watchdog error trips.

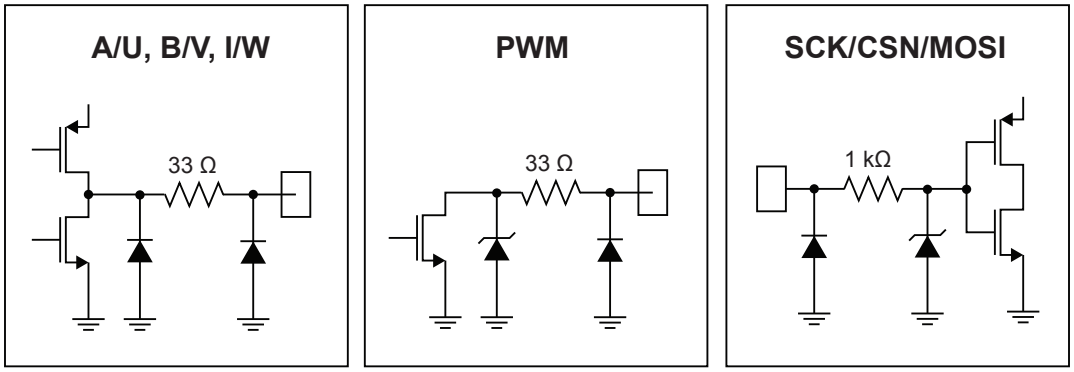
Value	Description
0	ABI pins do not respond to an OFE Flag
1	ABI outputs go high if an OFE is detected

PLH[6]:

Enable ABI all high (before inversion) as error mode if a PLL loss of lock is detected.

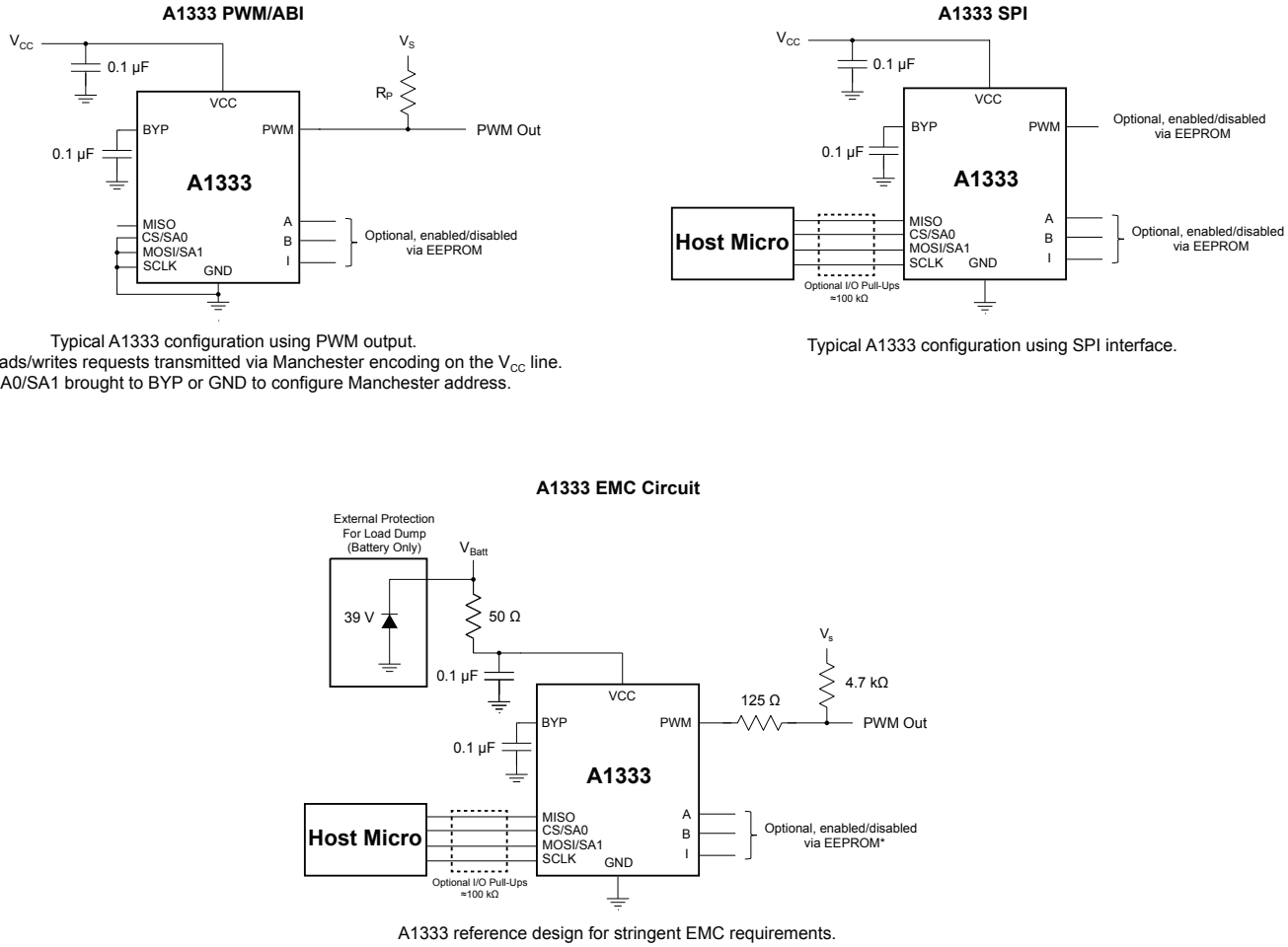
Value	Description
0	ABI pins do not respond to an PLK Flag
1	ABI outputs go high if the PLK flag is set

I/O STRUCTURES



APPLICATION INFORMATION

The A1333 features SPI, PWM, ABI/UVW, and Manchester outputs. Basic reference circuits for connecting the A1333 are shown below in Figure 32.



Typical A1333 configuration using PWM output.
Digital reads/writes requests transmitted via Manchester encoding on the V_{CC} line.
SA0/SA1 brought to BYP or GND to configure Manchester address.

Typical A1333 configuration using SPI interface.

A1333 reference design for stringent EMC requirements.
*If using ABI outputs, a 10 nF capacitor to GND on each line is recommended (this added capacitance will reduce the edge rates on ABI).

Figure 32: A1333 PWM/ABI, SPI, and EMC Application Circuits

ESD Performance

Under certain conditions, the ESD rating of the dual die IC may be less than 2 kV if ground pins are not tied together. Contact Allegro for questions regarding ESD optimization.

Table 23: HBM ESD Rating (per AEC-Q100 002)

Package	ESD Rating
TSSOP-14	5 kV
eTSSOP-24	4 kV [1]

[1] All GND pins shorted together.

Setting the Zero-Degree Position

When shipped from the factory, the default angle value when oriented as shown in Figure 33 is 0° for both die. In some cases, the end user may want to program an angle offset in the A1333 to compensate for variations in magnetic assemblies, or for applications where absolute system-level readings are required.

The internal algorithm for computing the output angle is as follows:

$$Angle_{out} = Angle_{RAW} - ZERO\_OFFSET$$

where ZERO_OFFSET is a 12-bit field in EEPROM.

To "zero out" the A1333 reported angle, during final application calibration, position the magnet above the A1333 in the desired zero-degree position and read the reported angle. This angle becomes the necessary ZERO_OFFSET value to "zero-out" the angle.

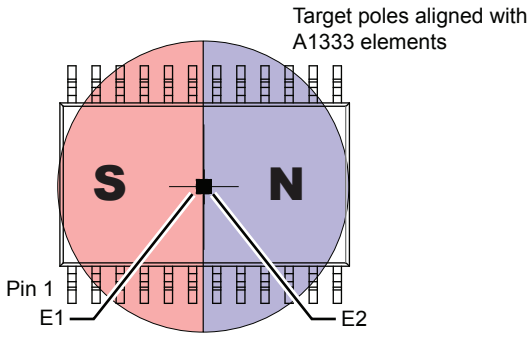


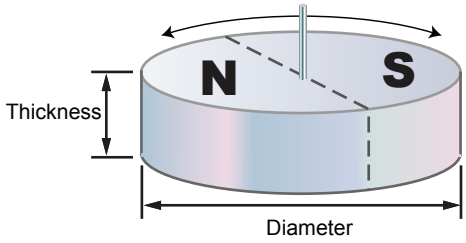
Figure 33: Orientation of Magnet Relative to Primary and Secondary Die

Magnetic Target Requirements

The A1333 is designed to operate with magnets constructed with a variety of magnetic materials, geometries, and field strengths. See Table 24 for a list of common magnet dimensions.

Table 24: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (sintered)*	10	2.5
Neodymium (sintered)	8	3
Neodymium / SmCo	6	2.5



* A sintered Neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

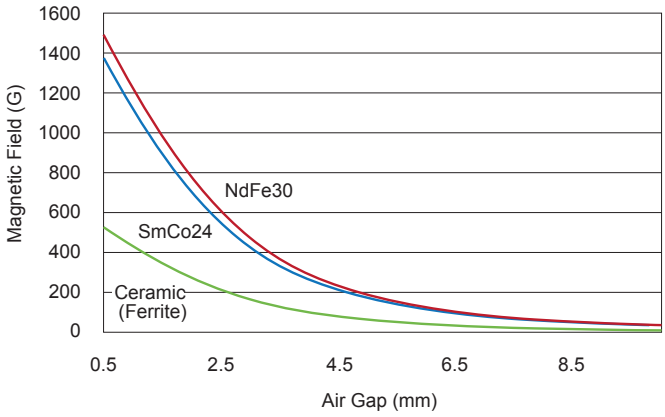


Figure 34: Magnetic Field versus Air Gap for a magnet 6 mm in diameter and 2.5 mm thick.

Allegro can provide similar curves for customer application magnets upon request. Allegro recommends larger magnets for applications that require optimized accuracy performance.

Magnet Misalignment

Magnetic misalignment with the A1333 package impacts the linearity of the observed magnetic signal and consequently the resulting accuracy. The influence of mechanical misalignment may be minimized by reducing the overall airgap and by choosing a larger magnet diameter. Figure 35 shows the influence of magnet diameter of eccentricity error.

The dual die variant of the A1333 uses a stacked die approach, resulting in a common eccentricity value for both die. This eliminates the "native misalignment" present in "side-by-side" packaging options.

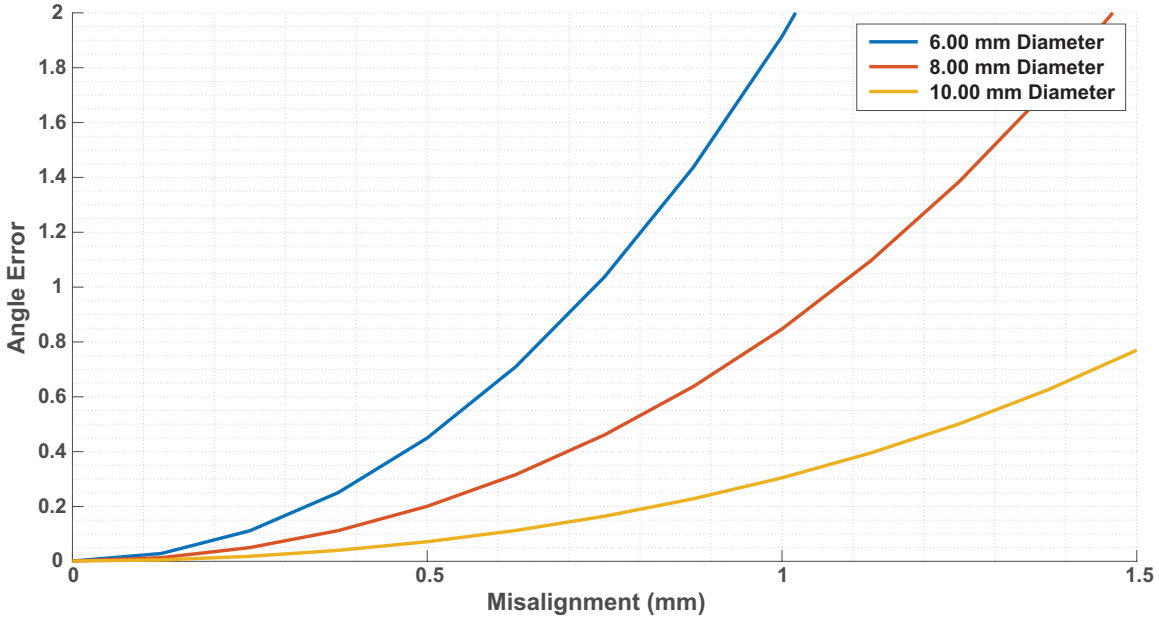


Figure 35: Simulated Error versus Eccentricity for different size magnet diameters, at 2.0 mm air gap

Typical Systemic Error versus magnet to sensor eccentricity (d_{axial}), Note: "Systemic Error" refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.

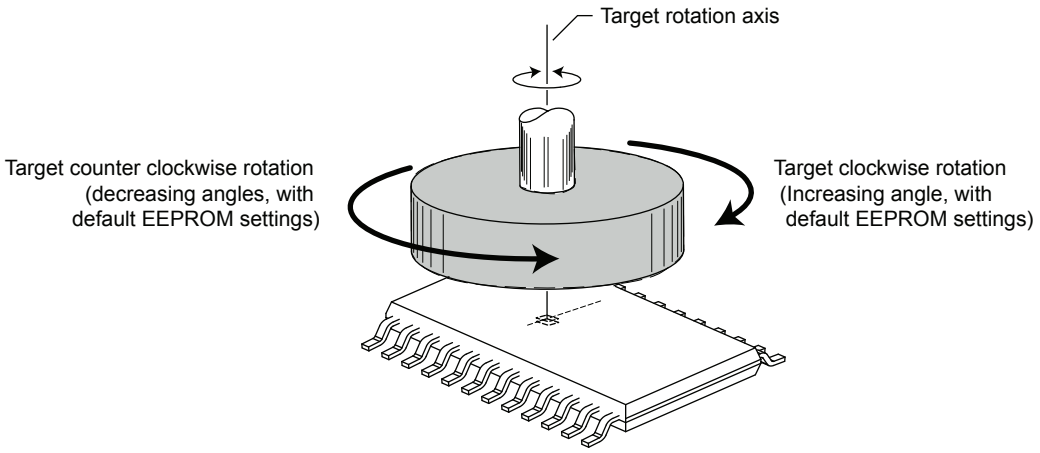
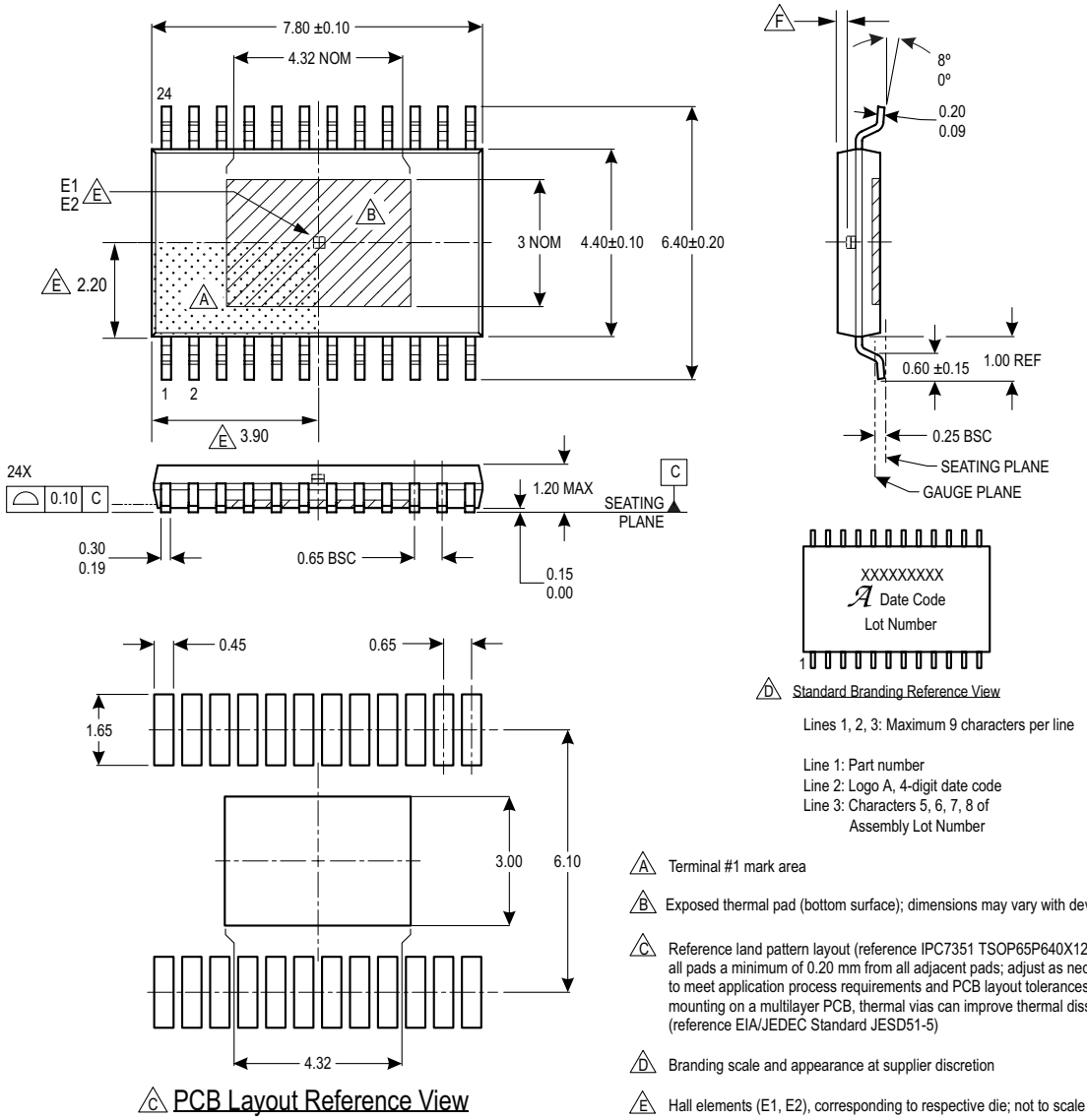


Figure 36: Rotation Direction Definition

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference MO-153 ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

D Standard Branding Reference View

Lines 1, 2, 3: Maximum 9 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

E Hall elements (E1, E2), corresponding to respective die; not to scale

F Active Area Depth 0.36 mm REF

Figure 37: Package LP, 24-Pin TSSOP with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference DWG-2870)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

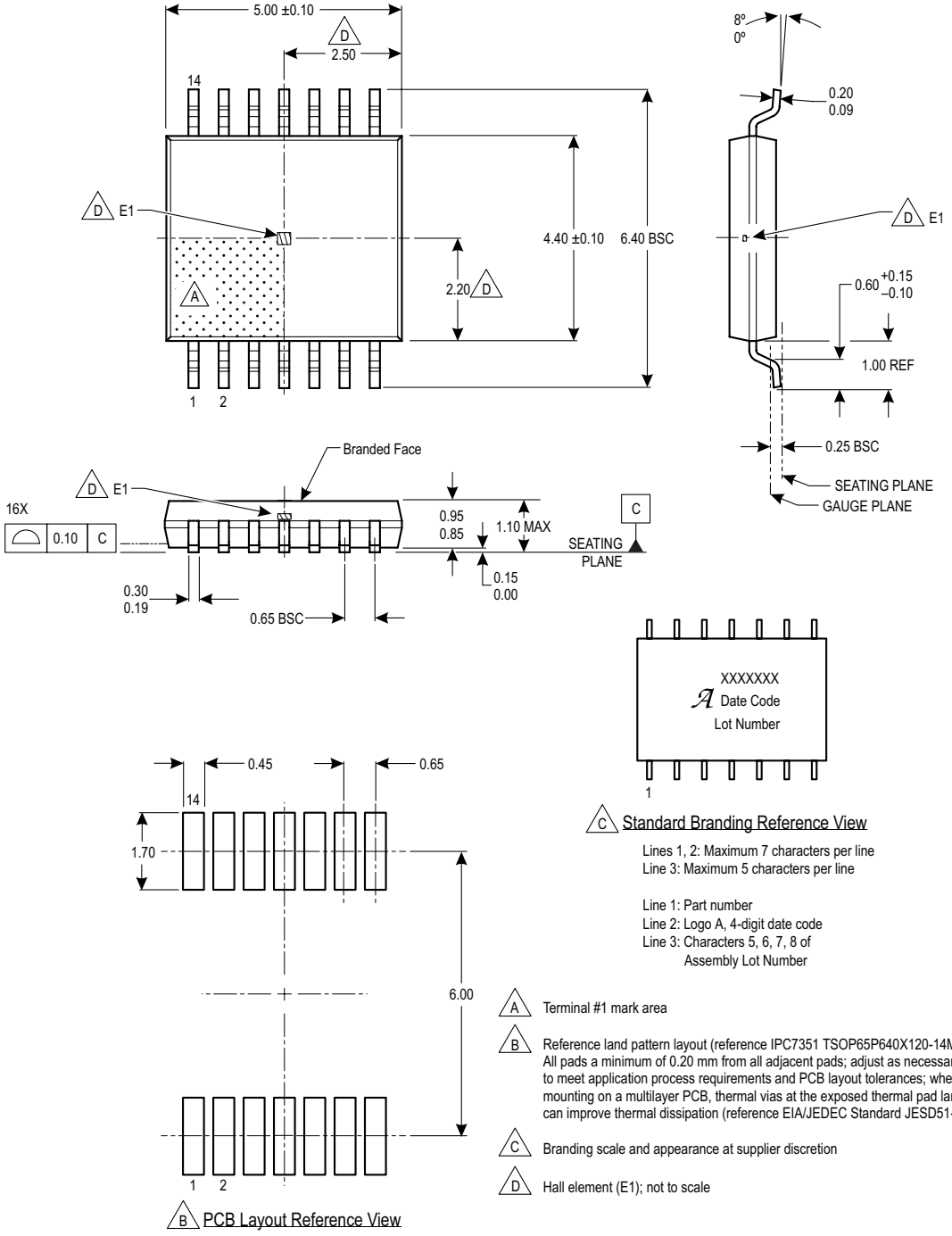


Figure 38: Package LE, 14-Pin TSSOP

APPENDIX A: CRC DOCUMENATION

SPI CRC Implementation

The four bit CRC used with SPI may be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16 bit input and generate a 4bit CRC
* Polynomial = x^4 + x^1 + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
    bool CRC0 = true;
    bool CRC1 = true;
    bool CRC2 = true;
    bool CRC3 = true;
    int  i;
    bool DoInvert;
    uint16_t mask = 0x8000;

    for (i = 0; i < 16; ++i)
    {
        DoInvert = ((input & mask) != 0) ^ CRC3; // XOR
required?

        CRC3 = CRC2;
        CRC2 = CRC1;
        CRC1 = CRC0 ^ DoInvert;
        CRC0 = DoInvert;
        mask >>= 1;
    }

    return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U
: 0U) + (CRC0 ? 1U : 0U);
}
```

Manchester CRC Implementation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD
uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
       bool C0 = false;
       bool C1 = false;
       bool C2 = false;
       bool C0p = true;
       bool C1p = true;
       bool C2p = true;
       uint64_t bitMask = 1;

       bitMask <<= numberOfBits - 1;

       // Calculate the state machine
       for (; bitMask != 0; bitMask >>= 1)
       {
              C2 = C1p;
              C0 = C2p ^ ((data & bitMask) != 0);
              C1 = C0 ^ C0p;

              C0p = C0;
              C1p = C1;
              C2p = C2;
       }

       return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U :
0U);
}
```

APPENDIX B: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual position of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is done by reading the angle sensor IC output and comparing it with a high resolution encoder (refer to Figure 39).

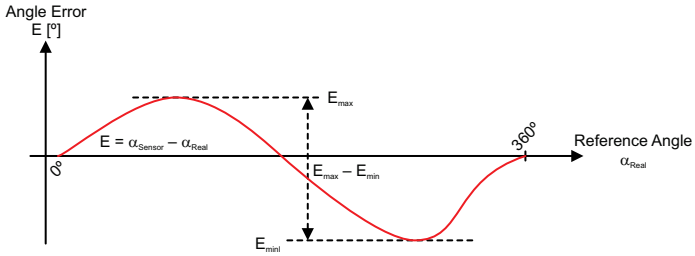


Figure 39: Angle Error Definition

Angle Error Definition

Throughout this document, the term “angle error” is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. The term “angle error” is calculated according to the following formula:

$$Angle\ Error = \frac{E\max - E\min}{2}$$

In other words, it is the amplitude of the deviation from a perfect straight line between 0 and 360 degrees. For the purposes of a generic definition, the offset of the IC angle profile is removed prior to the error calculation (this can be seen in Figure 39). The offset itself will depend on the starting IC angle position relative to the encoder 0° and thus can differ anywhere from 0-360°.

Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro’s factory trim, drift is measured at 150°C. The value is calculated using the following formula:

$$Angle_{Drift} = Angle_{25°C} - Angle_{150°C}$$

where each Angle value is an array corresponding to 16 angular positions around a circle.

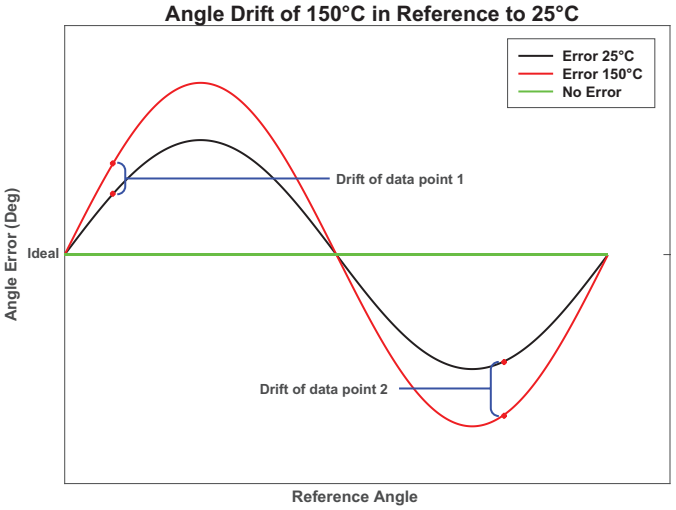


Figure 40: Angle Drift of 150°C in Reference to 25°C [1]

[1] Note that the data above is simply a representation of angle drift and not real data.

Revision History

Revision	Date	Description
–	September 25, 2017	Initial release

For the latest version of this document, visit our website:

www.allegromicro.com