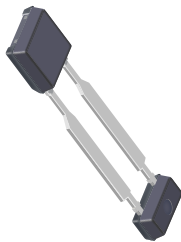


## Two-Wire, Zero-Speed, High Accuracy Differential Sensor IC

### FEATURES AND BENEFITS

- Integrated capacitor reduces requirement for external EMI protection component
- Fully optimized differential digital ring magnet and gear tooth sensor IC
- Running Mode Lockout
- Unique algorithms to assist in mitigation of system anomalies such as vibration
- AGC and reference adjust circuit
- Air gap independent switch points
- Digital output representing target mechanical profile
- Precise duty cycle throughout operating temperature range
- Short power-on time
- True zero-speed operation
- Undervoltage lockout (UVLO)
- Wide operating voltage range
- Internal current regulator for two-wire operation
- Robust test coverage capability using Scan Path and IDDQ measurement
- AEC-Q100 automotive qualified

### PACKAGE: 2-pin SIP (suffix UB)



Not to scale

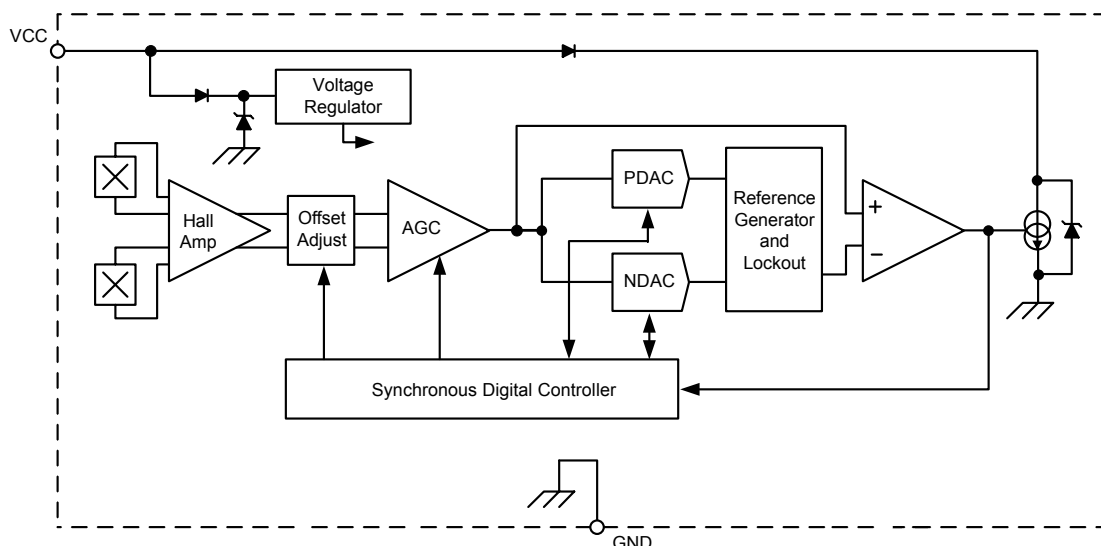
### DESCRIPTION

The A1684LUB is an optimized Hall-effect sensing integrated circuit that provides a user-friendly solution for true zero-speed digital ring magnet and, when magnetically back-biased, gear-tooth sensing in two-wire applications. The Hall-effect IC has been optimized for the automotive environment. This small package can be used in conjunction with a wide variety of target shapes and sizes.

The single integrated circuit incorporates a dual element Hall effect sensor IC and signal processing circuitry that switches in response to differential magnetic signals created by a ring magnet, or by a rotating ferromagnetic target when used in combination with a back-biasing magnet. The device contains a sophisticated compensating circuit to eliminate magnetic and system offsets. Digital tracking of the analog signal is used to achieve true zero-speed operation. Advanced calibration algorithms are used to adjust the device gain and offset at power-up, resulting in air gap independent switch points, which greatly improves output accuracy. In addition, advanced running mode calibration circuits mitigate the effect of system anomalies such as target vibration and sudden changes in air gap.

The regulated current output is configured for two-wire operation. When configured with a back-biasing magnet, this sensor IC is ideal for obtaining edge and duty cycle information in gear-tooth-based applications such as transmission speed.

The A1684 is provided in a 2-pin miniature SIP package (suffix UB) that is lead (Pb) free, with 100% matte tin leadframe plating.



Functional Block Diagram

# A1684LUB

## Two-Wire, Zero-Speed, High Accuracy Differential Sensor IC

### SPECIFICATIONS

#### SELECTION GUIDE

Part Number	Packing*
A1684LUBTN-T	Tape and reel



\*Contact Allegro™ for additional packing options

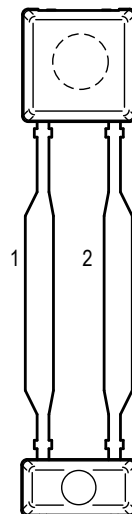
#### ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{CC}$		26.5	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Operating Ambient Temperature	$T_A$	Range L, refer to Power Derating Curve	-40 to 150	°C
Maximum Junction Temperature	$T_J(\text{max})$		165	°C
Storage Temperature	$T_{stg}$		-65 to 170	°C

#### INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Notes	Rating	Units
Nominal Capacitance	$C_{SUPPLY}$	Connected between VCC and GND	10000	pF

### PINOUT DIAGRAM AND TERMINAL LIST TABLE



Terminal List Table

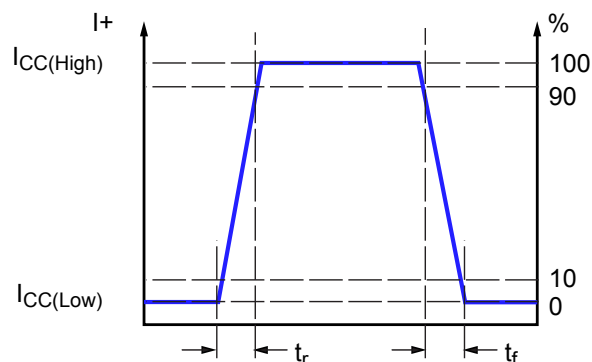
Number	Name	Function
1	VCC	Supply voltage
2	GND	Ground

Package UB, 2-Pin SIP Pin-out Diagram

## OPERATING CHARACTERISTICS: $V_{CC}$ and $T_A$ within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit <sup>2</sup>
<b>ELECTRICAL CHARACTERISTICS</b>						
Supply Voltage <sup>3</sup>	$V_{CC}$	Operating, $T_J < T_J(\text{max})$ , required across pin 1 to pin 2	4.0	–	24	V
Undervoltage Lockout	$V_{CC(\text{UV})}$	$V_{CC} 0 \rightarrow 5 \text{ V}$ or $5 \rightarrow 0 \text{ V}$	–	3.5	3.95	V
Reverse Supply Current <sup>4</sup>	$I_{RCC}$	$V_{CC} = -18 \text{ V}$	–	–	-10	mA
Supply Zener Clamp Voltage <sup>5</sup>	$V_Z$	$I_{CC} = I_{CC(\text{max})} + 3 \text{ mA}$ , $T_A = 25^\circ\text{C}$	28	–	–	V
Supply Zener Current	$I_Z$	$T_A = 25^\circ\text{C}$ , $V_{CC} = 28 \text{ V}$	–	–	19	mA
Supply Current	$I_{CC(\text{Low})}$	Low-current state	4	6	8	mA
	$I_{CC(\text{High})}$	High-current state	12	14	16	mA
Supply Current Ratio	$I_{CC(\text{High})} / I_{CC(\text{Low})}$	Ratio of high current to low current	1.85	–	3.05	–
<b>POWER-ON STATE CHARACTERISTICS</b>						
Power-On Time <sup>6</sup>	$t_{PO}$	$V_{CC} > V_{CC(\text{min})}$ , $f_{OP} < 100 \text{ Hz}$	–	1	2	ms
Power-On State <sup>7</sup>	POS	$t > t_{PO}$	–	$I_{CC(\text{High})}$	–	A
<b>OUTPUT STAGE</b>						
Output Rise Time <sup>8</sup>	$t_r$	Corresponds to measured output slew rate, from 10% to 90% $I_{CC}$ level, $C_{\text{SUPPLY}}$ , $R_{\text{SENSE}} = 100 \Omega$	0	2	4	$\mu\text{s}$
Output Fall Time <sup>8</sup>	$t_f$	Corresponds to measured output slew rate, from 90% to 10% $I_{CC}$ level, $C_{\text{SUPPLY}}$ , $R_{\text{SENSE}} = 100 \Omega$	0	2	4	$\mu\text{s}$
<b>PERFORMANCE CHARACTERISTICS</b>						
Operating Frequency	$f_{OP}$		0	–	12	kHz
Analog Signal Bandwidth	BW		16	20	–	kHz
Operate Point	$B_{OP}$	% of peak-to-peak $B_{\text{SIG}}$ , $AG_{OP}$ within specification	–	70	–	%
Release Point	$B_{RP}$	% of peak-to-peak $B_{\text{SIG}}$ , $AG_{OP}$ within specification	–	30	–	%
Running Mode Lockout Enable Threshold	$V_{\text{LOE}(\text{RM})}$	At peak-to-peak $V_{\text{PROC}} < V_{\text{LOE}(\text{RM})}$ , output switching disables	–	170	–	mV
Running Mode Lockout Release Threshold	$V_{\text{LOR}(\text{RM})}$	At peak-to-peak $V_{\text{PROC}} > V_{\text{LOR}(\text{RM})}$ , output switching enables	–	200	–	mV

Continued on the next page...



Definition of Output Rise Time and Output Fall Time

## OPERATING CHARACTERISTICS: $V_{CC}$ and $T_A$ within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit <sup>2</sup>
<b>CALIBRATION</b>						
Start Mode Hysteresis	$PO_{HYS}$		–	$V_{LOR(RM)}$	–	mV
Initial Calibration <sup>9</sup>	$CAL_I$	Rising output (current) edges, $f_{OP} < 200$ Hz	–	–	3	edges
<b>FUNCTIONAL CHARACTERISTICS</b>						
Operating Signal Range	$B_{SIG}$	Differential magnetic signal	50	–	1500	$G_{PK-PK}$
Extended Operating Signal Range	$B_{SIGEXT}$	Differential magnetic signal, output switching (no missed edges), duty cycle not guaranteed	30	–	–	$G_{PK-PK}$
Allowable User-Induced Differential Offset	$B_{DIFFEXT}$	Operation within specification	–100	–	+100	G
Maximum Sudden Signal Amplitude Change	$B_{SIG(INST)}$	Instantaneous symmetric magnetic signal amplitude change, measured as a percentage of peak-to-peak $B_{SIG}$ , $f_{OP} < 500$ Hz	–	45	–	%

<sup>1</sup> Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 12$  V. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>2</sup> 1 G (gauss) = 0.1 mT (millitesla).

<sup>3</sup> Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.

<sup>4</sup> Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.

<sup>5</sup> Sustained voltages beyond the clamp voltage may cause permanent damage to the IC.

<sup>6</sup> Measured from  $V_{CC} \geq V_{CC}(\text{min})$  to the time when the device is able to switch the output signal in response to a magnetic stimulus.

<sup>7</sup> Please refer to the Functional Description, Power-On section.

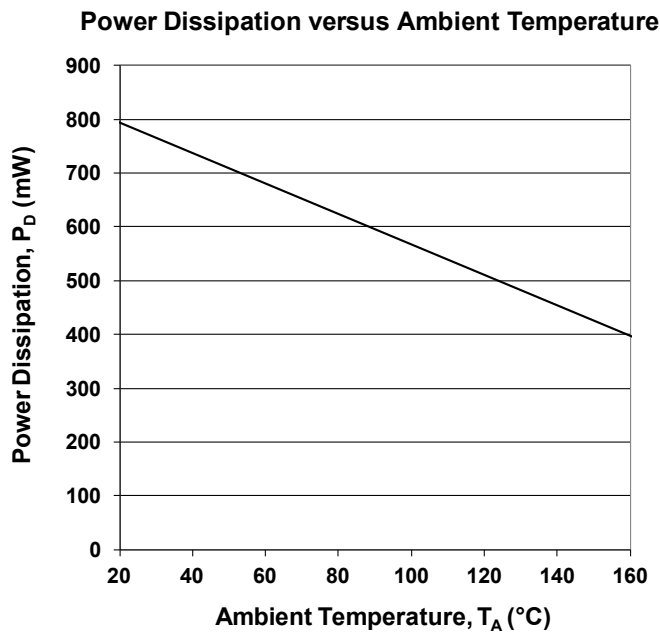
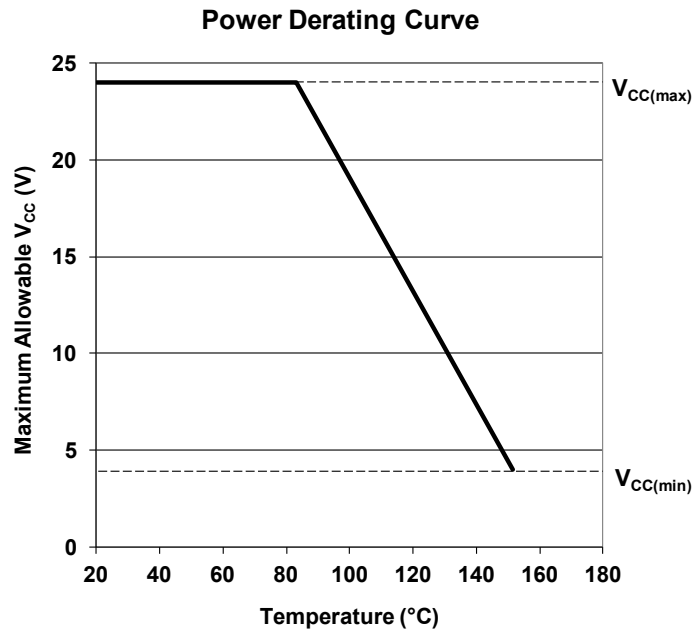
<sup>8</sup> Guaranteed by device characterization.

<sup>9</sup> For power-on frequency,  $f_{OP} < 200$  Hz. Higher power-on frequencies may result in more input magnetic cycles until full output edge accuracy is achieved, including the possibility of missed output edges.

**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB, with copper limited to solder pads	213	$^{\circ}C/W$

\*Additional thermal data available on the Allegro Web site.



## FUNCTIONAL DESCRIPTION

### Sensing Technology

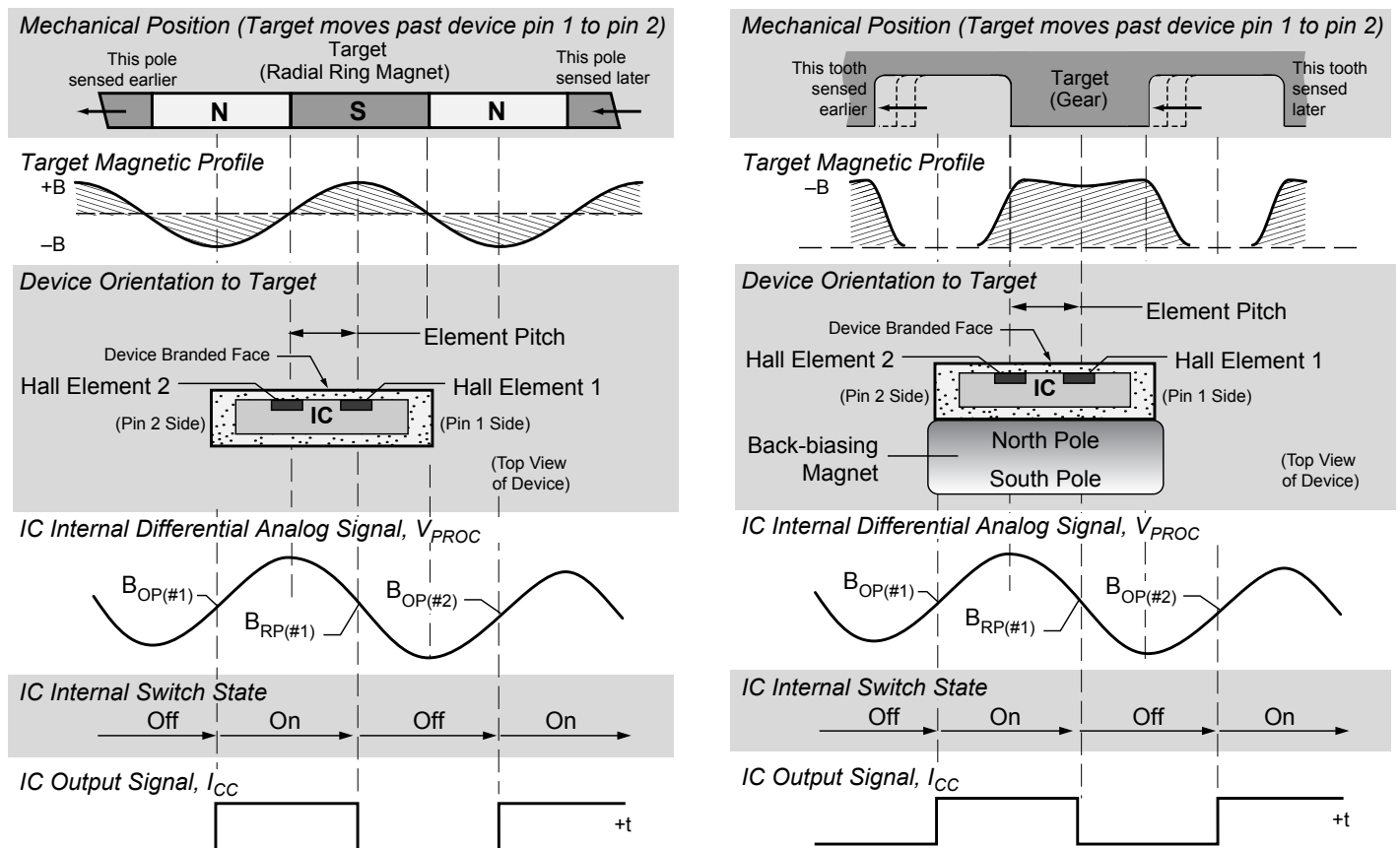
The A1684 sensor IC contains a single-chip differential Hall-effect circuit. As shown in Figure 1, the circuit supports two Hall elements (spaced at a 2.2 mm pitch), which simultaneously sense the magnetic profile of a ring magnet, or when coupled with a back-biasing magnet, the magnetic profile of a ferromagnetic gear target. The sensed magnetic fields at the two Hall elements are subtracted one from the other, to generate a differential internal analog voltage,  $V_{PROC}$ , that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also integrates a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly

affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

### Target Profiling During Operation

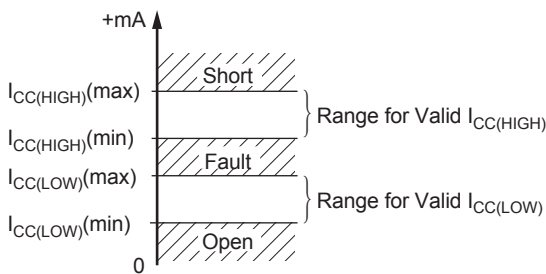
Under normal operating conditions, the IC is capable of providing digital information that is representative of the mechanical features of a rotating gear when back biased, or the poles of a rotating ring magnet. The waveform diagram in Figure 1 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the A1684. No additional optimization is needed and minimal processing circuitry is required.



**Figure 1: Magnetic Profile Reflecting the Geometry of the Target, Allowing the A1684 to Present an Accurate Digital Output Response.**

## Diagnostics

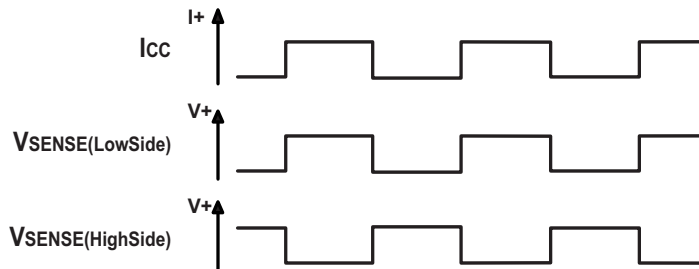
The regulated current output is configured for two-wire applications, requiring one less wire for operation than do switches with the traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges, shown in Figure 2 as  $I_{CC(HIGH)}$  and  $I_{CC(LOW)}$ . Any current level not within these ranges indicates a fault condition. If  $I_{CC} > I_{CC(HIGH)(max)}$ , then a short condition exists, and if  $I_{CC} < I_{CC(LOW)(min)}$ , then an open condition exists. Any value of  $I_{CC}$  between the allowed ranges for  $I_{CC(HIGH)}$  and  $I_{CC(LOW)}$  indicates a general fault condition.



**Figure 2: Diagnostic Characteristics of Supply Current Values.**

## Output Polarity States

$R_{SENSE}$ Location	$I_{CC}$ State	$V_{SENSE}$ State
High side (VCC pin side)	High	Low
	Low	High
Low side (GND pin side)	High	High
	Low	Low



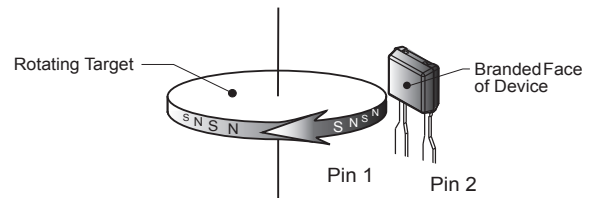
**Figure 4: Alternative Polarity Configurations Using Two-Wire Sensing**

The Output Polarity States table provides the permutations of output voltage relative to  $I_{CC}$ , given alternative locations for  $R_{SENSE}$ . Panel A shows the low-side,  $V_{SENSE(LowSide)}$ , sensing configuration, and panel B shows the high-side,  $V_{SENSE(HighSide)}$ , configuration. As shown by the current and voltage square waves on the left side,  $V_{SENSE(LowSide)}$  is in phase with  $I_{CC}$ , and  $V_{SENSE(HighSide)}$  is inverted.

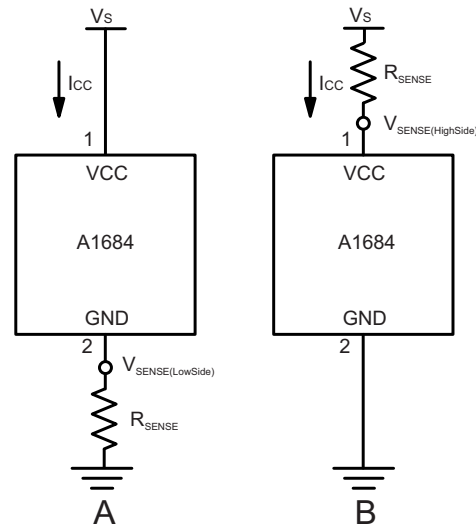
## Determining Output Signal Polarity

In Figure 1, the top of each panel, labeled *Mechanical Position*, represents the mechanical features of the target and orientation to the device. The bottom panels, labeled *IC Output Signal*, displays the square waveform corresponding to the digital output signal (current amplitude) that results from a target configured as shown in Figure 3. Referring to the target side nearest the face of the sensor IC, the direction of rotation is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 2 side.

In order to read the output signal as a voltage,  $V_{SENSE}$ , a sense resistor,  $R_{SENSE}$ , can be placed on either the VCC signal or on the GND signal. As shown in Figure 4, when  $R_{SENSE}$  is placed on the GND signal, the output signal voltage,  $V_{SENSE(LowSide)}$ , is in phase with  $I_{CC}$ . When  $R_{SENSE}$  is placed on the VCC signal, the output signal voltage,  $V_{SENSE(HighSide)}$ , is inverted relative to  $I_{CC}$ .



**Figure 3: Left-to-Right (pin 1 to pin 2) Direction of Target Rotation.**



**Figure 4: Alternative Polarity Configurations Using Two-Wire Sensing**

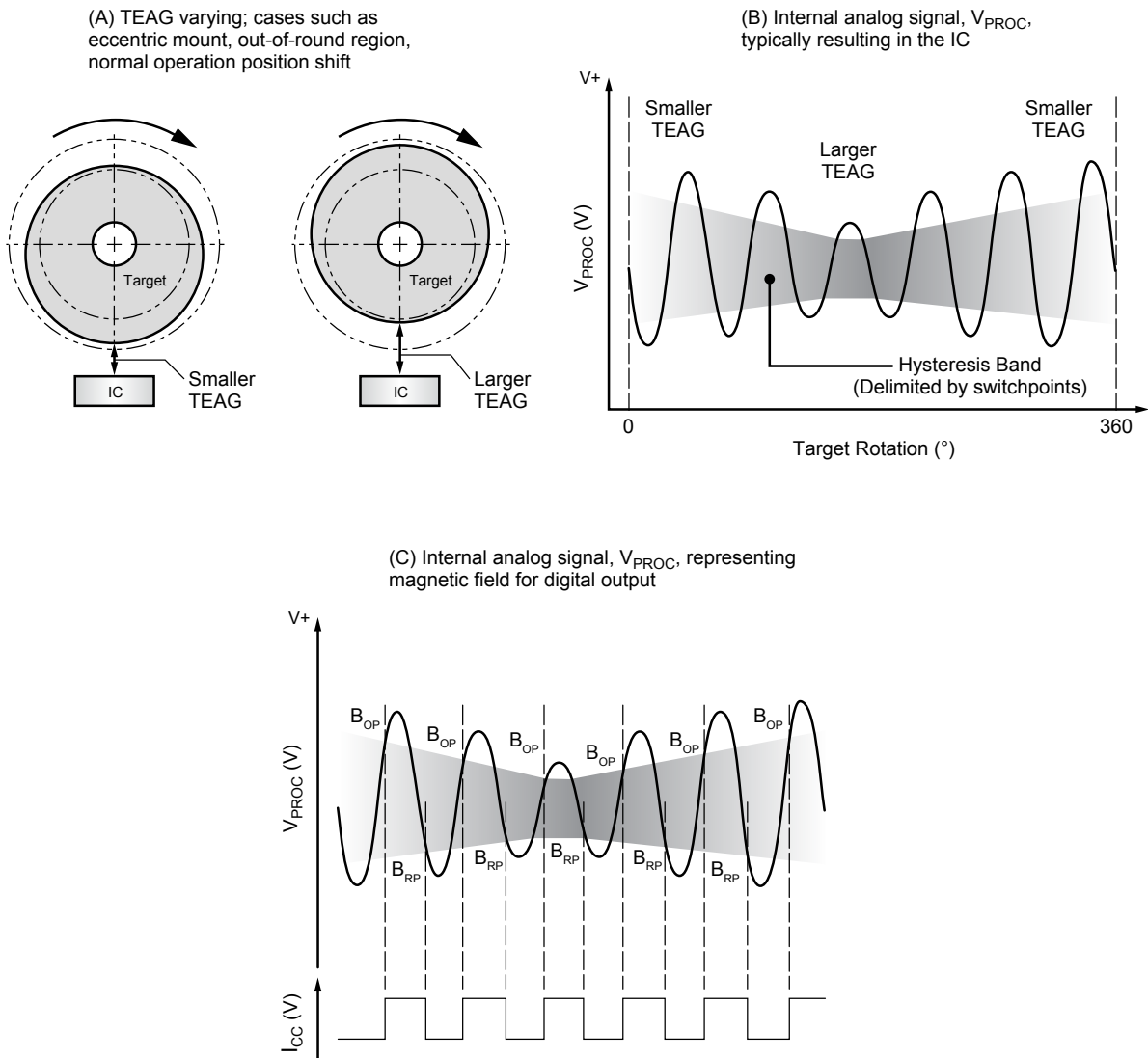
The Output Polarity States table provides the permutations of output voltage relative to  $I_{CC}$ , given alternative locations for  $R_{SENSE}$ . Panel A shows the low-side,  $V_{SENSE(LowSide)}$ , sensing configuration, and panel B shows the high-side,  $V_{SENSE(HighSide)}$ , configuration. As shown by the current and voltage square waves on the left side,  $V_{SENSE(LowSide)}$  is in phase with  $I_{CC}$ , and  $V_{SENSE(HighSide)}$  is inverted.

## Continuous Update of Switch Points

Switch points are the threshold levels of the differential internal analog signal,  $V_{PROC}$ , at which the device changes output signal state. The value of  $V_{PROC}$  is directly proportional to the magnetic flux density,  $B$ , induced by the target and sensed by the Hall elements. As  $V_{PROC}$  rises through a certain limit, referred to as the *operate point*,  $B_{OP}$ , the output state changes from high to low. As  $V_{PROC}$  falls below  $B_{OP}$  to a certain limit, the *release point*,  $B_{RP}$ ,

the output state changes from low to high.

As shown in Figure 5, threshold levels for the switch points are established as a function of the peak input signal levels. The device incorporates an algorithm that continuously monitors the input signal and updates the switching thresholds accordingly with limited inward movement of  $V_{PROC}$ . The switch point for each edge is determined by the detection of the previous two signal edges. In this manner, variations are tracked in real time.



**Figure 5: Continuous Update Algorithm**

The Continuous Update algorithm allows the Allegro IC to interpret and adapt to variances in the magnetic field generated by the target as a result of eccentric mounting of the target, out-of-round target shape, and similar dynamic application problems that affect the TEAG (Total Effective Air Gap). As shown in panel A, the variance in the target position results in a change in the TEAG. This affects the IC as a varying magnetic field, which results in proportional changes in the internal analog signal,  $V_{PROC}$ , shown in panel B. The Continuous Update algorithm is used to establish switch points based on the fluctuation of  $V_{PROC}$ , as shown in panel C.



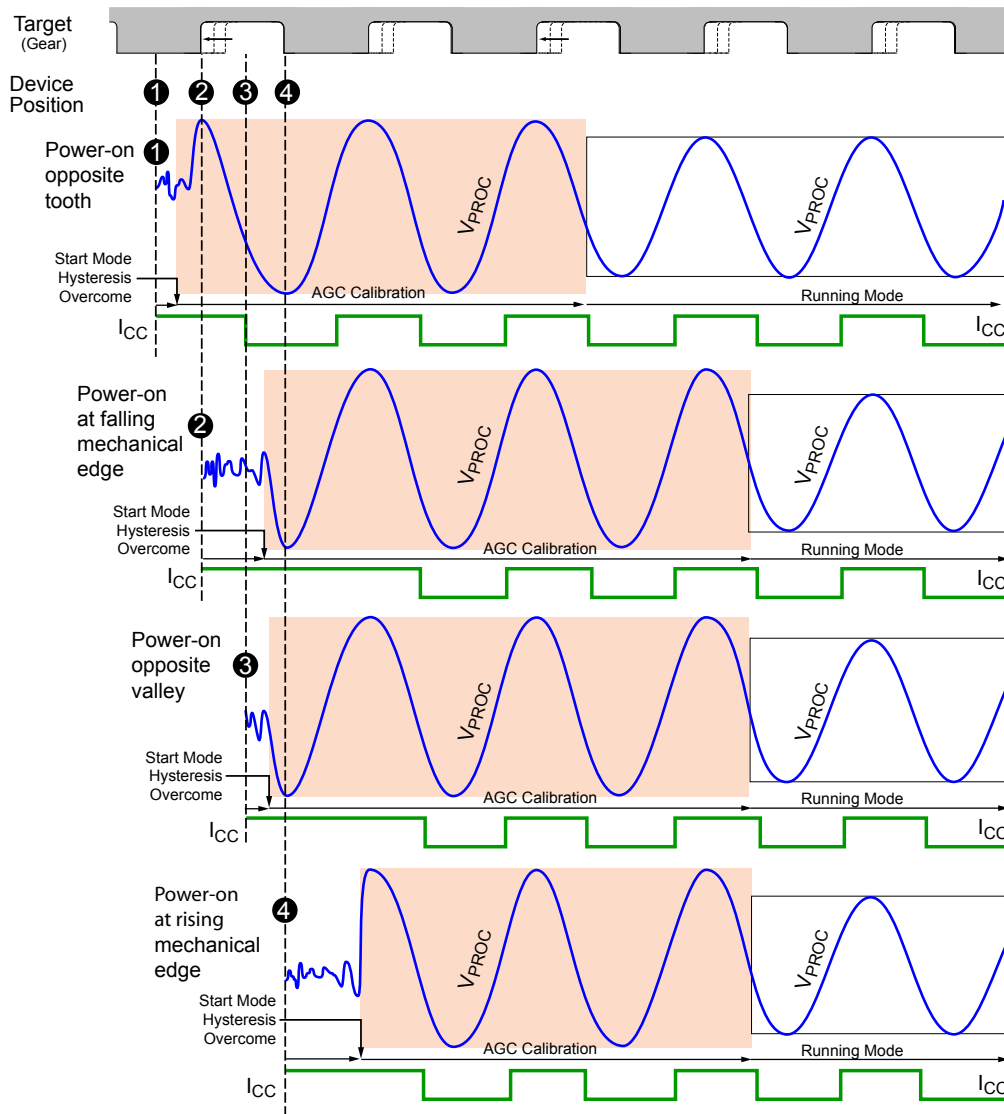
## Power-On

The A1684 is guaranteed to power-on in the high current state,  $I_{CC(High)}$ . When power ( $V_{CC} > V_{CC(min)}$ ) is applied to the device, a short period of time is required to power the various portions of the circuit. During this period, the A1684 will power-on in the high current state,  $I_{CC(High)}$ .

## Initial Edge Detection

The device self-calibrates using the initial teeth sensed, and then enters running mode. This results in reduced accuracy for a brief

period,  $CAL_1$ . However, this period allows the device to optimize for running mode operation. As shown in Figure 6 (assuming the south magnetic pole of a back-biasing magnet is adjacent to the rear of the A1684 case), the first three high peak signals corresponding to rising output edges are used to calibrate AGC (Automatic Gain Control). There is a slight variance in the duration of initialization, depending on what target feature is opposite the sensor IC when power-on occurs. Also, a high speed of target rotation at power-on may increase the quantity of output edges required in the  $CAL_1$  period.



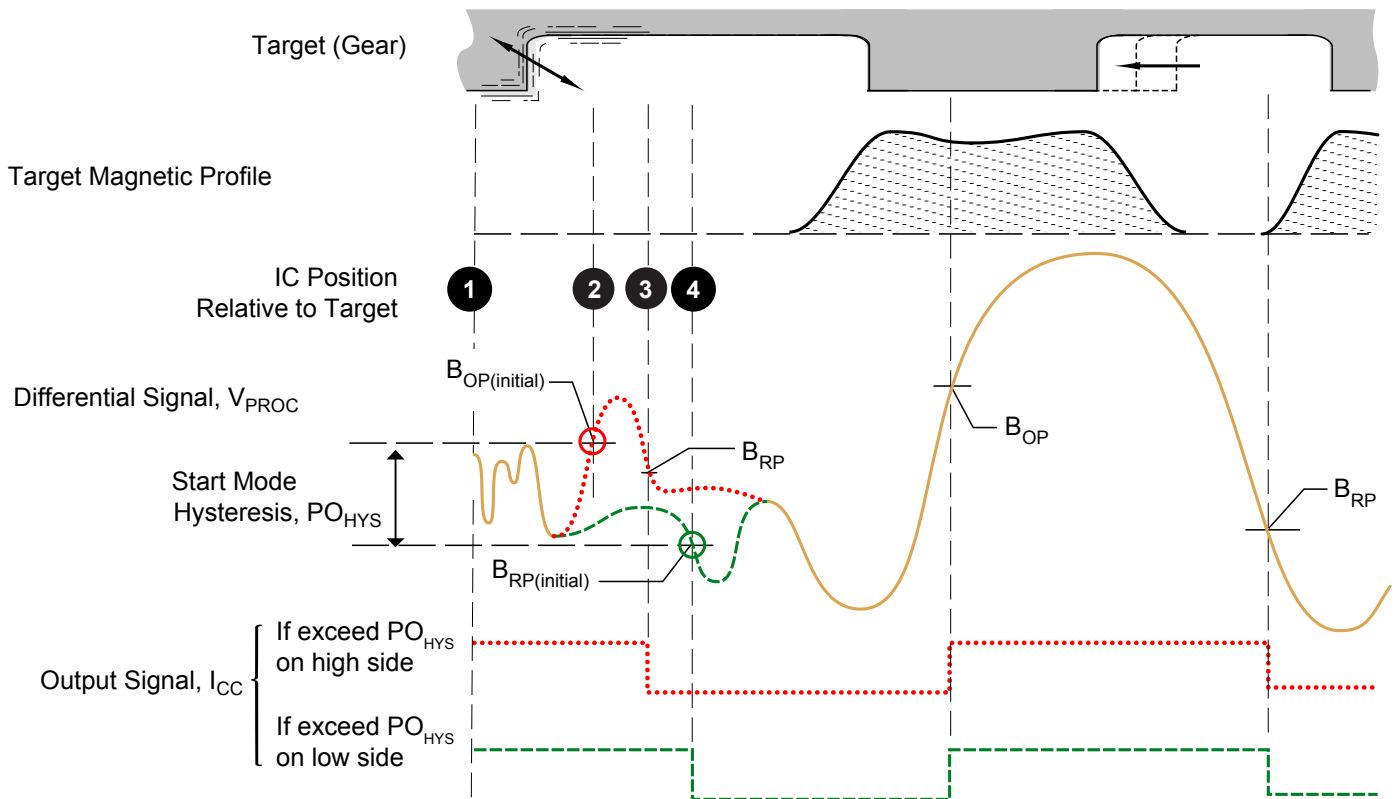
**Figure 6: Power-On Initial Edge Detection.**

This figure demonstrates four typical power-on scenarios. All of these examples assume a south magnetic pole of a back-biasing magnet is adjacent to the rear of the A1684 case. The length of time required to overcome Start Mode Hysteresis, as well as the combined effect of whether it is overcome in a positive or negative direction plus whether the next edge is in that same or opposite polarity, affect the point in time when AGC calibration begins. Three high peaks are always required for AGC calibration when  $f_{OP} \leq 200$  Hz, and more may be required at greater speeds.

## Start Mode Hysteresis

This feature helps to ensure optimal self-calibration by rejecting electrical noise and low-amplitude target vibration during initialization. This prevents AGC from calibrating the device on such spurious signals. Calibration can be performed using the actual target features.

A typical scenario is shown in Figure 7 (assuming the south magnetic pole of a back-biasing magnet is adjacent to the rear of the A1684 case). The hysteresis,  $PO_{HYS}$ , is a minimum level of the peak-to-peak amplitude of the internal analog electrical signal,  $V_{PROC}$ , that must be exceeded before the A1684 starts to compute switch points.



**Figure 7: Operation of Start Mode Hysteresis**

(assumes the south magnetic pole of a back-biasing magnet is adjacent to the rear of the A1684 case)

- At power-on (position 1), the A1684 begins sampling  $V_{PROC}$ .
- At the point where the Start Mode Hysteresis,  $PO_{HYS}$ , is exceeded, the device establishes an initial switching threshold, by using the Continuous Update algorithm. If  $V_{PROC}$  is rising through the limit on the high side (position 2), the switch point is  $B_{OP}$ , and if  $V_{PROC}$  is falling through the limit on the low side (position 4), it is  $B_{RP}$ . After this point, Start Mode Hysteresis is no longer a consideration. Note that a valid  $V_{PROC}$  value exceeding the Start Mode Hysteresis can be generated either by a legitimate target feature or by excessive vibration.
- In either case ( $B_{OP}$  or  $B_{RP}$ ), because the switch point is immediately passed as soon as it is established, the A1684 enables switching:
  - If on the high side, at  $B_{OP}$  (position 2) the output would switch from low to high. However, because output is already high, no output switching occurs.
  - At the next switch point, where  $B_{RP}$  is passed (position 3), the output switches from high to low.
  - If on the low side, at  $B_{RP}$  (position 4) the output switches from high to low.

## Undervoltage Lockout

When the supply voltage falls below the minimum operating voltage,  $V_{CC(UV)}$ ,  $I_{CC}$  goes high and remains high regardless of the state of the magnetic gradient from the target. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the device. Because  $V_{CC}$  is below the  $V_{CC(min)}$  specification during lockout, the  $I_{CC}$  levels may not be within specification.

## Power Supply Protection

The device contains an on-chip regulator and can operate over a wide  $V_{CC}$  range. For devices that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to Figure 8 for an example of a basic application circuit.

## Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain is then automatically adjusted. Figure 9 illustrates the effect of this feature.

## Running Mode Gain Adjust

The A1684 has a feature during Running mode to compensate for dynamic air gap variation. If the system increases the mag-

netic input drastically, the device will gradually readjust the gain downwards, allowing the chip to regain the optimum internal electrical signal with the new, larger, magnetic signal.

## Dynamic Offset Cancellation (DOC)

The offset circuitry when combined with AGC automatically reduces the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including both Power-on mode and Running mode, compensating for any offset drift (within Allowable User-Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

## Running Mode Lockout

The A1684 has a Running mode lockout feature to prevent switching on small signals that are characteristic of vibration signals. The internal logic of the chip evaluates small signal amplitudes below a certain level to be vibration. In that event, the output is blanked (locked-out) until the amplitude of the signal returns to normal operating levels.

## Watchdog

The A1684 employs a watchdog circuit to prevent extended loss of output switching during sudden impulses and vibration in the system. If the system changes the magnetic input drastically such that target feature detection is terminated, the device will fully reset itself, allowing the chip to recalibrate properly on the new magnetic input signal.

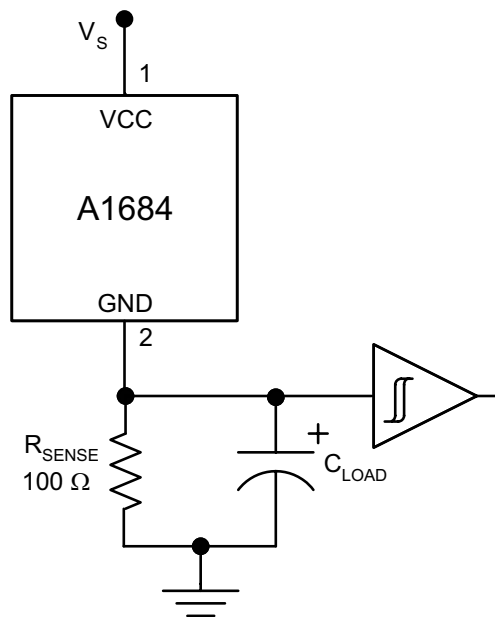


Figure 8: Typical Circuit for Proper Device Operation

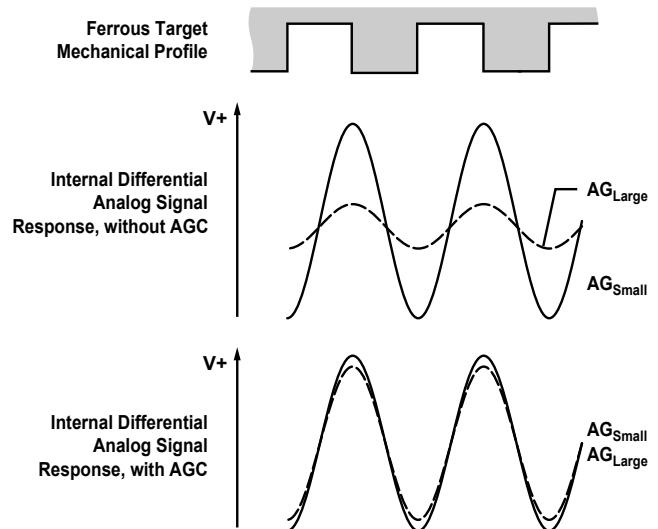
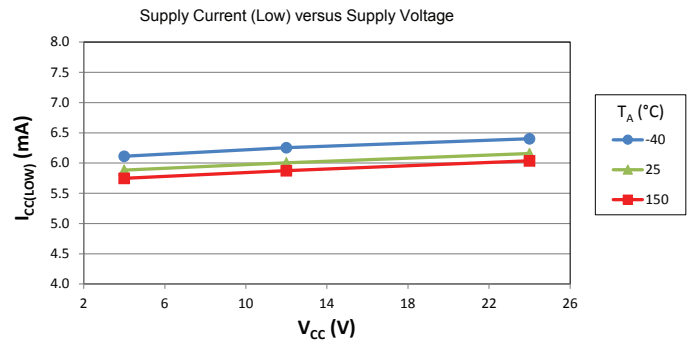
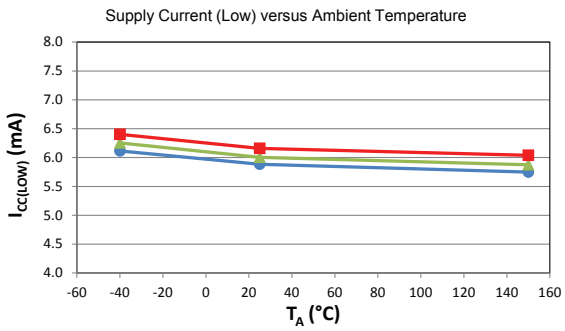
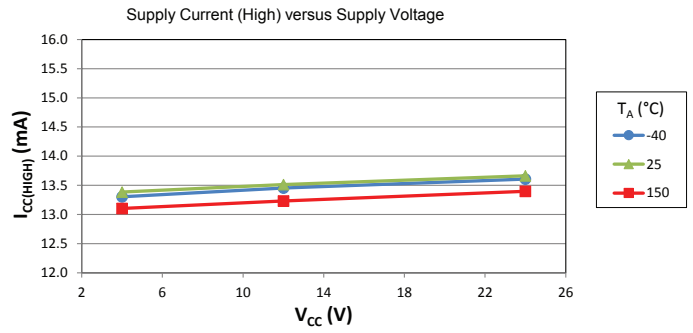
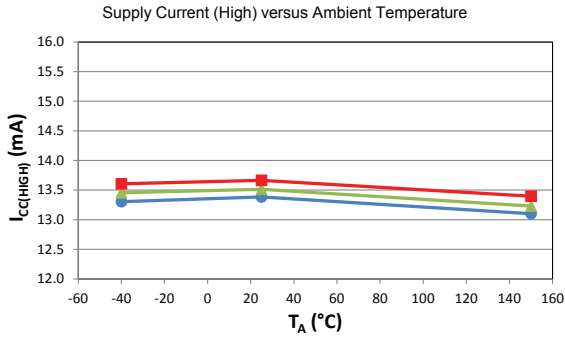


Figure 9: Automatic Gain Control (AGC)

The AGC function corrects for variances in the air gap. Differences in the air gap cause differences in the magnetic field at the device, but AGC prevents that from affecting device performance, as shown in the lowest panel.

## CHARACTERISTIC PERFORMANCE SUPPLY CURRENT



## POWER DERATING

The device must be operated below the maximum junction temperature of the device,  $T_{J(max)}$ . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance,  $R_{\theta JA}$ , is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity,  $K$ , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case,  $R_{\theta JC}$ , is relatively small component of  $R_{\theta JA}$ . Ambient air temperature,  $T_A$ , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $I_{CC} = 6\text{ mA}$ , and  $R_{\theta JA} = 213\text{ }^\circ\text{C/W}$ , then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 6\text{ mA} = 72\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 72\text{ mW} \times 213\text{ }^\circ\text{C/W} = 15.3^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 15.3^\circ\text{C} = 40.3^\circ\text{C}$$

A worst-case estimate,  $P_{D(max)}$ , represents the maximum allowable power level ( $V_{CC(max)}$ ,  $I_{CC(max)}$ ), without exceeding  $T_{J(max)}$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for UB package  $V_{CC}$  at  $T_A = 150^\circ\text{C}$ , using a minimum-K PCB using a single layer PCB.

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 213^\circ\text{C/W}$ ,  $T_{J(max)} = 165^\circ\text{C}$ ,  $V_{CC(max)} = 24\text{ V}$ , and  $I_{CC(max)} = 16\text{ mA}$ .

Calculate the maximum allowable power level,  $P_{D(max)}$ . First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA}$$

$$P_{D(max)} = 15^\circ\text{C} \div 213^\circ\text{C/W} = 70.5\text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 70.5\text{ mW} \div 16\text{ mA} = 4.4\text{ V}$$

The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(est)}$ .

Compare  $V_{CC(est)}$  to  $V_{CC(max)}$ . If  $V_{CC(est)} \leq V_{CC(max)}$ , then reliable operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  requires enhanced  $R_{\theta JA}$ . If  $V_{CC(est)} \geq V_{CC(max)}$ , then operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  is reliable under these conditions.

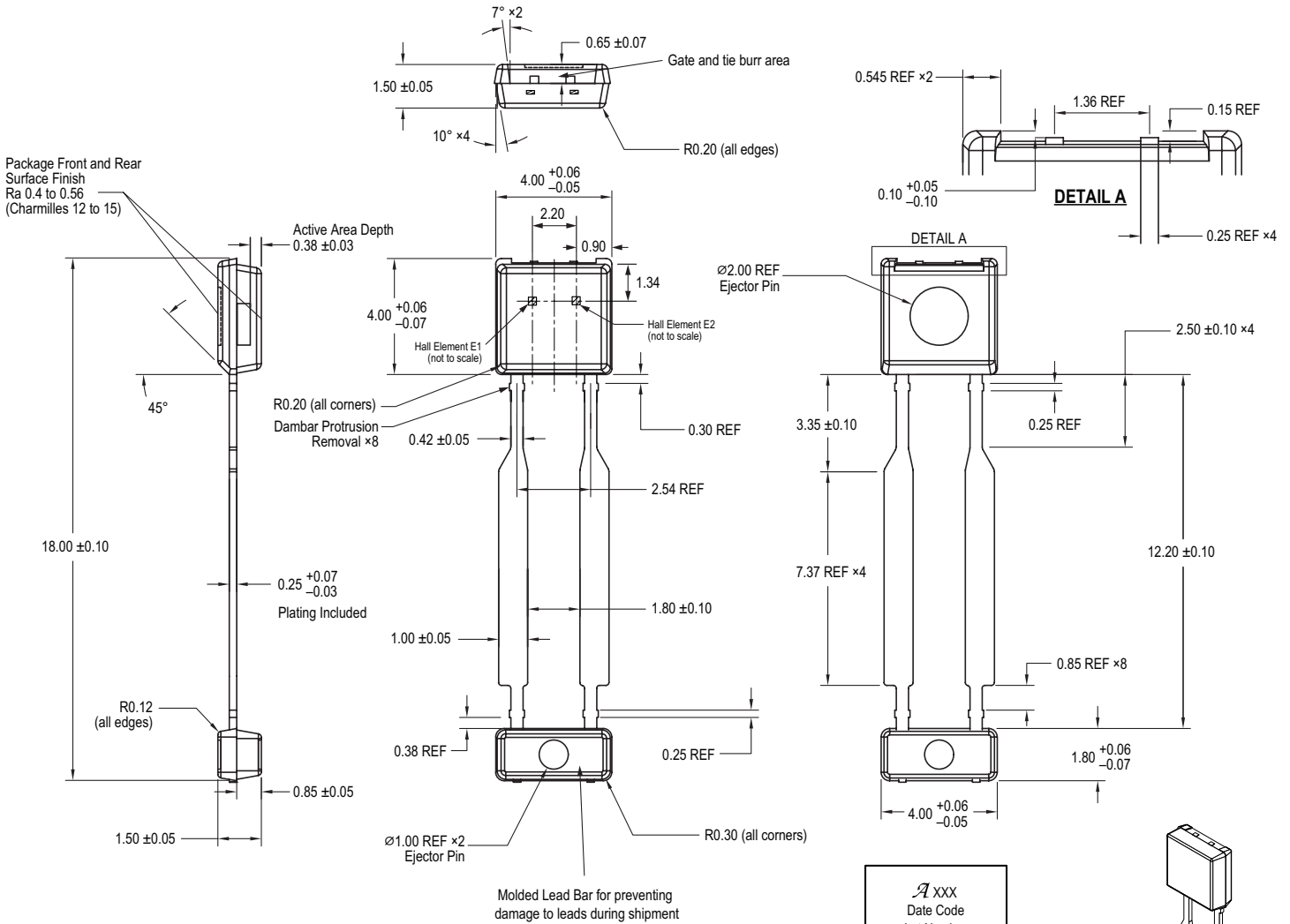
## PACKAGE OUTLINE DRAWING

**For Reference Only – Not for Tooling Use**

(Reference DWG-0000408, Rev. 4)

Dimensions in millimeters – NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown



Standard Branding Reference View

Line 1 = Logo A, 3 characters  
Lines 2, 3 = Max 5 characters per line

Line 1: Logo A, 3-digit Part Number  
Line 2: 4-digit Date Code  
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Exception allowed for parts with multiple package variants:  
Line 1: Last 4 digits of part number plus Package Variant

Branding scale and appearance at supplier discretion

Figure 10: Package UB, 2-Pin SIP

## Revision History

Number	Date	Description
–	March 7, 2014	Initial release
1	October 7, 2014	Updated Package Outline Drawing and reformatted document (was Rev. 0.1).
2	December 15, 2014	Updated $C_{SUPPLY}$ , $t_r$ , $t_f$ , and package drawing (was Rev. 0.2).
3	March 24, 2015	Updated branding on Package Outline Drawing (was Rev. 0.3).
4	December 7, 2015	Added AEC-Q100 qualified bullet to Features and Benefits (was Rev. 0.4)
5	March 1, 2016	Updated Package Outline Drawing molded lead bar footnote, Internal Discrete Capacitor Ratings table, corrected Characteristic Performance labels, and renumbered revisions.
6	July 22, 2016	Corrected Hall spacing dimension of Package Outline Drawing.
7	November 8, 2016	Updated Figure 1.
8	March 29, 2019	Minor editorial updates.
9	April 2, 2020	Minor editorial updates.
10	April 6, 2022	Updated package drawing (page 14)

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