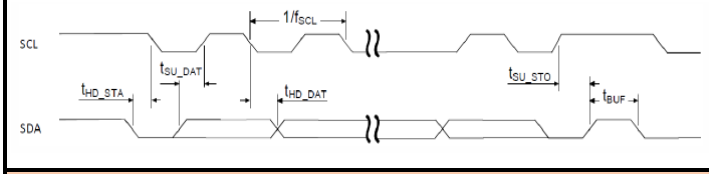
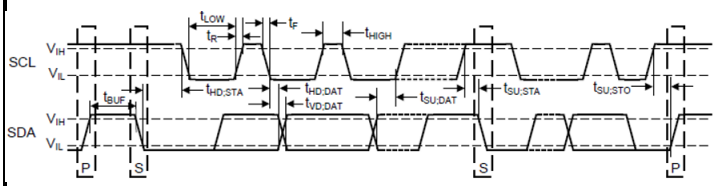
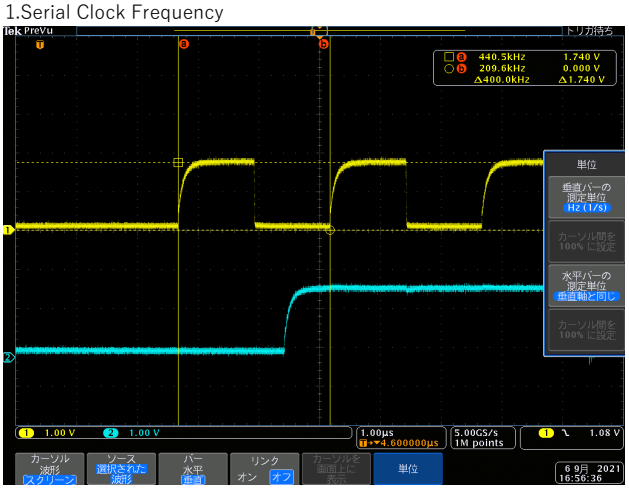
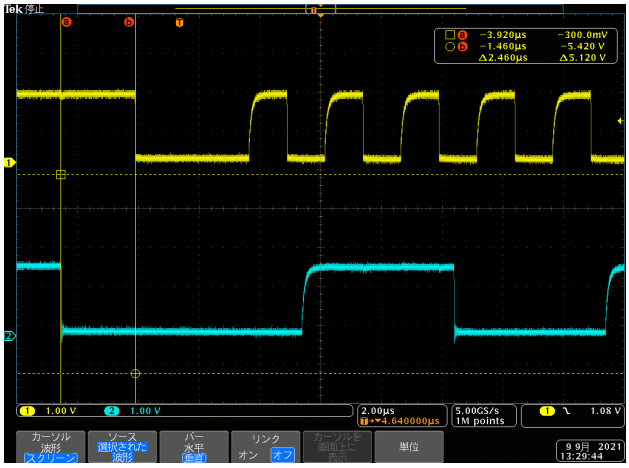
| CPU | |
|---|---|
|  | |
| **TI TMP117** | |
|  | |

1.Serial Clock Frequency

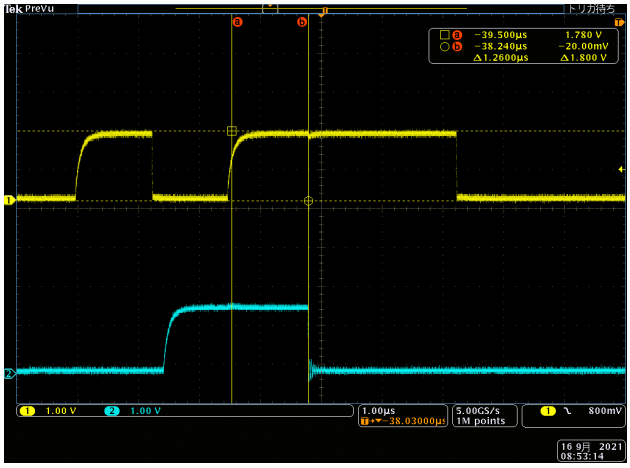



2.Bus Free Time Between a Stop/Start Condition

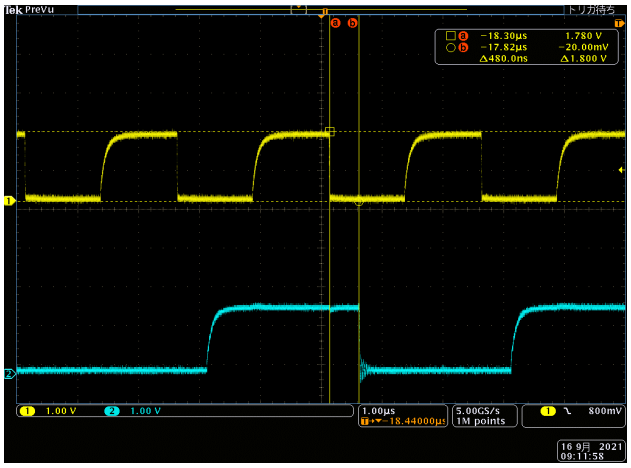

3.Hold Time for Repeated Start Condition



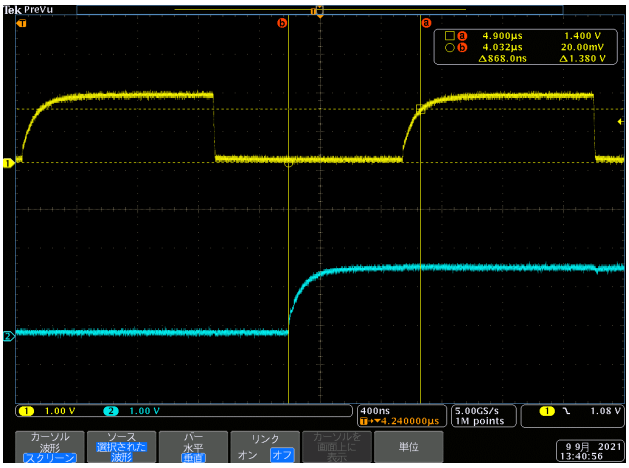

4.Setup Time for a Repeated START Condition



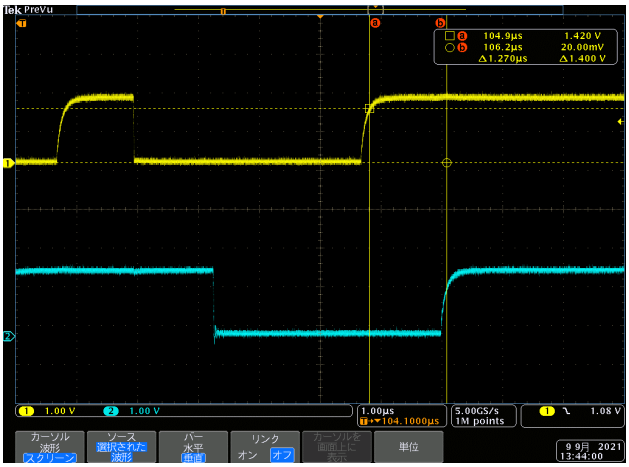
5.Data Hold Time




6.Data Setup Time



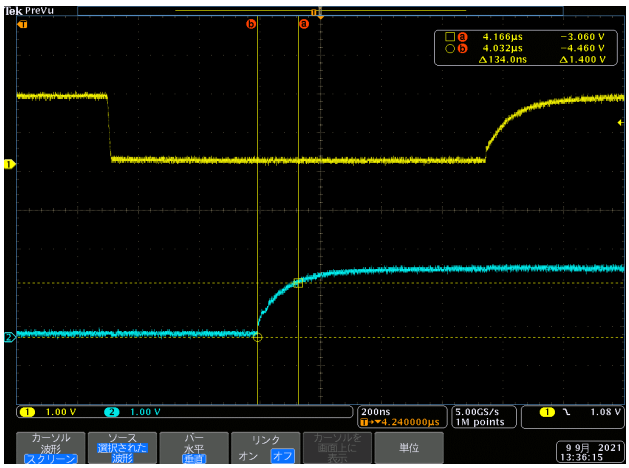

7.Setup Time for STOP Condition



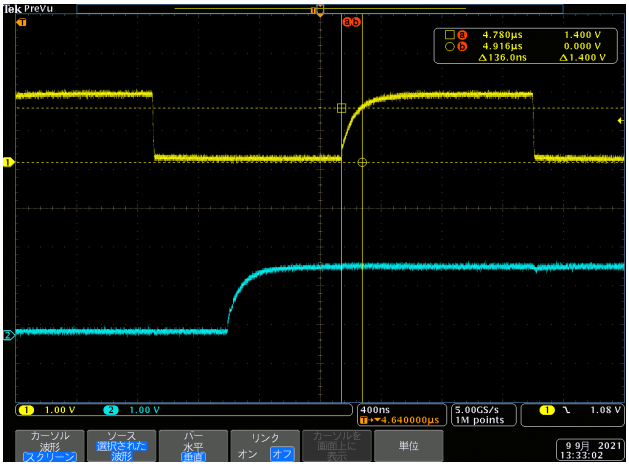

8.Pulse Width of Suppressed Spike

Not observable

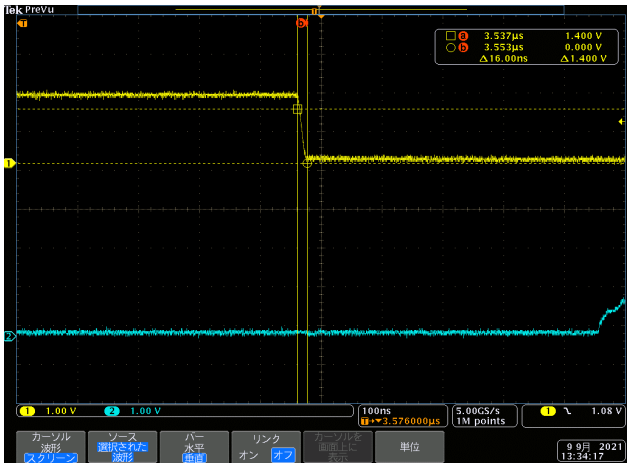
9.SDA Rise Time



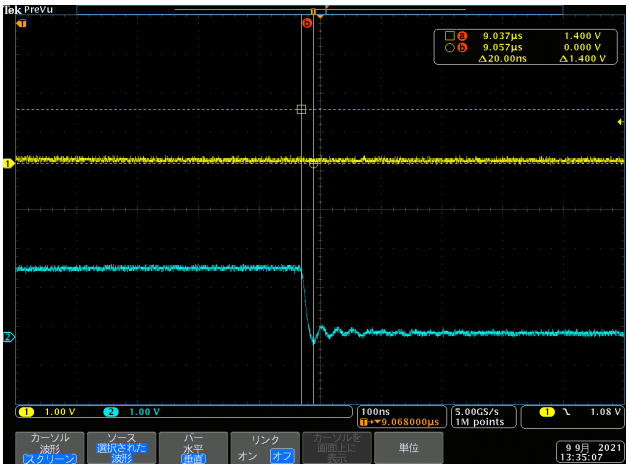

10.SCL Rise Time



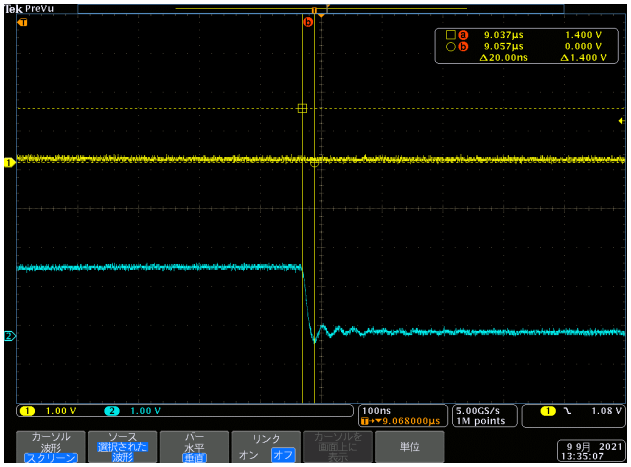
11.SCL Receiving Fall Time




12.SDA Receiving Fall Time

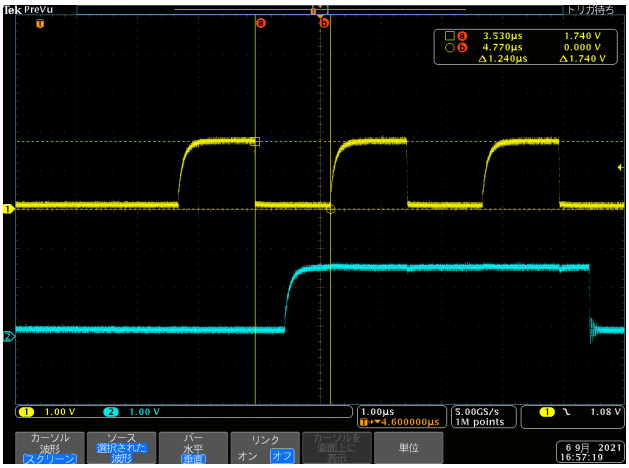



13.SDA Transmitting Fall Time

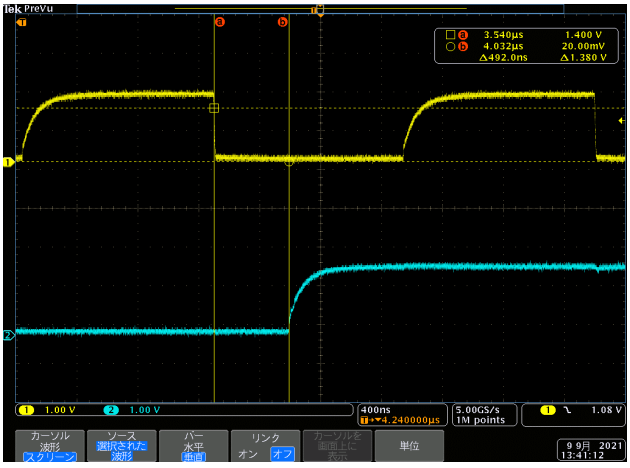



14.SCL Pulse-Width Low

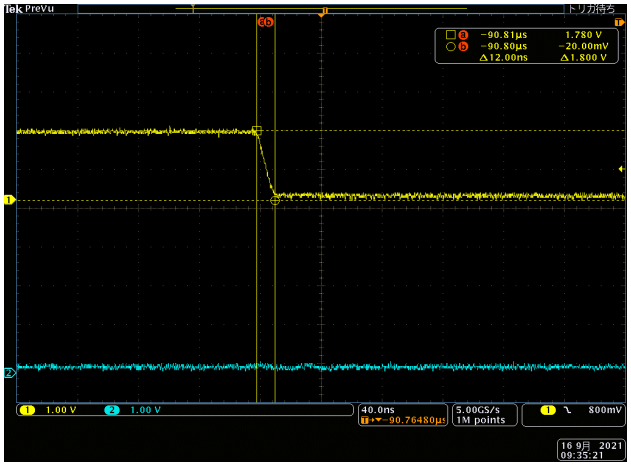

15.SCL Pulse-Width High



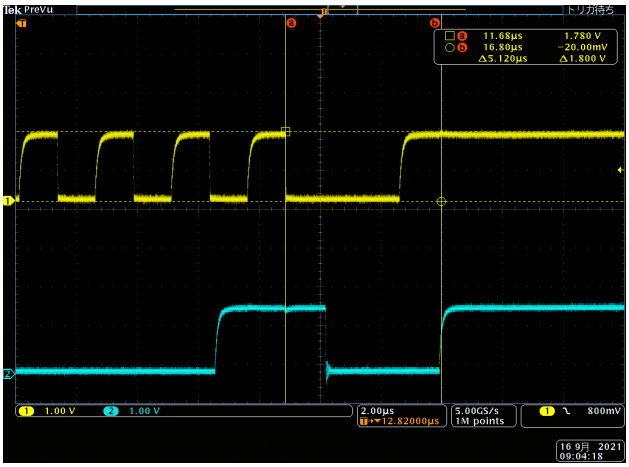

16.Data Valid Time



17.Output Fall Time




18.Data Valid Acknowledge Time




19.SDA Rise Time after ACK