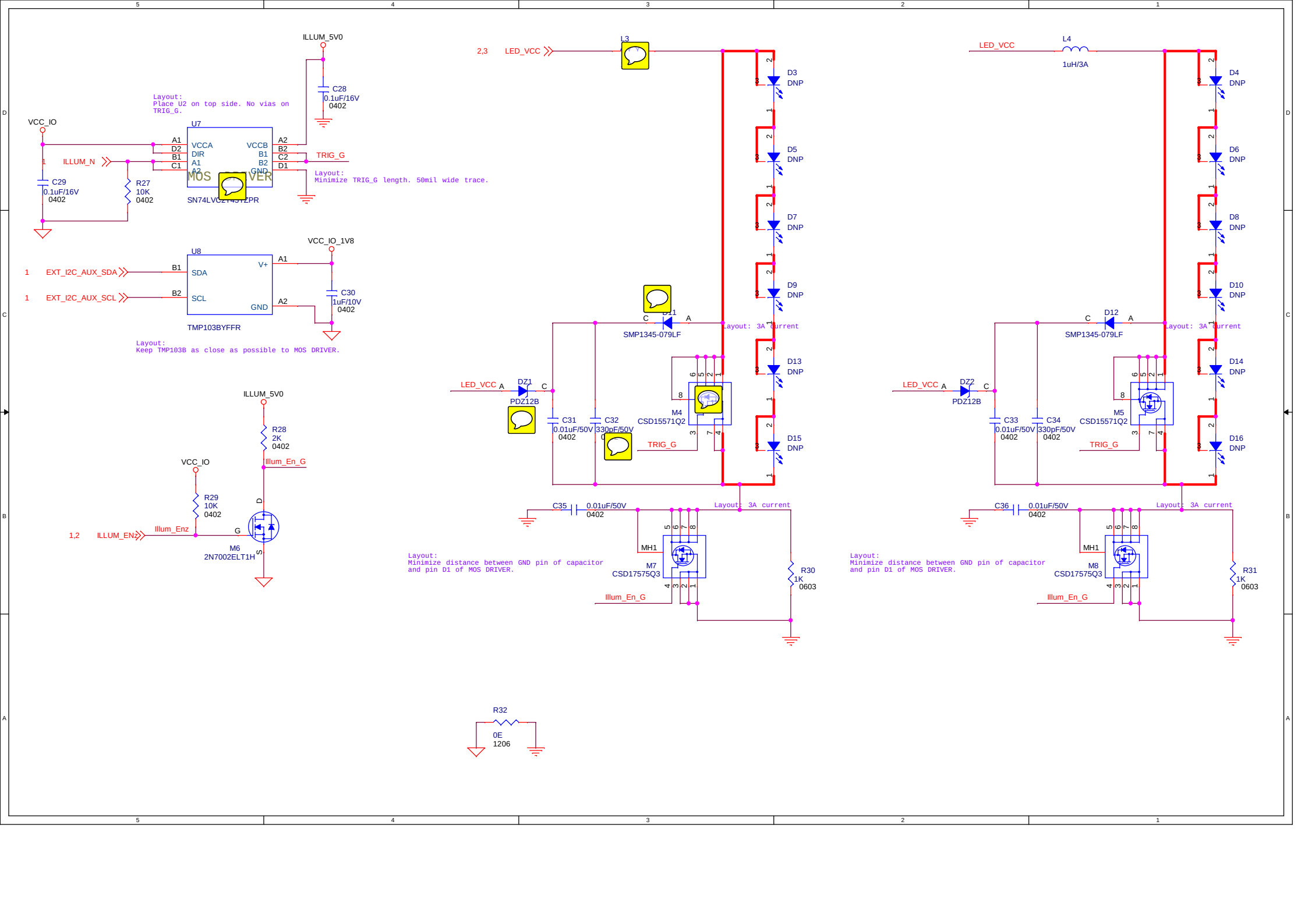
ILLUM_5V0
C28
0.1uF/16V
0402
Layout:
Place U2 on top side. No vias on
TRIG_G.
VCC_IO
U7
A1
D2
B1
C1
VCCA
DIR
A1
A2
VCCB
B1
B2
GND
A2
B2
C2
D1
TRIG_G
1
ILLUM_N
C29
0.1uF/16V
0402
R27
10K
0402
MOS DRIVER
SN74LVC2T45YZPR
Layout:
Minimize TRIG_G length. 50mil wide trace.
VCC_IO_1V8
U8
1
EXT_I2C_AUX_SDA
B1
SDA
V+
A1
C30
1uF/10V
0402
1
EXT_I2C_AUX_SCL
B2
SCL
GND
A2
TMP103BYFFR
Layout:
Keep TMP103B as close as possible to MOS DRIVER.
ILLUM_5V0
R28
2K
0402
Illum_En_G
VCC_IO
R29
10K
0402
D
1,2
ILLUM_ENz
Illum_Enz
G
M6
2N7002ELT1H
S
2,3
LED_VCC
L3
D3
DNP
D5
DNP
D7
DNP
D9
DNP
D11
C
A
SMP1345-079LF
Layout: 3A current
D13
DNP
D15
DNP
LED_VCC
A
DZ1
C
PDZ12B
C31
0.01uF/50V
0402
C32
330pF/50V
TRIG_G
M4
CSD15571Q2
C35
0.01uF/50V
0402
Layout: 3A current
MH1
M7
CSD17575Q3
Illum_En_G
R30
1K
0603
Layout:
Minimize distance between GND pin of capacitor
and pin D1 of MOS DRIVER.
R32
0E
1206
LED_VCC
L4
1uH/3A
D4
DNP
D6
DNP
D8
DNP
D10
DNP
D12
C
A
SMP1345-079LF
Layout: 3A current
D14
DNP
D16
DNP
LED_VCC
A
DZ2
C
PDZ12B
C33
0.01uF/50V
0402
C34
330pF/50V
TRIG_G
M5
CSD15571Q2
C36
0.01uF/50V
0402
Layout: 3A current
MH1
M8
CSD17575Q3
Illum_En_G
R31
1K
0603
Layout:
Minimize distance between GND pin of capacitor
and pin D1 of MOS DRIVER.