

## FEATURES

- **Ultralow Supply Current: 850nA**
- **Low Drift**
  - A Grade: 10 ppm/°C Max
  - B Grade: 20 ppm/°C Max
- **High Accuracy**
  - A Grade: 0.05% Max
  - B Grade: 0.1% Max
- **Long-Term Drift: 15ppm/ $\sqrt{\text{kHr}}$  (LS8 Package)**
- **No Humidity Sensitivity (LS8 Package)**
- High Output Drive Current: 5mA Min
- Low Dropout Voltage: 10mV Max
- Fully Specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Operational from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Wide Supply Range to 18V
- Reverse Input/Output Protection
- Available Output Voltage Options: 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V
- Available in Low Profile (1mm) ThinSOT™, (2mm  $\times$  2mm) DFN and High Stability Hermetic (5mm  $\times$  5mm) LS8 Packages

## APPLICATIONS

- Precision A/D and D/A Converters
- Portable Gas Monitors
- Battery- or Solar-Powered Systems
- Precision Regulators
- Low Voltage Signal Processing
- Micropower Remote Sensing

## DESCRIPTION

The **LT<sup>®</sup>6656** is a tiny precision voltage reference that draws less than 1 $\mu$ A of supply current and can operate with a supply voltage within 10mV of the output voltage. The LT6656 offers an initial accuracy of 0.05% and temperature drift of 10ppm/°C. The combined low power and precision characteristics are ideal for portable and battery powered instrumentation.

The LT6656 can supply up to 5mA of output drive with 65ppm/mA of load regulation, allowing it to be used as the supply voltage and the reference input to a low power ADC. The LT6656 can accept a supply voltage up to 18V and withstand the reversal of the input connections.

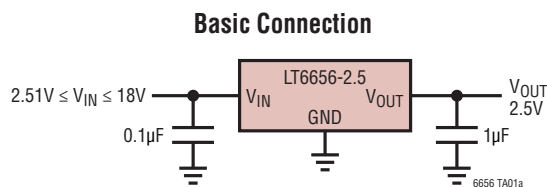
The LT6656 output is stable with 1 $\mu$ F or larger output capacitance and operates with a wide range of output capacitor ESR.

This reference is fully specified for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and is functional over the extreme temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Low hysteresis and a consistent temperature drift are obtained through advanced design, processing and packaging techniques.

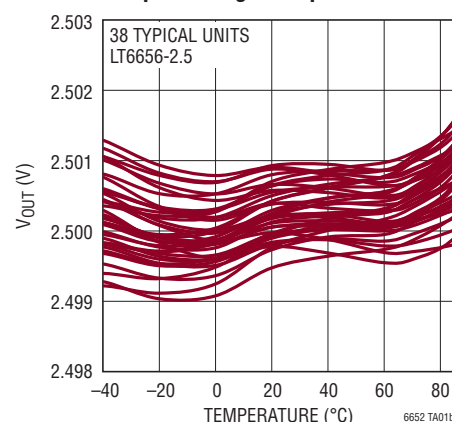
The LT6656 is offered in the 6-lead SOT-23, (2mm  $\times$  2mm) DFN, and 8-lead LS8 Packages. The LS8 is a 5mm  $\times$  5mm surface mount hermetic package that provides outstanding stability.

LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and ThinSOT is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.

## TYPICAL APPLICATION



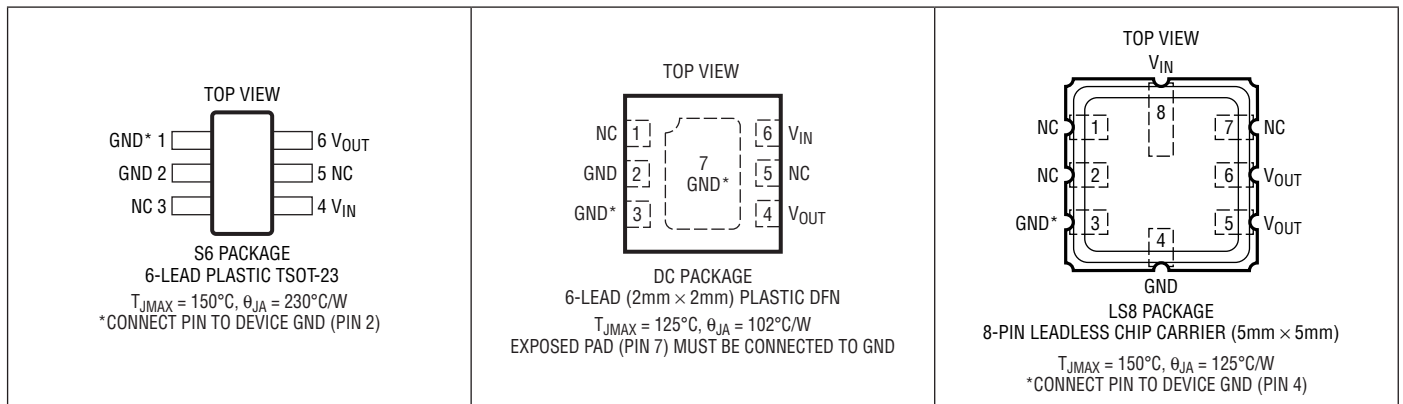
**Output Voltage Temperature Drift**



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage.....	±20V	Operating Temperature Range (Note 2)..	-55°C to 125°C
Output Voltage.....	-0.3V to 20V	Output Short Circuit Duration .....	Indefinite
Output Voltage Above Input Voltage .....	20V	Junction Temperature .....	150°C
Specified Temperature Range (Note 2)		Storage Temperature Range (Note 3).....	-65°C to 150°C
Commercial .....	0°C to 70°C	Lead Temperature (Soldering, 10 sec.)	
Industrial .....	-40°C to 85°C	TSOT-23 (Note 4).....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

### LEAD FREE FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6656ACS6-1.25#TRMPBF	LT6656ACS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-1.25#TRMPBF	LT6656BCS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-1.25#TRMPBF	LT6656AIS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-1.25#TRMPBF	LT6656BIS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACS6-2.048#TRMPBF	LT6656ACS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-2.048#TRMPBF	LT6656BCS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-2.048#TRMPBF	LT6656AIS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-2.048#TRMPBF	LT6656BIS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACS6-2.5#TRMPBF	LT6656ACS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-2.5#TRMPBF	LT6656BCS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-2.5#TRMPBF	LT6656AIS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-2.5#TRMPBF	LT6656BIS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACS6-3#TRMPBF	LT6656ACS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-3#TRMPBF	LT6656BCS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-3#TRMPBF	LT6656AIS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-3#TRMPBF	LT6656BIS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACS6-3.3#TRMPBF	LT6656ACS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-3.3#TRMPBF	LT6656BCS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-3.3#TRMPBF	LT6656AIS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-3.3#TRMPBF	LT6656BIS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	-40°C to 85°C

# ORDER INFORMATION

## LEAD FREE FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6656ACS6-4.096#TRMPBF	LT6656ACS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-4.096#TRMPBF	LT6656BCS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-4.096#TRMPBF	LT6656AIS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-4.096#TRMPBF	LT6656BIS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACS6-5#TRMPBF	LT6656ACS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-5#TRMPBF	LT6656BCS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-5#TRMPBF	LT6656AIS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656BIS6-5#TRMPBF	LT6656BIS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6656ACDC-1.25#TRMPBF	LT6656ACDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-1.25#TRMPBF	LT6656BCDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-1.25#TRMPBF	LT6656AIDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-1.25#TRMPBF	LT6656BIDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-2.048#TRMPBF	LT6656ACDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-2.048#TRMPBF	LT6656BCDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-2.048#TRMPBF	LT6656AIDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-2.048#TRMPBF	LT6656BIDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-2.5#TRMPBF	LT6656ACDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-2.5#TRMPBF	LT6656BCDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-2.5#TRMPBF	LT6656AIDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-2.5#TRMPBF	LT6656BIDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-3#TRMPBF	LT6656ACDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-3#TRMPBF	LT6656BCDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-3#TRMPBF	LT6656AIDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-3#TRMPBF	LT6656BIDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-3.3#TRMPBF	LT6656ACDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-3.3#TRMPBF	LT6656BCDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-3.3#TRMPBF	LT6656AIDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-3.3#TRMPBF	LT6656BIDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-4.096#TRMPBF	LT6656ACDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-4.096#TRMPBF	LT6656BCDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-4.096#TRMPBF	LT6656AIDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-4.096#TRMPBF	LT6656BIDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656ACDC-5#TRMPBF	LT6656ACDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-5#TRMPBF	LT6656BCDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-5#TRMPBF	LT6656AIDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6656BIDC-5#TRMPBF	LT6656BIDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	
LT6656AILS8-1.25#PBF†	656125	8-Lead (5mm × 5mm) Ceramic LCC	-40°C to 85°C	
LT6656BILS8-1.25#PBF†	656125	8-Lead (5mm × 5mm) Ceramic LCC	-40°C to 85°C	

TRM = 500 pieces. \*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeand reel/>

†This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

## AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	SPECIFIED TEMPERATURE RANGE	
			0°C TO 70°C	-40°C TO 85°C
			ORDER PART NUMBER*	ORDER PART NUMBER*
1.250V	0.05%	10ppm/°C	LT6656ACS6-1.25	LT6656AIS6-1.25
	0.05%	10ppm/°C	N/A	LT6656AILS8-1.25
	0.10%	20ppm/°C	LT6656BCS6-1.25	LT6656BIS6-1.25
	0.10%	10ppm/°C	LT6656ACDC-1.25	LT6656AIDC-1.25
	0.10%	15ppm/°C	N/A	LT6656BILS8-1.25
	0.20%	20ppm/°C	LT6656BCDC-1.25	LT6656BIDC-1.25
2.048V	0.05%	10ppm/°C	LT6656ACS6-2.048	LT6656AIS6-2.048
	0.10%	20ppm/°C	LT6656BCS6-2.048	LT6656BIS6-2.048
	0.10%	10ppm/°C	LT6656ACDC-2.048	LT6656AIDC-2.048
	0.20%	20ppm/°C	LT6656BCDC-2.048	LT6656BIDC-2.048
2.500V	0.05%	10ppm/°C	LT6656ACS6-2.5	LT6656AIS6-2.5
	0.10%	20ppm/°C	LT6656BCS6-2.5	LT6656BIS6-2.5
	0.10%	10ppm/°C	LT6656ACDC-2.5	LT6656AIDC-2.5
	0.20%	20ppm/°C	LT6656BCDC-2.5	LT6656BIDC-2.5
3.000V	0.05%	10ppm/°C	LT6656ACS6-3	LT6656AIS6-3
	0.10%	20ppm/°C	LT6656BCS6-3	LT6656BIS6-3
	0.10%	10ppm/°C	LT6656ACDC-3	LT6656AIDC-3
	0.20%	20ppm/°C	LT6656BCDC-3	LT6656BIDC-3
3.300V	0.05%	10ppm/°C	LT6656ACS6-3.3	LT6656AIS6-3.3
	0.10%	20ppm/°C	LT6656BCS6-3.3	LT6656BIS6-3.3
	0.10%	10ppm/°C	LT6656ACDC-3.3	LT6656AIDC-3.3
	0.20%	20ppm/°C	LT6656BCDC-3.3	LT6656BIDC-3.3
4.096V	0.05%	10ppm/°C	LT6656ACS6-4.096	LT6656AIS6-4.096
	0.10%	20ppm/°C	LT6656BCS6-4.096	LT6656BIS6-4.096
	0.10%	10ppm/°C	LT6656ACDC-4.096	LT6656AIDC-4.096
	0.20%	20ppm/°C	LT6656BCDC-4.096	LT6656BIDC-4.096
5.000V	0.05%	10ppm/°C	LT6656ACS6-5	LT6656AIS6-5
	0.10%	20ppm/°C	LT6656BCS6-5	LT6656BIS6-5
	0.10%	10ppm/°C	LT6656ACDC-5	LT6656AIDC-5
	0.20%	20ppm/°C	LT6656BCDC-5	LT6656BIDC-5

\*See Order Information section for complete part number listing.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = V_{OUT} + 0.5\text{V}$  (for LT6656-1.25,  $V_{IN} = 2.2\text{V}$ ),  $C_L = 1\mu\text{F}$ ,  $I_L = 0$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Error	LT6656ACS6, LT6656AIS6, LT6656AILS8	-0.05		0.05	%
	LT6656BCS6, LT6656BIS6, LT6656BILS8	-0.1		0.1	%
	LT6656ACDC, LT6656AIDC	-0.1		0.1	%
	LT6656BCDC, LT6656BIDC	-0.2		0.2	%
Output Voltage Temperature Coefficient (Note 5)	LT6656A	●	5	10	ppm/°C
	LT6656B	●	12	20	ppm/°C
Line Regulation	$V_{IN} = (V_{OUT} + 0.5\text{V})$ to 18V LT6656-2.048, LT6656-2.5, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●	2	25	ppm/V ppm/V
	$V_{IN} = 2.2\text{V}$ to 18V LT6656-1.25	●	2	25	ppm/V ppm/V
Load Regulation (Note 6)	$I_L = 5\text{mA}$ , Sourcing LT6656-2.048, LT6656-2.5, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●	65	150	ppm/mA ppm/mA
	$I_L = 5\text{mA}$ , Sourcing LT6656S6-1.25, LT6656DC-1.25	●	80	175	ppm/mA ppm/mA
	$I_L = 5\text{mA}$ , Sourcing LT6656LS8-1.25	●	135	250	ppm/mA ppm/mA
Dropout Voltage (Note 7)	$V_{IN} - V_{OUT}$ , $\Delta V_{OUT}$ Error $\leq 0.1\%$ $I_L = 0$ LT6656-2.048, LT6656-2.5, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●	3	10	mV mV
	$I_L = 5\text{mA}$ , Sourcing LT6656-2.048, LT6656-2.5, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●	250	370	mV mV
Minimum Input Voltage	$I_L = 0$ , $\Delta V_{OUT}$ Error $\leq 0.1\%$ LT6656-1.25	●	1.35	1.5	V
	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		1.6	V
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		1.8	V
Supply Current		●	0.85	1.0	$\mu\text{A}$ $\mu\text{A}$
Output Short Circuit Current	Short $V_{OUT}$ to GND		18		mA
	Short $V_{OUT}$ to $V_{IN}$		4		mA
Input Reverse Leakage Current	$V_{IN} = -18\text{V}$ , $V_{OUT} = \text{GND}$		80		$\mu\text{A}$
Reverse Output Current	$V_{IN} = \text{GND}$ , $V_{OUT} = 18\text{V}$		30		$\mu\text{A}$
Output Voltage Noise (Note 8)	0.1Hz to 10Hz		30		ppm <sub>P-P</sub>
	10Hz to 1kHz, LT6656-1.25		50		$\mu\text{V}_{\text{RMS}}$
	10Hz to 1kHz, LT6656-2.5		80		$\mu\text{V}_{\text{RMS}}$
	10Hz to 1kHz, LT6656-5		140		$\mu\text{V}_{\text{RMS}}$
Turn-On Time	LT6656-1.25, 0.1% Settling		15		ms
	LT6656-2.5, 0.1% Settling		30		ms
	LT6656-5, 0.1% Settling		60		ms
Long Term Drift of Output Voltage (Note 9)	LT6656S6, LT6656DC		50		ppm/ $\sqrt{\text{kHz}}$
	LT6656LS8		15		ppm/ $\sqrt{\text{kHz}}$
Hysteresis (Note 10)	LT6656S6, LT6656DC				
	$\Delta T = 0^\circ\text{C}$ to $70^\circ\text{C}$		25		ppm
	$\Delta T = -40^\circ\text{C}$ to $85^\circ\text{C}$		70		ppm
	LT6656LS8				
$\Delta T = 0^\circ\text{C}$ to $70^\circ\text{C}$		15		ppm	
$\Delta T = -40^\circ\text{C}$ to $85^\circ\text{C}$		55		ppm	

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT6656C is guaranteed to meet specified performance from 0°C to 70°C. The LT6656C is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6656I is guaranteed to meet specified performance from -40°C to 85°C. By design, the LT6656 is guaranteed functional over the operating temperature range of -55°C to 125°C.

**Note 3:** If the LT6656 is stored outside of the specified temperature range, the output may shift due to hysteresis.

**Note 4:** The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications section.

**Note 5:** Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

**Note 6:** Load regulation is measured with a pulse from no load to the specified load current. Output changes due to die temperature change must be taken into account separately.

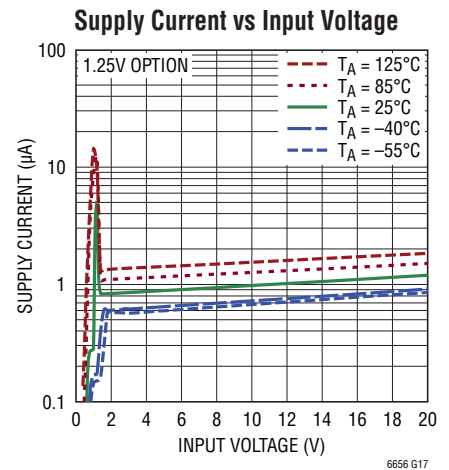
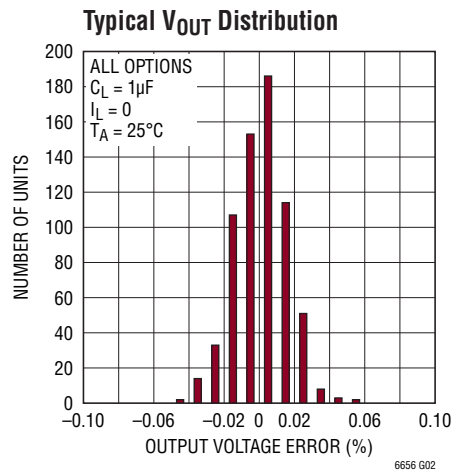
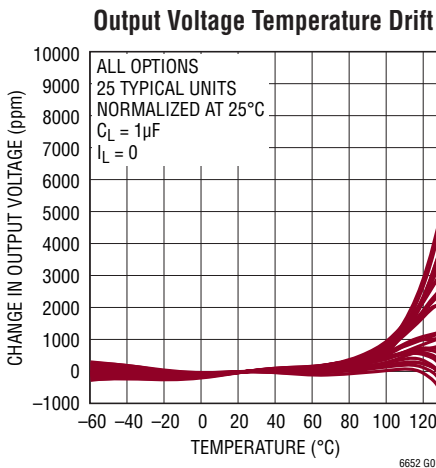
**Note 7:** Excludes load regulation errors.

**Note 8:** Peak-to-peak noise is measured with a 3-pole highpass filter at 0.1Hz and a 4-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. The test time is 10 seconds. RMS noise is measured on a spectrum analyzer in a shielded environment.

**Note 9:** Long term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly.

**Note 10:** Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature) hysteresis is usually not a dominant error source. Typical hysteresis is the worst-case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

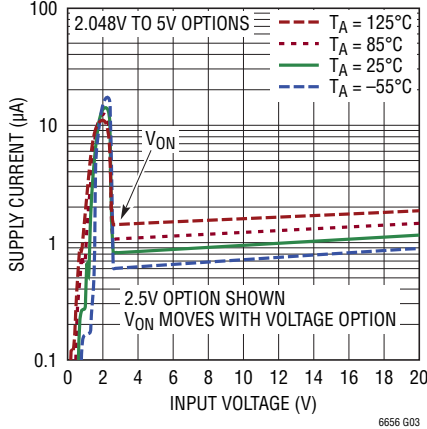
## TYPICAL PERFORMANCE CHARACTERISTICS



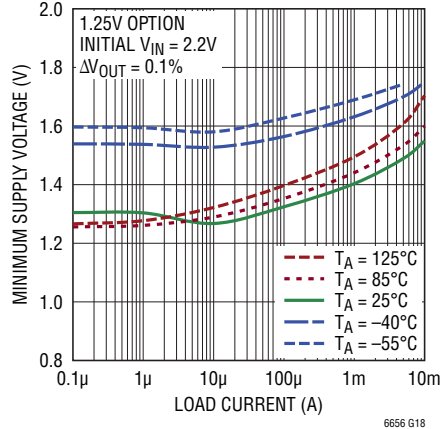


# TYPICAL PERFORMANCE CHARACTERISTICS

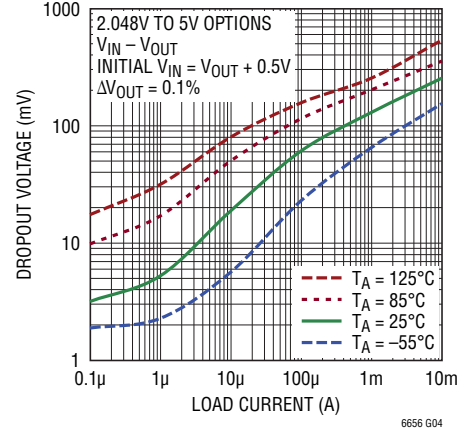
**Supply Current vs Input Voltage**



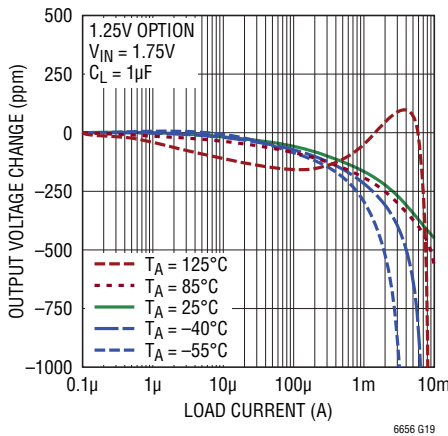
**Minimum Supply Voltage vs Load Current**



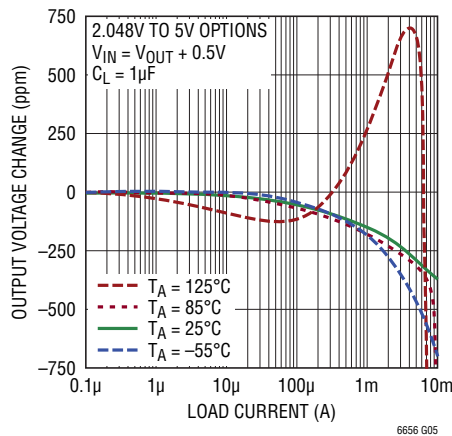
**Dropout Voltage vs Load Current**



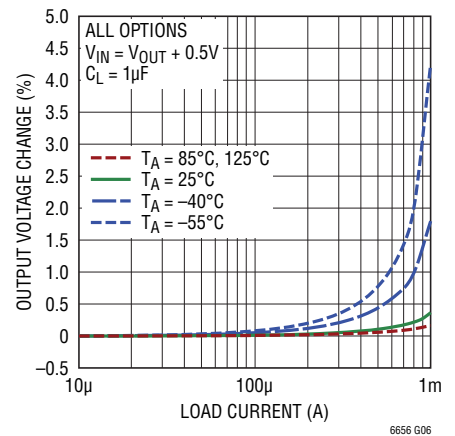
**Load Regulation (Sourcing)**



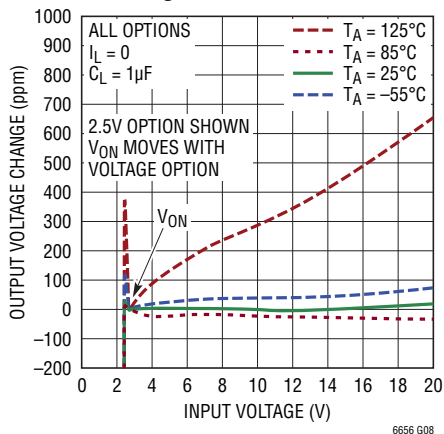
**Load Regulation (Sourcing)**



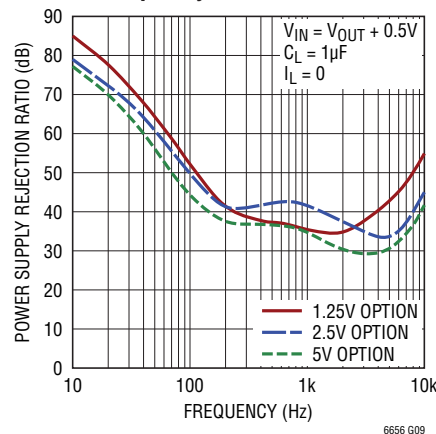
**Load Regulation (Sinking)**



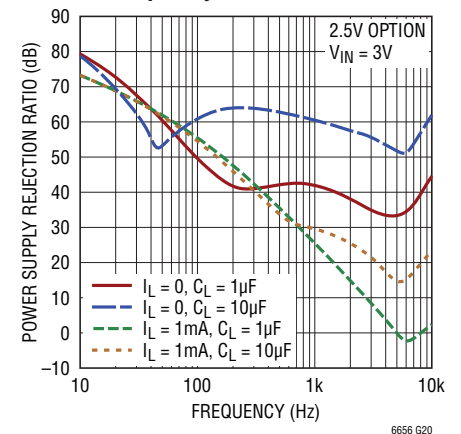
**Line Regulation**



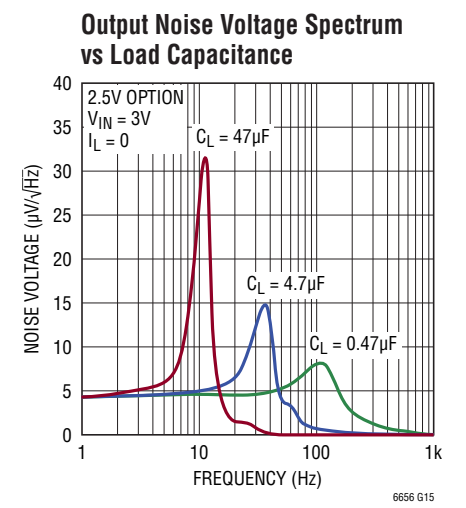
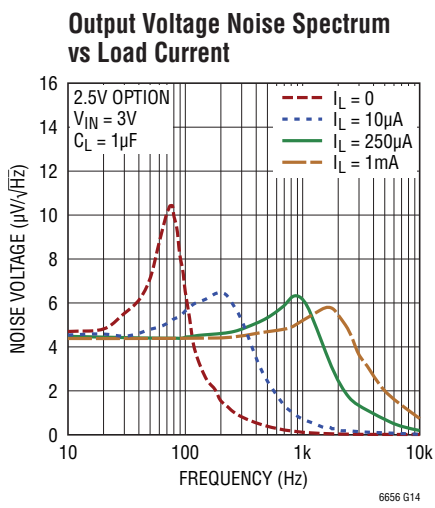
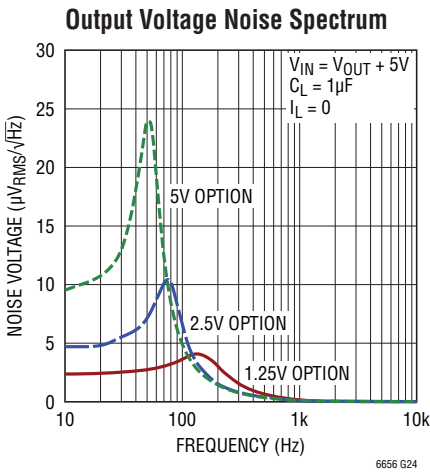
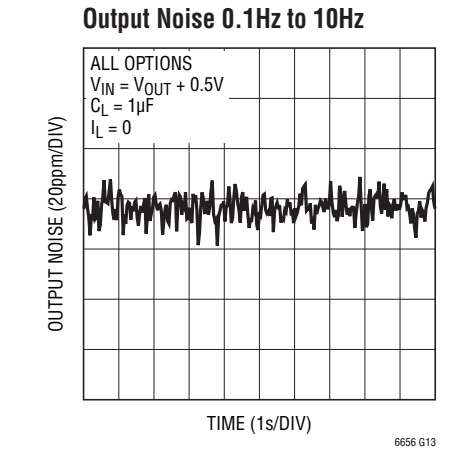
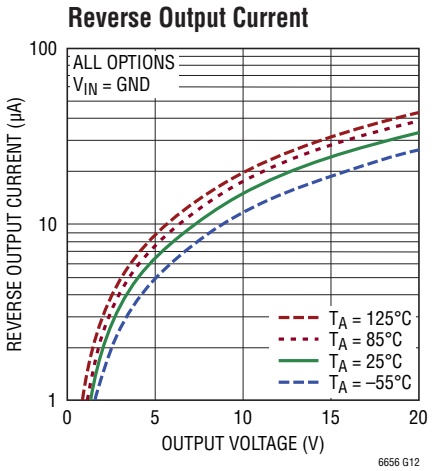
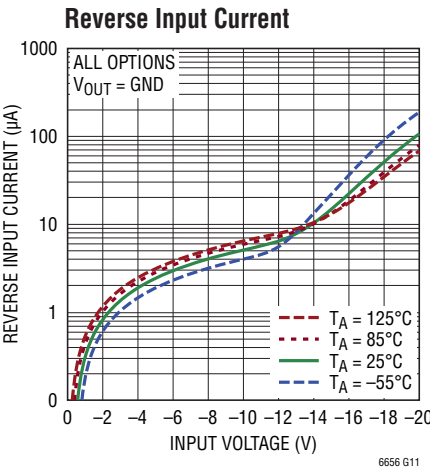
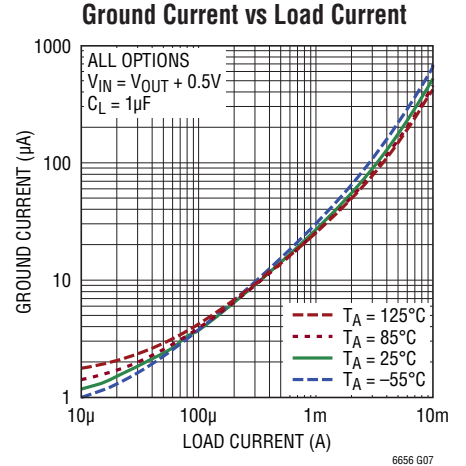
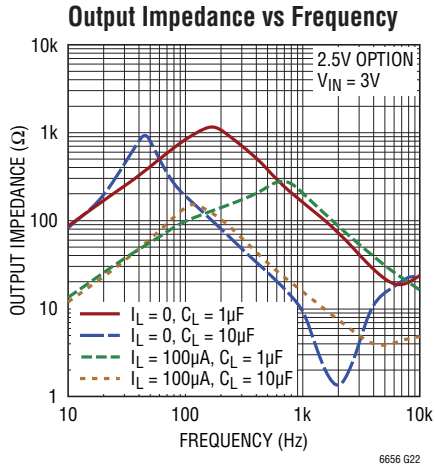
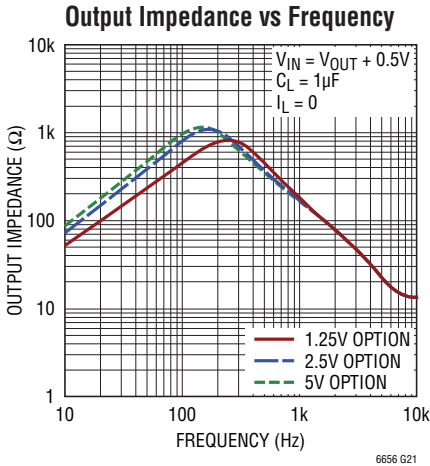
**Power Supply Rejection Ratio vs Frequency**



**Power Supply Rejection Ratio vs Frequency**



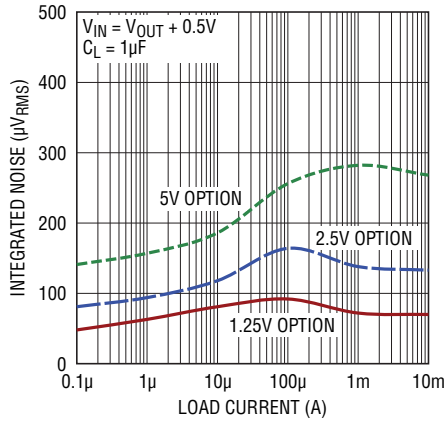
TYPICAL PERFORMANCE CHARACTERISTICS



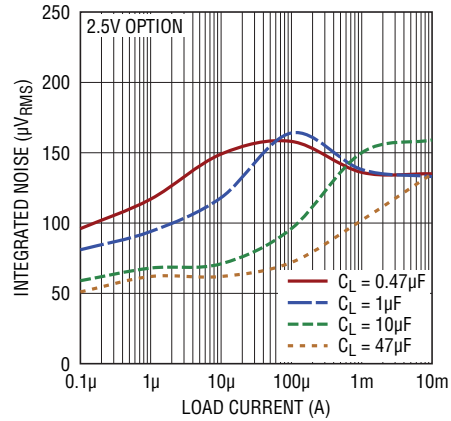


# TYPICAL PERFORMANCE CHARACTERISTICS

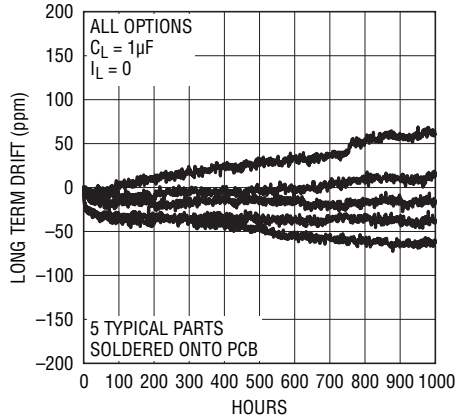
**Integrated 10Hz to 1kHz Noise vs Load Current**



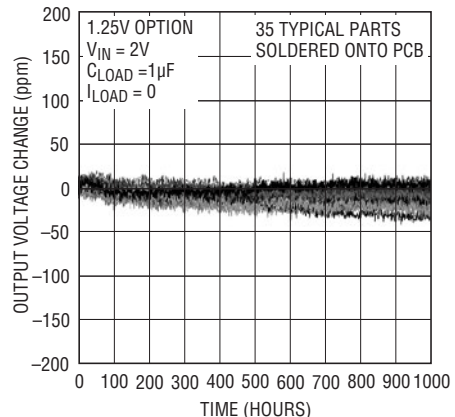
**Integrated 10Hz to 1kHz Noise vs Load Current**



**Long-Term Drift**



**Long-Term Drift (LS8)**



## PIN FUNCTIONS

### (TSOT-23/DFN)

**GND\* (Pin 1/Pin 3):** Internal Function. This pin must be tied to ground.

**GND (Pin 2/Pin 2):** Device Ground.

**NC (Pins 3, 5/Pins 1, 5):** Not Internally Connected. May be tied to  $V_{IN}$ ,  $V_{OUT}$ , GND or floated.

**$V_{IN}$  (Pin 4/Pin 6):** Power Supply. The minimum supply varies with output load and voltage option, see the Dropout Voltage specification in the Electrical Characteristics table for further details. The maximum input voltage is 18V. Bypass  $V_{IN}$  with a 0.1 $\mu$ F capacitor to ground.

**$V_{OUT}$  (Pin 6/Pin 4):** Output Voltage. A minimum output capacitor of 1 $\mu$ F is required for stable operation.

**GND\* (Exposed Pad Pin 7, DFN Only):** This pin must be tied to ground.

### (LS8)

**NC (Pins 1, 2, 7):** Not Internally Connected. May be tied to  $V_{IN}$ ,  $V_{OUT}$ , GND or floated.

**GND\* (Pin 3):** Internal Function. This pin must be tied to ground.

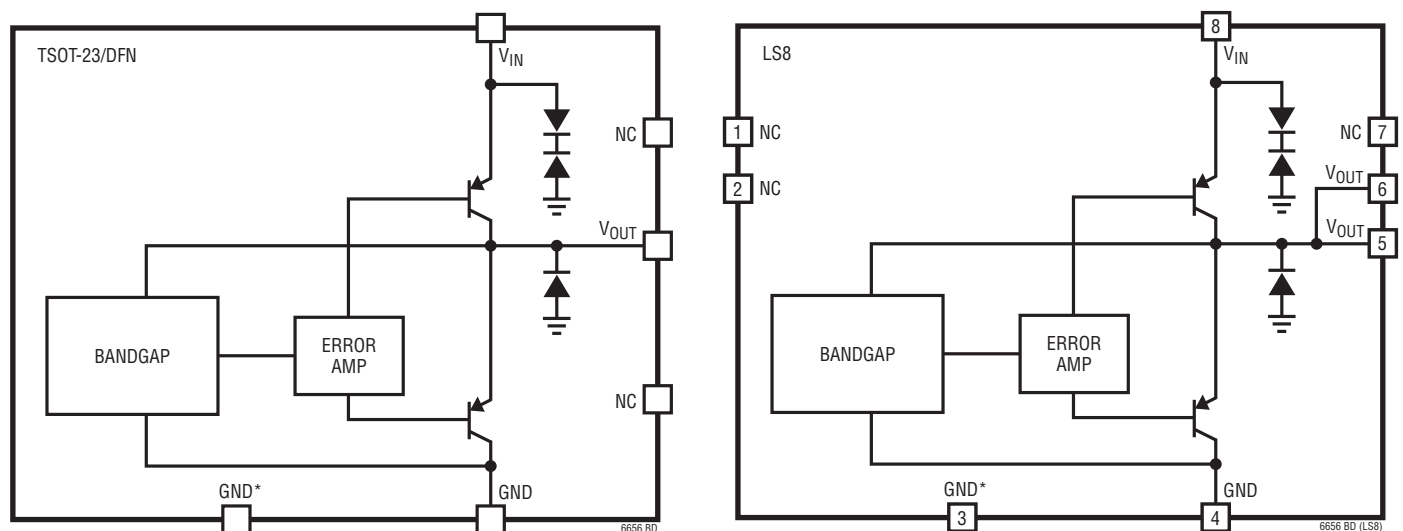
**GND (Pin 4):** Device Ground.

**$V_{OUT}$  (Pin 5):** Output Voltage. A minimum output capacitor of 1 $\mu$ F is required for stable operation.

**$V_{OUT}$  (Pin 6):** Output Voltage. Tie to pin 5 for best load regulation.

**$V_{IN}$  (Pin 8):** Power Supply. Bypass  $V_{IN}$  with a 0.1 $\mu$ F capacitor to ground.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Long Battery Life

Series references have a large advantage over shunt style references. Shunt references require a resistor from the power supply to operate. This resistor must be chosen to supply the maximum current that can be demanded by the load. When the load is not operating at this maximum current, the shunt reference must always sink this current, resulting in high dissipation and shortened battery life.

The LT6656 series reference does not require a current setting resistor and is specified to operate with any supply from 1.5V to 18V, depending on the output voltage option, load current and operating temperature (see Dropout Voltage and Minimum Input Voltage in the Typical Performance Characteristics). When the load does not demand current, the LT6656 reduces its dissipation and battery life is extended. If the reference is not delivering load current, it dissipates only a few  $\mu\text{W}$ , yet the same connection can deliver 5mA of load current when required.

### Start-Up

To ensure proper start-up, the output voltage should be between  $-0.3\text{V}$  and the rated output voltage. If the output load may be driven more than  $0.3\text{V}$  below ground, a low forward voltage schottky diode from the output to ground is required. The turn-on characteristics can be seen in Figure 1.

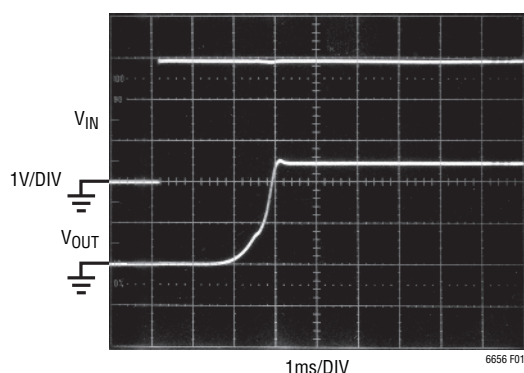


Figure 1. LT6656-2.5 Turn-On Characteristics,  $C_L = 1\mu\text{F}$

### Output Voltage Options

The performance of the LT6656 is consistent for the 2.048V to 5V options. The 1.25V option has slightly reduced load regulation, and unlike the higher voltage options, the minimum operating supply voltage is limited by internal circuitry rather than the output voltage.

Parameters that are based on changes in the output voltage, such as load regulation and hysteresis, remain proportional to the output voltage and are specified in relative units, for example, parts per million (ppm). Parameters that are not based on changes in the output voltage, such as supply current and reverse input current, are the same for all options.

The bandwidth of the LT6656 decreases with higher output voltage. This causes parameters that are affected by both bandwidth and output voltage, such as wideband noise and output impedance, to increase less with higher output voltage.

### Bypass and Load Capacitance

The LT6656 voltage reference needs a  $0.1\mu\text{F}$  input bypass capacitor placed within an inch of the input pin. An additional  $2.2\mu\text{F}$  capacitor should be used when the source impedance of the input supply is high or when driving heavy loads. The bypassing of other local devices may serve as the required components. The output of the LT6656 requires a capacitance of  $1\mu\text{F}$  or larger. The LT6656 is stable with a wide variety of capacitor types including ceramic, tantalum and electrolytic due to its low sensitivity to ESR ( $5\Omega$  or less).

The test circuit in Figure 2 was used to test the response and stability of the LT6656 to various load currents. The resultant transient responses can be seen in Figure 3 and Figure 4. The large scale output response to a 500mV input step is shown in Figure 5 with a more detailed photo and description in the Output Settling section.

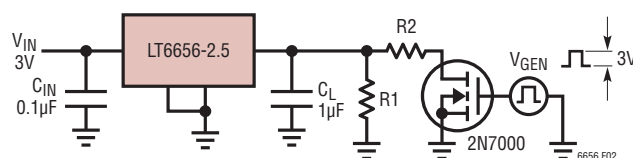


Figure 2. Transient Load Test Circuit

APPLICATIONS INFORMATION

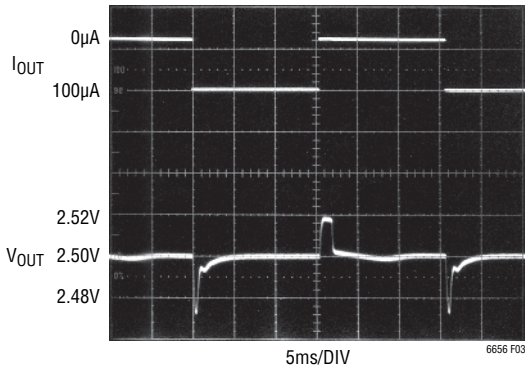


Figure 3. Transient Response, 0µA to 100µA Load Step (R2 = 24.9k, R1 = Open)

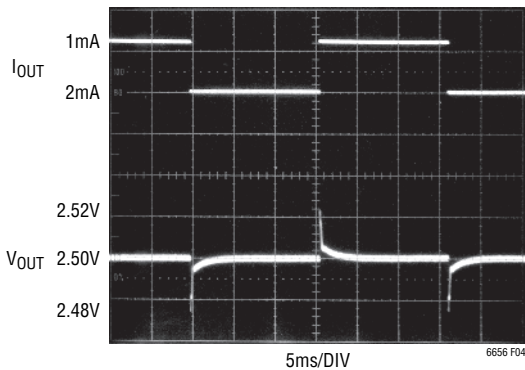


Figure 4. Transient Response, 1mA to 2mA Load Step (R1 = R2 = 2.49k)

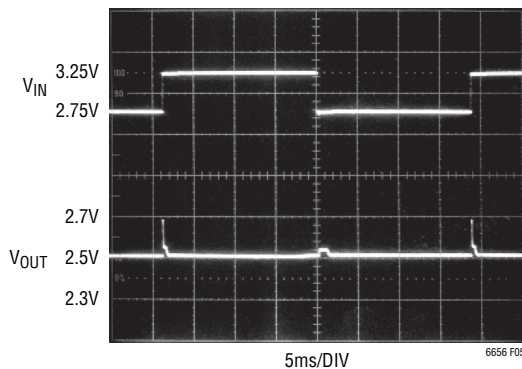


Figure 5. Output Response to 0.5Vp-p Step on VIN, CL = 1µF, IL = 0

Output Settling

The output of the LT6656 is primarily designed to source current into a load, but is capable of sinking current to aid in output transient recovery. The output stage uses a class B architecture to minimize quiescent current and has a crossover dead band as the output transitions from sourcing to sinking current.

The settling time is typically less than 8ms for output loads up to 5mA, however the time required to settle when the load is turned off or in response to an input transient can be significantly longer due to the dead band (shown in Figure 7). During this interval the output stage is neither sourcing nor sinking current so the settling time is dominated by the ability of the application circuit to discharge the output capacitor to the voltage at which the sourcing circuitry in the output stage reactivates. Larger load currents will decrease the settling time and higher output capacitance will increase the settling time.

In application circuits where the LT6656 is experiencing a load step greater than 5µA, such as an ADC reference and supply implementation, the settling time will typically remain less than 8ms, regardless of the output settling from a previous load step.

The settling time can be estimated by the following equation:

$$\text{Settling time} \approx \frac{2(\text{Deadband})(C_L)}{I_L} + (V_{OUT})(0.8\text{ms/V})$$

The deadband is ≈7mV for the 2.5V option, is proportional to the voltage option (i.e., ≈14mV for the 5V option) and can double due to variations in processing.

The graph in Figure 6 shows the settling time versus load step with no load and with a constant 2µA load applied. Note the settling time can be longer with load steps that are not large enough to activate the sinking side of the output stage.

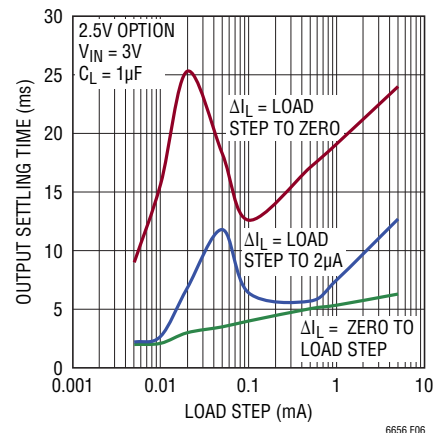
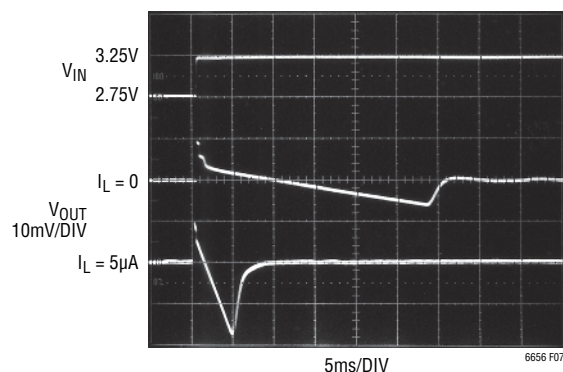


Figure 6. Output Settling Time to 0.05% vs Load Step

## APPLICATIONS INFORMATION



**Figure 7. Detailed Output Response to a 0.5V Input Step,  
 $C_{IN} = C_L = 1\mu F$**

The photo in Figure 7 shows the output response to a 0.5V input step in both a no-load and 5 $\mu$ A load condition. In the no-load condition only the bias current of the internal bandgap reference (about 400nA) is available to discharge the output capacitor.

### Output Noise

Low frequency noise is proportional to the output voltage and is insensitive to output current and moderate levels of output capacitance.

Wideband noise increases less with higher output voltage and is proportional to the bandwidth of the output stage, increasing with higher load current and lower output capacitance.

Peaking in the noise response is another factor contributing to the output noise level for a given frequency range. Noise peaking can be reduced by increasing the size of the output capacitor when driving heavier loads, or conversely, reducing the size of the output capacitor when driving lighter loads. Noise plots in the Typical Performance Curves section show noise spectrum with various load currents and output capacitances.

### Internal Protection

The LT6656 incorporates several internal protection features that make it ideal for use in battery powered systems. Reverse input protection limits the input current to typically less than 40 $\mu$ A when either the LT6656 or the battery is installed backwards. In systems where

the output can be held up by a backup battery with the input pulled to ground, the reverse output protection of the LT6656 limits the output current to typically less than 30 $\mu$ A. The current versus reverse voltage is shown in the Typical Performance Characteristics section.

### Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. A more realistic way to determine long-term drift is to measure it over the time interval of interest. The LT6656 drift data was taken over 100 parts that were soldered onto PC boards in a typical application configuration. The boards were then placed into a constant temperature oven with  $T_A = 30^\circ\text{C}$ , their outputs scanned regularly and measured with an 8.5 digit DVM. The parts chosen in the Long Term Drift curves in the Typical Performance Characteristics section represent high, low and typical units.

### Hysteresis

Hysteresis on the LT6656 is measured in two steps, for example, from 25 $^\circ\text{C}$  to -40 $^\circ\text{C}$  to 25 $^\circ\text{C}$ , then from 25 $^\circ\text{C}$  to 85 $^\circ\text{C}$  to 25 $^\circ\text{C}$ , for the industrial temperature range. After preconditioning by one thermal cycle, this two-step cycle is repeated several times and the maximum hysteresis from all the partial cycles is noted.

Results over both commercial and industrial temperature ranges are shown in Figure 8 and Figure 9. The parts cycled over the higher temperature range have a higher hysteresis than those cycled over the lower range.

### Power Dissipation

The LT6656 will not exceed the maximum junction temperature when operating within its specified temperature range of -40 $^\circ\text{C}$  to 85 $^\circ\text{C}$ , maximum input voltage of 18V and specified load current of 5mA.

### IR Reflow Shift

The different expansion and contraction rates of the materials that make up the LT6656 package may induce small stresses on the die that can cause the output to shift during

APPLICATIONS INFORMATION

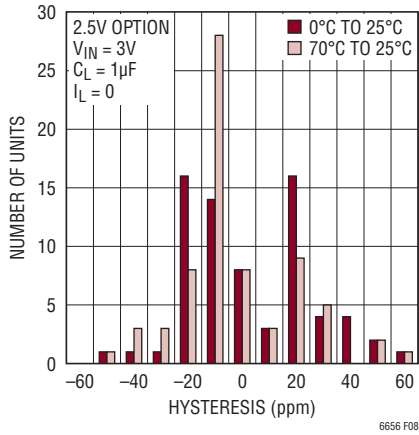


Figure 8. LT6656 S6, DC 0°C to 70°C Hysteresis

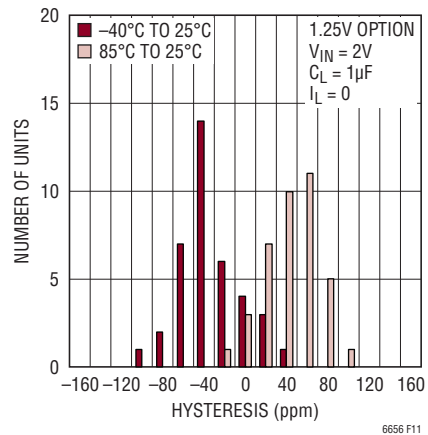


Figure 11. LT6656 LS8 -40°C to 85°C Hysteresis

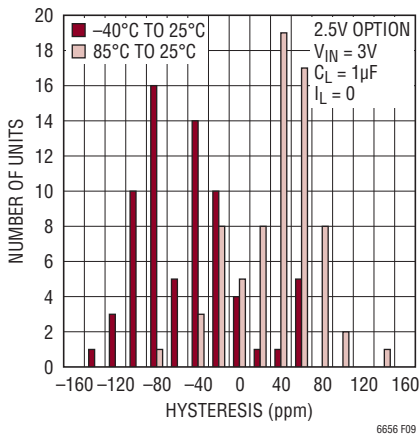


Figure 9. LT6656 S6, DC -40°C to 85°C Hysteresis

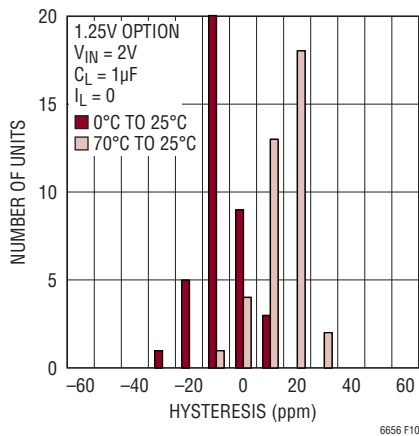


Figure 10. LT6656 LS8 0°C to 70°C Hysteresis

IR reflow. Common lead free IR reflow profiles reach over 250°C, considerably more than lead solder profiles. The higher reflow temperature of the lead free parts exacerbates the issue of thermal expansion and contraction causing the output shift to generally be greater than with a leaded reflow process.

The lead free IR reflow profile used to experimentally measure the output voltage shift in the LT6656-2.5 is shown in Figure 12. Similar results can be expected using a convection reflow oven. Figures 13 and 14 show the change in output voltage that was measured for parts that were run through the reflow process for 1 cycle and also 3 cycles. Additional drift of the LT6656 after IR reflow does not vary significantly.

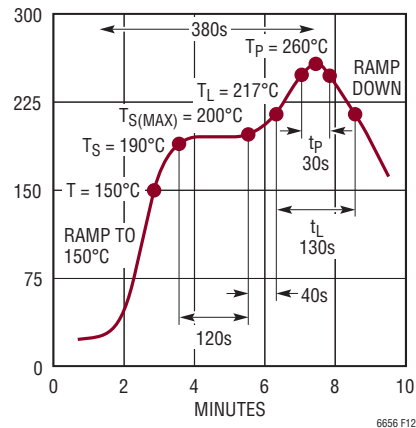
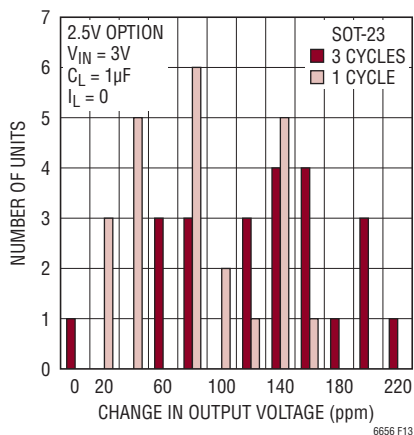


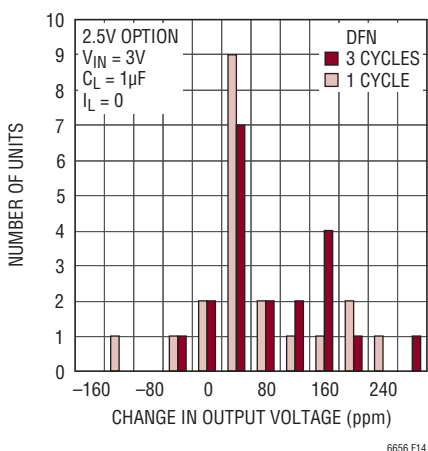
Figure 12. Lead Free Reflow Profile Due to IR Reflow



## APPLICATIONS INFORMATION



**Figure 13.  $\Delta V_{OUT}$  Due to IR Reflow, Peak Temperature = 260°C, SOT-23**



**Figure 14.  $\Delta V_{OUT}$  Due to IR Reflow, Peak Temperature = 260°C, DFN**

### PC Board Layout

The mechanical stress of soldering a surface mount voltage reference to a PC board can cause the output voltage to shift and temperature coefficient to change.

To reduce the effects of stress-related shifts, position the reference near the short edge of the PC board or in a corner. In addition, slots can be cut into the board on two sides of the device. See Application Note AN82 for more information. <http://www.linear.com>

The input and output capacitors should be mounted close to the package. The GND and  $V_{OUT}$  traces should be as

short as possible to minimize the voltage drops caused by load and ground currents. Excessive trace resistance directly impacts load regulation.

### Humidity Sensitivity

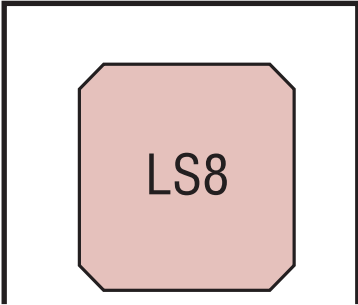
Plastic mold compounds absorb water. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside, which can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern. However, PC board material may absorb water and apply mechanical stress to the LT6656LS8. Proper board materials and layout are essential.

For best stability, the PC board layout is critical. Change in temperature and position of the PC board, as well as aging, can alter the mechanical stress applied to components soldered to the board. FR4 and similar materials also absorb water, causing the board to swell. Even conformal coating or potting of the board does not always eliminate this effect, though it may delay the symptoms by reducing the rate of absorption. Removing power and ground planes in the PC board under the voltage reference can improve the stability significantly.

Figure 15a shows a tab cut through the PC board on three sides of an LT6656, which significantly reduces stress on the IC, as described in Application Note 82. For even better performance, Figure 15b shows slots cut through the PC board on all four sides. The slots should be as long as possible, and the corners just large enough to accommodate routing of traces. It has been shown that for PC boards designed in this way, humidity sensitivity can be reduced to less than 35ppm for a change in relative humidity of approximately 60%. Mounting the reference near the center of the board, with slots on four sides, can further reduce the sensitivity to less than 10ppm.

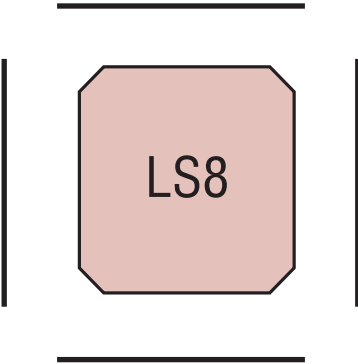
An additional advantage of slotting the PC board is that the LT6656 is thermally isolated from surrounding circuitry. This can help reduce thermocouple effects and improve accuracy.

**APPLICATIONS INFORMATION**



6656 F15a

**Figure 15a. 3-Sided PCB Cutout**



6656 F12b

**Figure 15b. 4-Sided PCB Cutout**

## TYPICAL APPLICATIONS

### Regulator Reference

The robust input and output of the LT6656 along with its high output current make it an excellent precision low power regulator as well as a reference. The LT6656 would be a good match with a small, low power microcontroller. Using the LT6656 as a regulator reduces power consumption, decreases solution size and increases the accuracy of the microcontroller's on board ADC.

### Low Power ADC Reference

Low power ADCs draw only a few  $\mu\text{A}$ s during their idle period and well over  $100\mu\text{A}$  during conversions. Despite these surges of current, the ADC in reality can have very low power consumption. Figure 17 shows the LTC2480, a low power delta sigma ADC. When the ADC is disabled its quiescent current ( $I_Q$ ) is roughly  $1\mu\text{A}$ , during conversion the  $I_Q$  jumps up to  $160\mu\text{A}$ . In reality, the power consumption is not only based on the  $I_Q$  during conversion, but the real power consumption of the ADC is set by the conversion time and the sample rate. The LTC2480 shown in Figure 17 has a conversion time of 160ms which sets the maximum sample rate of 6 samples per second. The maximum sample rate also sets the maximum current consumption to  $160\mu\text{A}$ , but at slower sample rates the ADC will have significantly lower average current draw. If the ADC is sampled at 1 sample per second the average current drawn by the ADC during a 1 second interval would only be  $26.4\mu\text{A}$ . When taking into consideration the current drawn by the reference, the total current draw is

only  $27.4\mu\text{A}$ . This system is greatly simplified because the precision reference does not need to be cycled on and off to save power. Furthermore, leaving the reference on continuously eliminates concern for turn-on settling time.

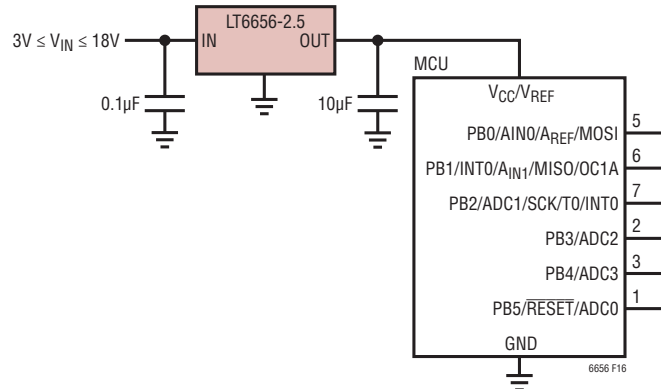


Figure 16. Microcontroller Reference and Regulator

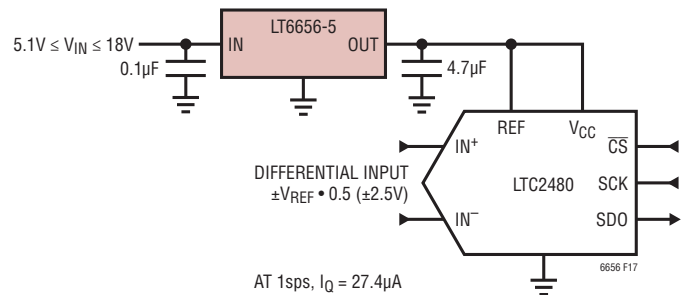
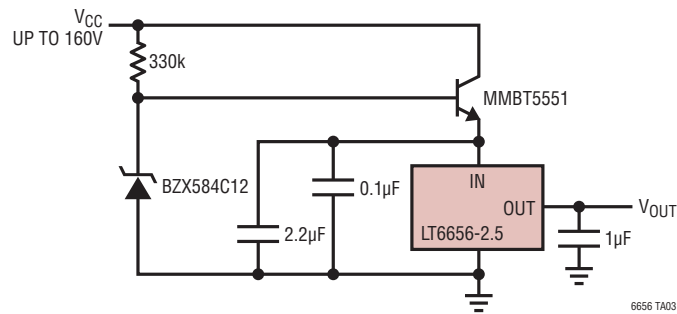


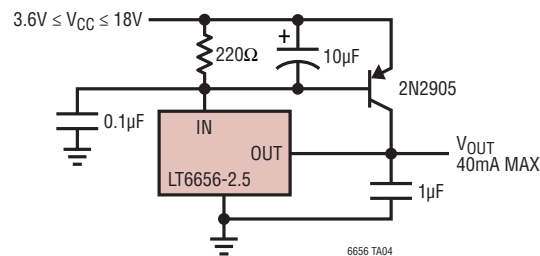
Figure 17. Low Power ADC Reference

## TYPICAL APPLICATIONS

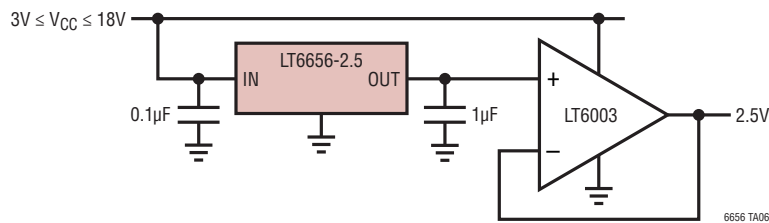
### Extended Supply Range Reference



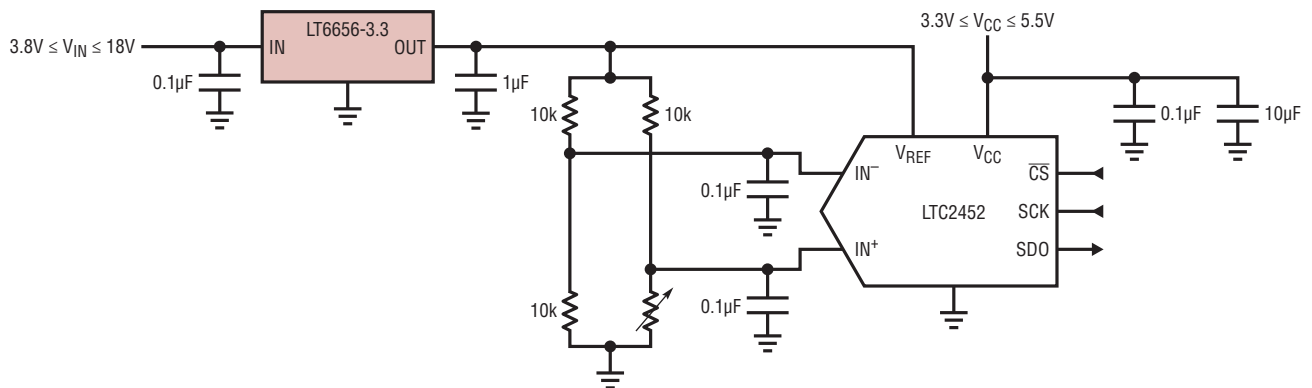
### Boosted Output Current Reference



### Micropower Regulator, $I_Q = 2\mu A$ , Sink Up to 8mA

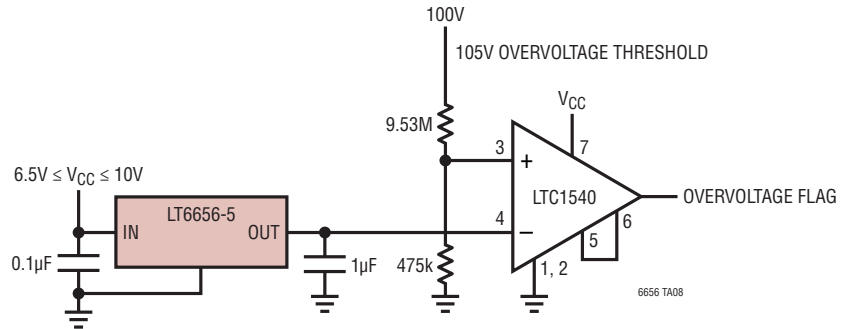


### ADC Reference and Bridge Excitation Supply

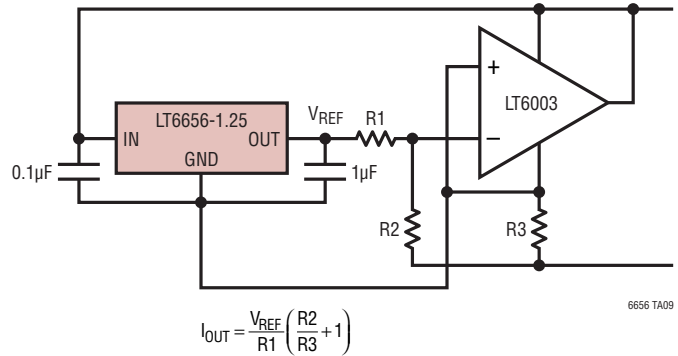


# TYPICAL APPLICATIONS

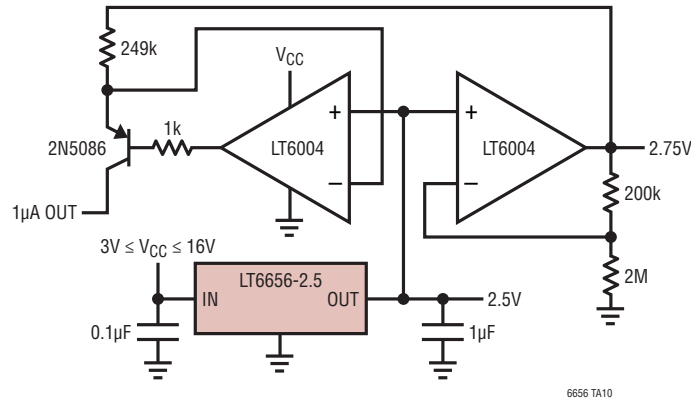
Low Power Precision High Voltage Supply Monitor,  $I_Q = 1.4\mu A$ , High Voltage Supply Load =  $10\mu A$



## 2-Terminal Current Source



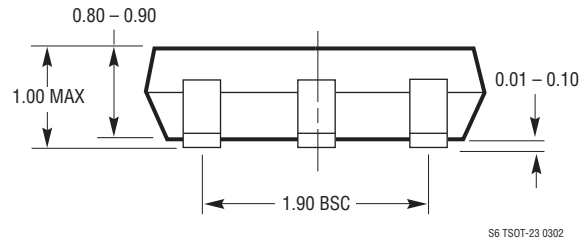
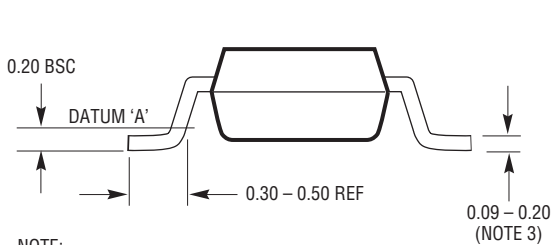
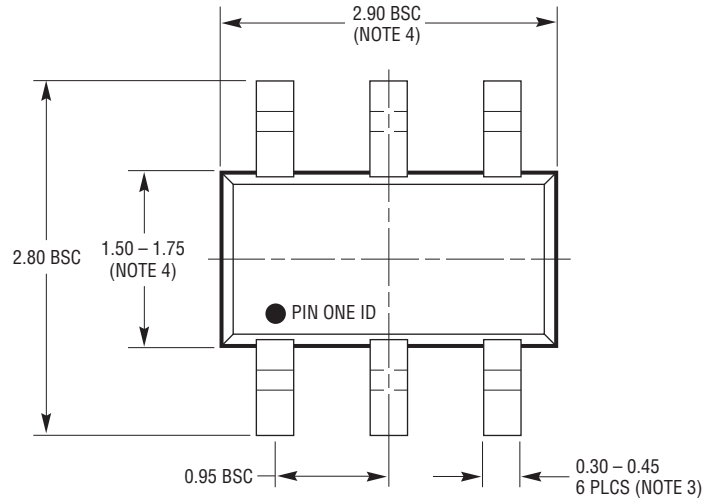
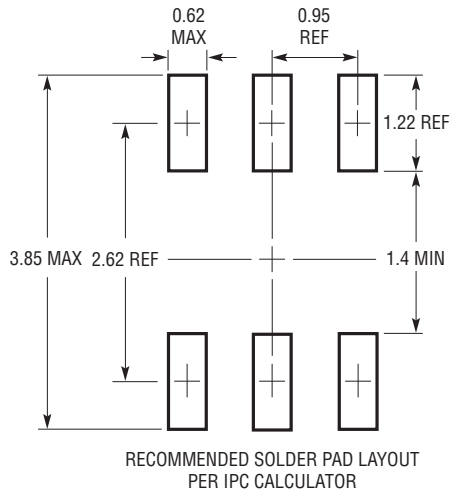
## Precision Current and Boosted Reference, $I_Q = 5.5\mu A$



# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## S6 Package 6-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1636)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

S6 TSOT-23 0302

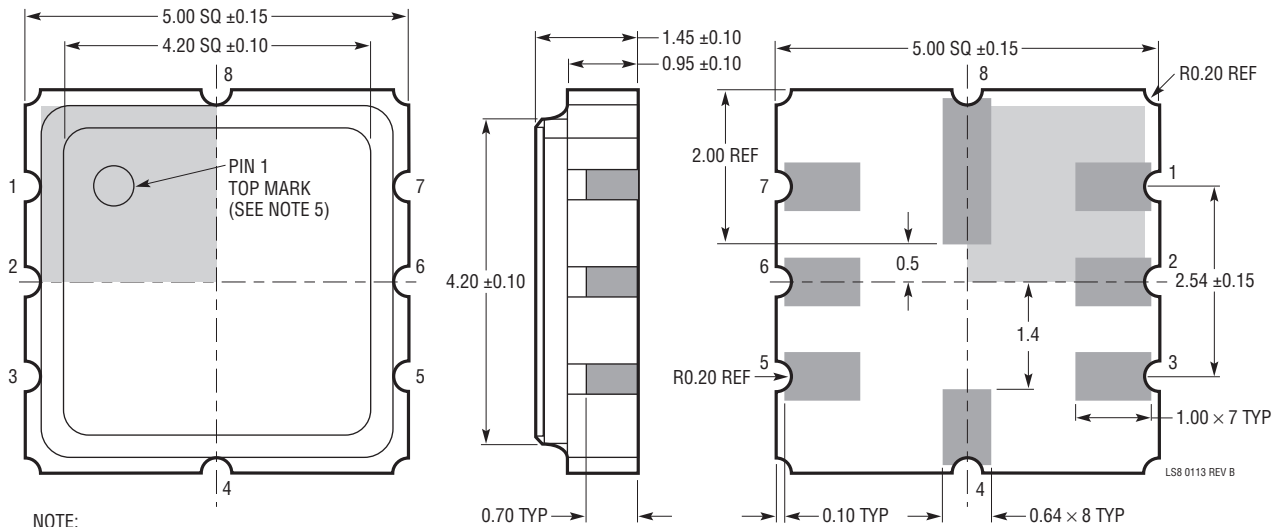
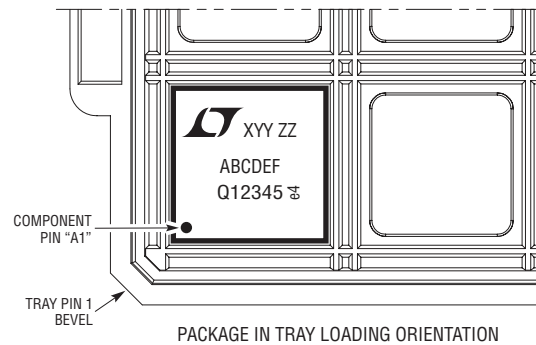
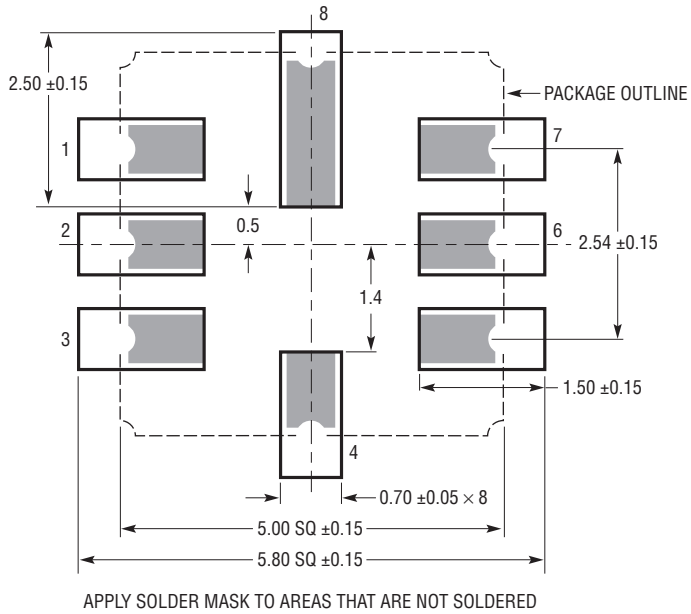




# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## LS8 Package 8-Pin Leadless Chip Carrier (5mm × 5mm) (Reference LTC DWG # 05-08-1852 Rev B)



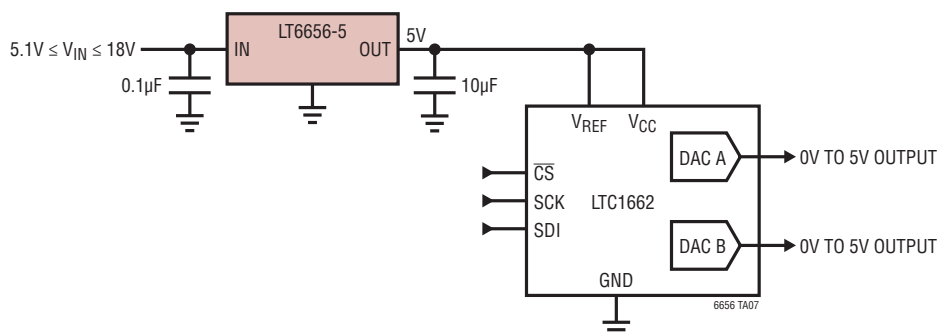
- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS  
PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
  4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
  5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/10	Voltage options added (1.25, 2.048, 3, 3.3), reflected throughout the data sheet	1 to 18
B	5/11	Added 6-lead DFN package reflected throughout the data sheet	1 to 20
C	11/13	Addition of 1.25V option in the LS8 package	1 to 4
		Note 10 updated with additional explanation of hysteresis	6
		Pin Functions updated to show pin numbers and LS8 package	10
		Block Diagram updated to show pin numbers and LS8 package	10
		Hysteresis section updated with additional explanation	13
		Hysteresis graphs updated for SOT23 and LS8 packages	14
		New section added for Humidity Sensitivity	15, 16

## TYPICAL APPLICATION

Reference Regulator for Micropower DAC, Total  $I_Q = 4.8\mu A$



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LT1389</a>	Nanopower Precision Shunt Voltage Reference	0.05% Max 10ppm/°C Max, 800nA Supply
<a href="#">LTC1440</a>	Micropower Comparator with Reference	3.7µA Max Supply Current, 1% 1.182V Reference, MSOP, PDIP and SO-8 Packages
<a href="#">LT1460</a>	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages
<a href="#">LT1461</a>	Micropower Precision LDO Series Reference	3ppm/°C Max Drift, 0°C to 70°C, -40°C to 85°C, -40°C to 125°C Options in SO-8
<a href="#">LT1495</a>	1.5µA Precision Rail-to-Rail Dual Op Amp	1.5µA Max Supply Current, 100pA Max IOS
<a href="#">LTC1540</a>	Nanopower Comparator with Reference	600nA Max Supply Current, 2% 1.182V Reference, MSOP and SO-8 Packages
<a href="#">LT1634</a>	Micropower Precision Shunt Voltage Reference	0.05% Max, 10ppm/°C Max Drift, 1.25V, 2.5V, 4.096V, 5V, 10µA Maximum Supply Current
<a href="#">LT1790</a>	Micropower Precision Series Reference	0.05% Max, 10ppm/°C Max, 60µA Supply, SOT23 Package
<a href="#">LTC1798</a>	6µA Low Dropout Series Reference	Available in Adjustable, 2.5V, 3V, 4.096V and 5V
<a href="#">LT6003</a>	1.6V, 1µA Precision Rail-to-Rail Op Amp	1µA Max Supply Current, 1.6V Minimum Operating Voltage, SOT-23 and DFN Packages
<a href="#">LT6650</a>	Micropower Reference with Buffer Amplifier	0.05% Max, 5.6µA Supply, SOT-23 Package
<a href="#">LT6660</a>	Tiny Micropower Series Reference	0.2% Max, 20ppm/°C Max, 20mA Output Current, 2mm × 2mm DFN
<a href="#">LT6700</a>	Micropower, Low Voltage Dual Comparator with 40mV Reference	6.5µA Supply Current, 1.4V Minimum Operating Voltage





MOISTURE SENSITIVITY LEVEL FOR SURFACE MOUNT PACKAGE				
PACKAGE CATEGORY	DESCRIPTION (SURFACE MOUNT PACKAGE)	LTC Designated Package Codes	J-STD-020 MSL	Dry Pack Required?
SO	8 LEAD SO	S8	1	No
	8 LEAD SO EXPOSED PAD	S8E	3	Yes
	14 LEAD SO	S	1	No
	16 LEAD SO (NARROW)	S	1	No
	16, 18, 20, 24, 28 LEAD SO (WIDE)	SW	1	No
SOT	3 LEAD SOT-23	S3	1	No
	4 LEAD SOT-23	S4	1	No
	3 LEAD SOT-223	ST	1	No
	5 LEAD TSOT	S5	1	No
	6 LEAD TSOT	S6	1	No
	8 LEAD TSOT	TS8	1	No
SSOP	16, 20, 24, 28 LEAD SSOP (NARROW)	GN	1	No
	16, 20, 24, 28, 36, 44, 48 LEAD SSOP	G	1	No
	36, 44 LEAD SSOP (WIDE)	GW	1	No
TQFP	32 LEAD TQFP	LU	TBQ	TBQ
	32 LEAD TQFP EXPOSED PAD	LUE	TBQ	TBQ
TSSOP	14, 20 LEAD TSSOP (4.4mm)	F	1	No
	48 LEAD TSSOP (6.1mm)	FW	1	No
	56 LEAD TSSOP (6.1mm)	FW	1	No
	16, 20, 24, 28, 38 LEAD TSSOP (4.4mm) EXPOSED DIE PAD	FE	1	No
	38 LEAD TOP EXPOSED PAD TSSOP (4.4mm)	FTE	1	1
UTDFN	8 LEAD UTDFN (2mm x 2mm)	KC	1	No
	10 LEAD UTDFN (3mm x 3mm)	KD	1	No
	14 LEAD UTDFN (4mm x 4mm)	KE	1	No
UTQFN	16, 20 LEAD UTQFN (3mm x 3mm)	PD	1	No
	20 LEAD UTQFN (3mm x 4mm)	PDC	1	No
	24, 28 LEAD UTQFN (4mm x 4mm)	PF	1	No
NOTES:	Peak Body Reflow Temperature determined per JEDEC J-STD-020. + Requires dry pack. & May observe delamination; classified MSL 1 per J-STD-020 Annex A Reliability Assessment. * Hermetic package, not moisture sensitive.			



## Tape and Reel Specifications—Surface Mount for LTCXXXX, LTXXXX, LTMXXXX PRODUCTS

### Tape and Reel Packing


Tape and reel packing is available for all SO, TSOT (thin SOT-23), SOT-23 3L/4L, SOT-223, SSOP, TSSOP, QFN, DFN and DD packages in accordance with EIA Specification 481-D with the following exceptions: **(DFN(DCB), TSOT and SC70 pin 1 is placed into quadrant 2. The pin 1 quadrant graphic “” is added onto the reel and pizza box labels. For square QFN as non-compliant to Figure 2 in the EIA-481 rev. D, but LTC will follow the Flow Chart for the Rules in Figure 3).**

Table 1 lists the applicable tape widths, dimensions and quantities for all LTC surface mount products. Consult a

sales office for tape and reel pricing and minimum order requirements. **Tape and reel packaging is ordered with a ‘#TRPBF’ suffix for lead free finish parts or a ‘#TR’ suffix for lead based finish parts.**

**\*Packages marked with an asterisk (\*) below are available in 500 unit reels through designated sales channels. 500 unit reels are ordered with a ‘#TRMPBF’ or ‘#TRM’ suffix.**

**\*\*Tape Widths marked with a double asterisk (\*\*) converted to 8mm width in July 2007.**

**Table 1. Tape and Reel Specifications**

LTC Package Code Designator	LTC Package Type	Number of Leads Offered	W Tape Width	P <sub>1</sub> Component Pitch	P <sub>0</sub> Hole Pitch	Reel Diameter	Units per Reel
DC*	DFN (2mm × 2mm)	3, 4, 6, 8	8/12mm**	4mm	4mm	180mm (7")	2,500*
DCB*	DFN (2mm × 3mm)	6, 8	8/12mm**	4mm	4mm	180mm (7")	2,500*
DD	DFN (3mm × 3mm)	8, 10, 12	12mm	8mm	4mm	330mm (13")	2,500
DDB*	DFN (3mm × 2mm)	8, 10, 12	8/12mm**	4mm	4mm	180mm (7")	2,500*
DE, UE	DFN (4mm × 3mm)	12, 14	12mm	8mm	4mm	330mm (13")	2,500
DF	DFN (4mm × 4mm)	12	12mm	8mm	4mm	330mm (13")	2,500
DH	DFN (5mm × 5mm)	16	12mm	8mm	4mm	330mm (13")	2,500
DHC	DFN (5mm × 3mm)	16	12mm	8mm	4mm	330mm (13")	2,500
DHD	DFN (5mm × 4mm)	16	12mm	8mm	4mm	330mm (13")	2,500
DJC	DFN (6mm × 3mm)	22	16mm	8mm	4mm	330mm (13")	2,500
DKD	DFN (7mm × 4mm)	24, 32	16mm	8mm	4mm	330mm (13")	2,500
F	TSSOP (4.4mm)	14, 20	16mm	8mm	4mm	330mm (13")	2,500
FE	TSSOP (4.4mm)	16, 20, 24	16mm	8mm	4mm	330mm (13")	2,500
FE	TSSOP (4.4mm)	28, 38	16mm	12mm	4mm	330mm (13")	2,000
FW	TSSOP (6.1mm)	48, 56	24mm	12mm	4mm	330mm (13")	1,800
G	SSOP (5.3mm)	16	16mm	12mm	4mm	330mm (13")	2,000
G	SSOP (5.3mm)	20, 24	16mm	12mm	4mm	330mm (13")	1,800
G	SSOP (5.3mm)	28, 36, 44, 48	24mm	12mm	4mm	330mm (13")	2,000
GN	SSOP (0.150)	16	12mm	8mm	4mm	330mm (13")	2,500
GN	SSOP (0.150)	20, 24, 28	16mm	8mm	4mm	330mm (13")	2,500
GW	SSOP (7.62mm)	36, 44	24mm	12mm	4mm	330mm (13")	1,000
KC	UTDFN (2mm × 2mm)	8	8mm	8mm	4mm	180mm (7")	2,500
KD	UTDFN (3mm × 3mm)	10	12mm	8mm	4mm	330mm (13")	2,500
KE	UTDFN (4mm × 3mm)	14	12mm	8mm	4mm	330mm (13")	2,500
M, Q, R	DD	3, 5 or 7	24mm	16mm	4mm	330mm (13")	750
MS8, MS8E	MSOP (0.118)	8	12mm	8mm	4mm	330mm (13")	2,500

# TAPE AND REEL

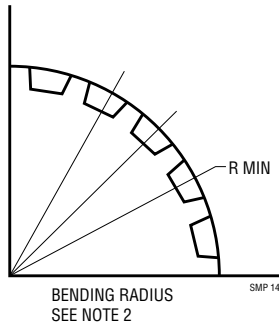
## TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT

Table 1. Tape and Reel Specifications (cont)

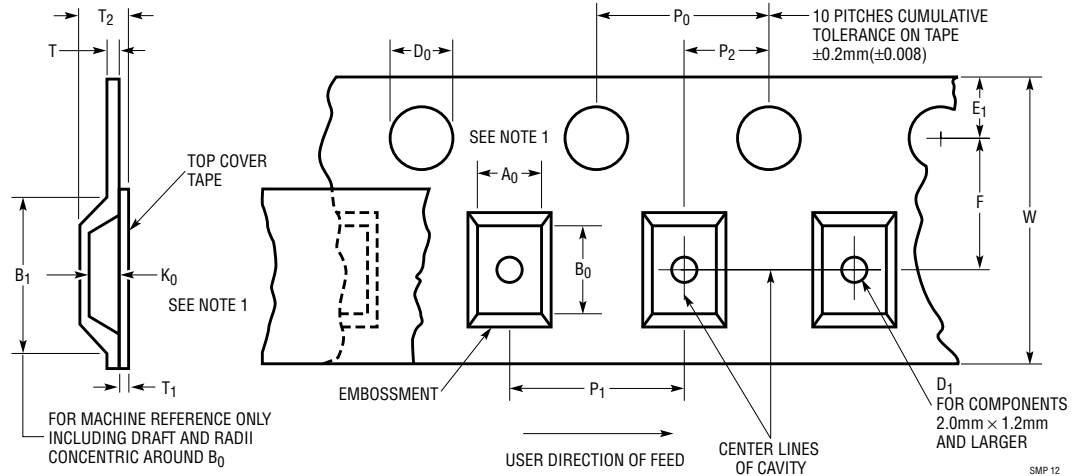
LTC Package Code Designator	LTC Package Type	Number of Leads Offered	W Tape Width	P <sub>1</sub> Component Pitch	P <sub>0</sub> Hole Pitch	Reel Diameter	Units per Reel
MS, MSE	MSOP (0.118)	10, 12, 16	12mm	8mm	4mm	330mm (13")	2,500
PD	UTQFN (3mm × 3mm)	16	12mm	8mm	4mm	330mm (13")	2,500
PDC	UTQFN (3mm × 4mm)	20	12mm	8mm	4mm	330mm (13")	2,500
PF	UTQFN (4mm × 4mm)	24, 28	12mm	8mm	4mm	330mm (13")	2,500
S8, S8E	SO (0.150)	8	12mm	8mm	4mm	330mm (13")	2,500
S	SO (0.150)	14	16mm	8mm	4mm	330mm (13")	2,500
S	SO (0.150)	16	16mm	8mm	4mm	330mm (13")	2,500
ST	SOT-223	3	16mm	12mm	4mm	330mm (13")	2,000
SW	SO (0.300)	16	16mm	12mm	4mm	330mm (13")	1,000
SW	SO (0.300)	18	24mm	12mm	4mm	330mm (13")	1,000
SW	SO (0.300)	20	24mm	12mm	4mm	330mm (13")	1,000
SW	SO (0.300)	24	24mm	12mm	4mm	330mm (13")	1,000
SW	SO (0.300)	28	24mm	12mm	4mm	330mm (13")	1,000
S3*	SOT-23	3	8mm	4mm	4mm	180mm (7")	2,500*
S5*	SOT-23, TSOT	5	8mm	4mm	4mm	180mm (7")	2,500*
S6*	SOT-23, TSOT	6	8mm	4mm	4mm	180mm (7")	2,500*
SC6*	SC70	6	8mm	4mm	4mm	180mm (7")	2,500*
SC8*	SC70	8	8mm	4mm	4mm	180mm (7")	2,500*
TS8*	TSOT	8	8mm	4mm	4mm	180mm (7")	2,500*
UDB*	QFN (3mm × 2mm)	10, 12	8mm	4mm	4mm	180mm (7")	2,500*
UD	QFN (3mm × 3mm)	16, 20	12mm	8mm	4mm	330mm (13")	2,500
UDC	QFN (3mm × 4mm)	18, 20, 24	12mm	8mm	4mm	330mm (13")	2,500
UDD	QFN (3mm × 5mm)	24	12mm	8mm	4mm	330mm (13")	2,500
UDE	QFN (3mm × 6mm)	28	16mm	8mm	4mm	330mm (13")	2,500
UF	QFN (4mm × 4mm)	16, 20, 24, 28	12mm	8mm	4mm	330mm (13")	2,500
UFD	QFN (4mm × 5mm)	20, 24, 28	12mm	8mm	4mm	330mm (13")	2,500
UFE	QFN (4mm × 6mm)	26, 32, 38	16mm	8mm	4mm	330mm (13")	2,500
UFF	QFN (4mm × 7mm)	34, 36, 44	16mm	8mm	4mm	330mm (13")	2,500
UH	QFN (5mm × 5mm)	20, 24, 32, 40	12mm	8mm	4mm	330mm (13")	2,500
UHE	QFN (5mm × 6mm)	28, 36, 42	16mm	8mm	4mm	330mm (13")	2,500
UHF	QFN (5mm × 7mm)	38	16mm	8mm	4mm	330mm (13")	2,500
UHG	QFN (5mm × 8mm)	39, 40, 52	16mm	8mm	4mm	330mm (13")	2,500
UHH	QFN (5mm × 9mm)	48, 56, 58	16mm	8mm	4mm	330mm (13")	2,500
UJ	QFN (6mm × 6mm)	40	16mm	12mm	4mm	330mm (13")	2,000
UK	QFN (7mm × 7mm)	44, 48	16mm	12mm	4mm	330mm (13")	2,000
UKG	QFN (7mm × 8mm)	47, 52	16mm	12mm	4mm	330mm (13")	2,000
UKH	QFN (7mm × 9mm)	64	16mm	12mm	4mm	330mm (13")	2,000
UKJ	QFN (7mm × 11mm)	64	24mm	12mm	4mm	330mm (13")	2,000
UKK	QFN (7mm × 12mm)	68	24mm	12mm	4mm	330mm (13")	2,000
UP	QFN (9mm × 9mm)	64	16mm	12mm	4mm	330mm (13")	2,000
WKG	QFN (7mm × 8mm)	52	16mm	12mm	4mm	330mm (13")	2,000
WP	QFN (9mm × 9mm)	64	16mm	12mm	4mm	330mm (13")	2,000

**TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT**

**Bending Radius**



**Embossed Carrier Dimensions (8mm, 12mm, 16mm, 24mm Tape Only)**



**Embossed Tape—Constant Dimensions**

Tape Width	$D_0$	$E_1$	$P_0$	$P_2$	T Max	$T_1$ Max	$A_0 B_0 k_0$
8mm	1.5	+0.10	$4.0 \pm 0.10$	$2.0 \pm 0.05$	0.600	0.10	See Note 1
12mm		-0.0	$(0.069 \pm 0.004)$	$(0.079 \pm 0.002)$	(0.024)	(0.004)	
16mm	(0.059)	+0.004					
24mm		-0.0					

**Embossed Tape Variable Dimensions**

Tape Width	$B_1$ Max	$D_1$ Min	F	$T_2$ Max	R Min	W Max
8mm	4.35 (0.171)	1.0 (0.039)	$3.5 \pm 0.05$	2.5 (0.098)	25 0.984	8.3
12mm (0.323)	8.2 (0.059)	1.5 (0.217 ± 0.002)	$5.5 \pm 0.05$ (0.256)	6.5 (0.256)	30 (1.181)	12.3
16mm	12.1 (0.476)	1.5 (0.217 ± 0.002)	$7.5 \pm 0.10$ (0.295 ± 0.004)	8.0 (0.315)	40 (1.575)	16.3
24mm	20.1 (0.791)	1.5 (0.217 ± 0.002)	$11.5 \pm 0.10$ (0.453 ± 0.004)	12.0 (0.472)	50 (1.969)	24.3

**Note 1:** The cavity defined by  $A_0$ ,  $B_0$  and  $K_0$  shall surround the component with sufficient clearance that:

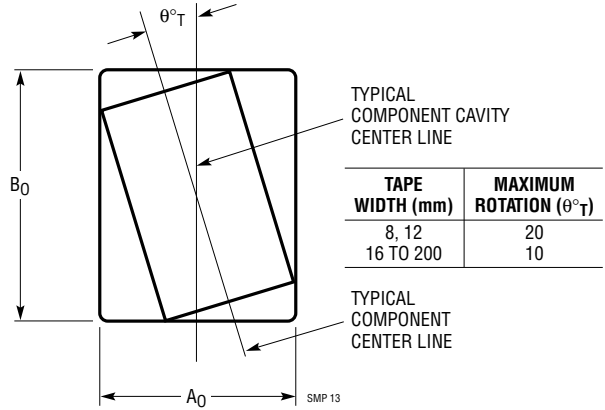
- a) the component does not protrude above the top surface of the carrier tape.
- b) the component can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed.

- c) rotation of the component is limited to 20° maximum for 8mm and 12mm tapes and 10° maximum for 16mm and 24mm tapes.
- d) lateral movement of the component is restricted to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16mm and 24mm wide tape.

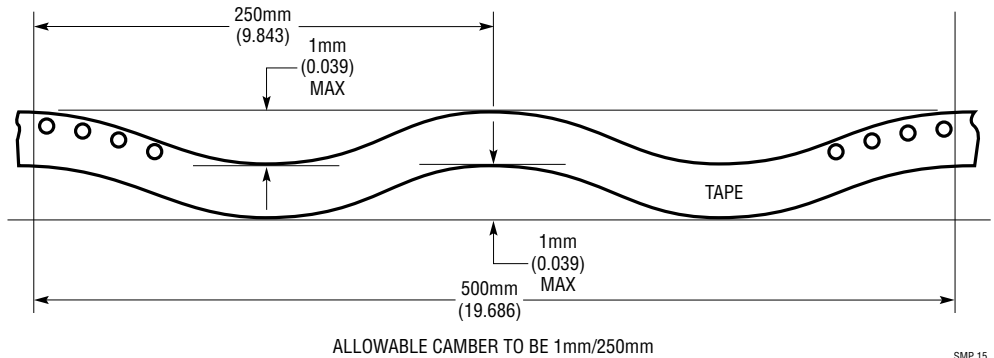
**Note 2:** The tape with or without components shall pass around R without damage.

**TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT**

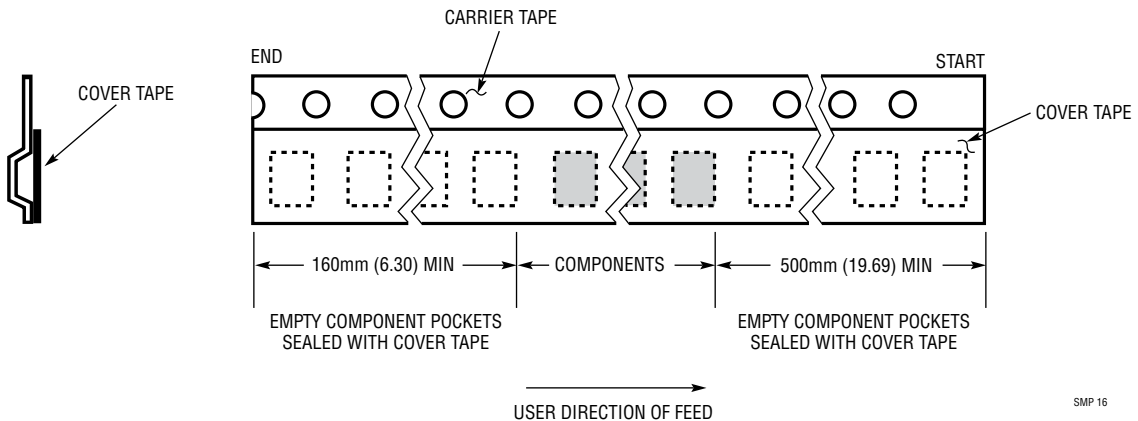
**Component Rotation**



**Tape Camber (Top View)**

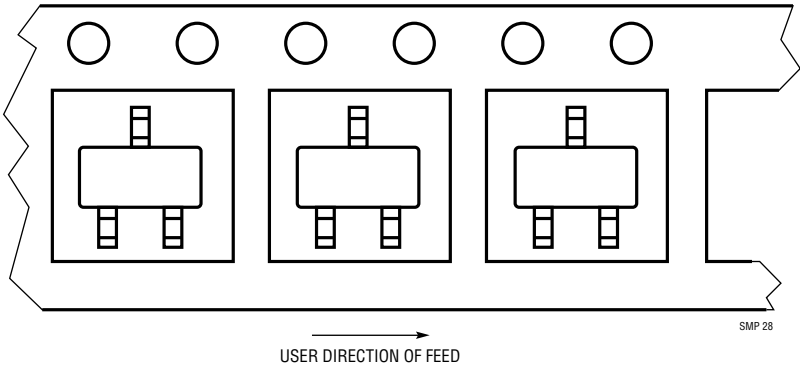


**Tape Leader (Start/End) Specification**

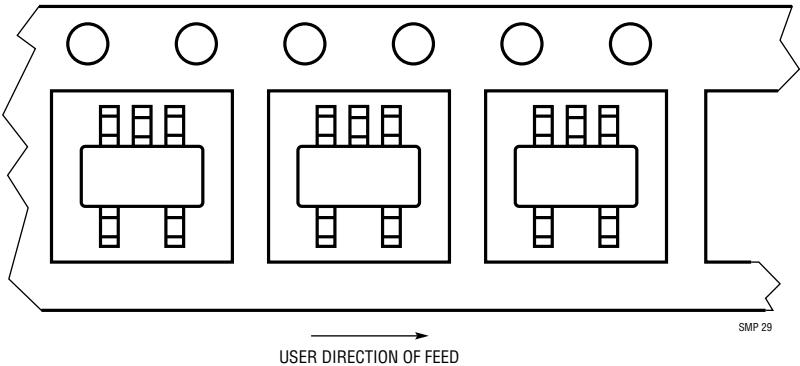


**TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT**

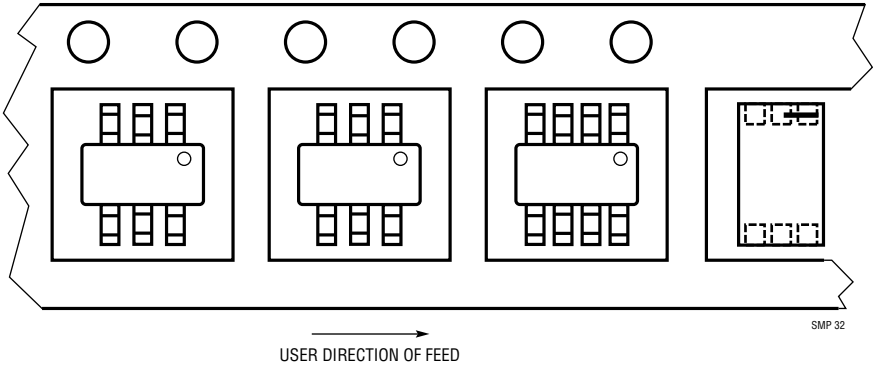
**S3**  
**SOT-23 Devices**



**S5**  
**TSOT, SOT-23 Devices**

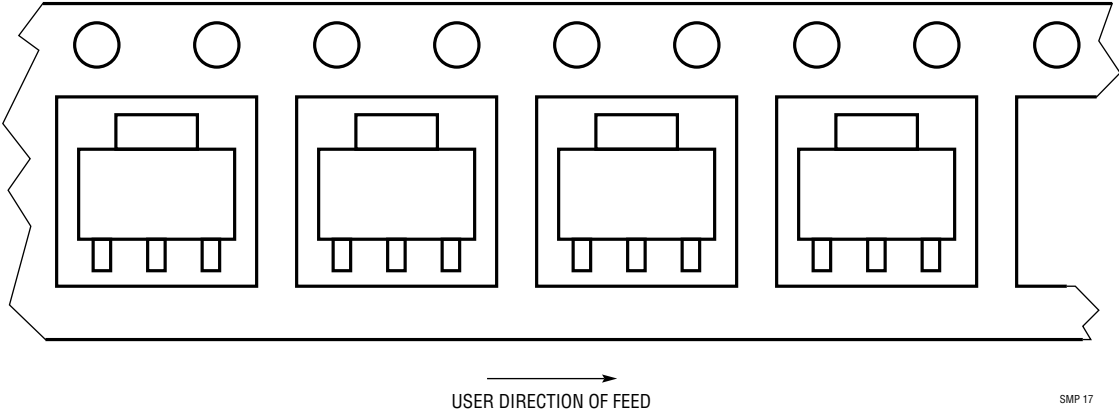


**SC6, S6 and TS8**  
**SC70, TSOT, SOT-23, DFN (DCB) Devices**



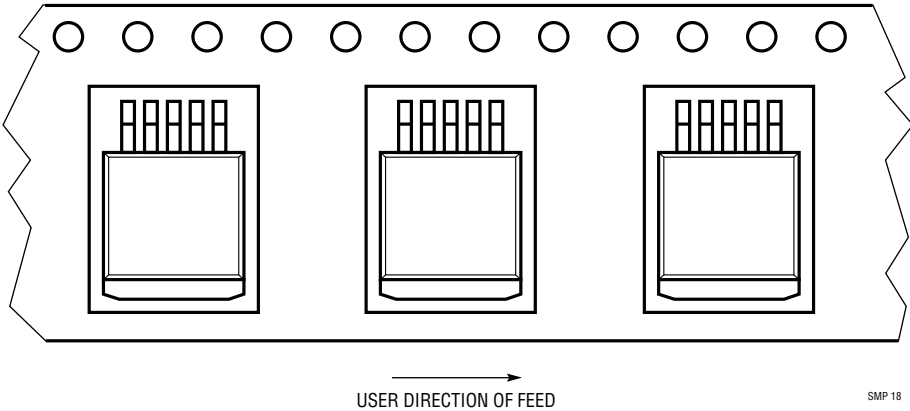
**TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT**

**ST  
SOT-223 Devices**



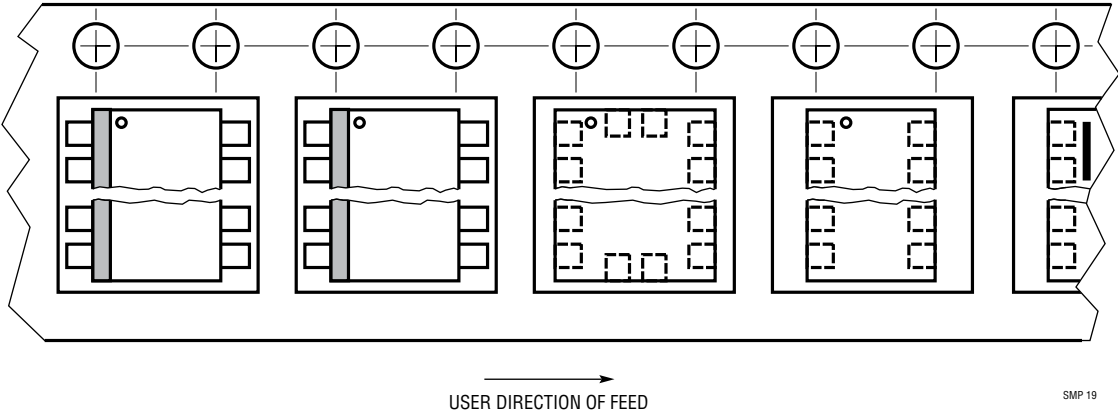
SMP 17

**M, Q, R  
DD Pak Devices**



SMP 18

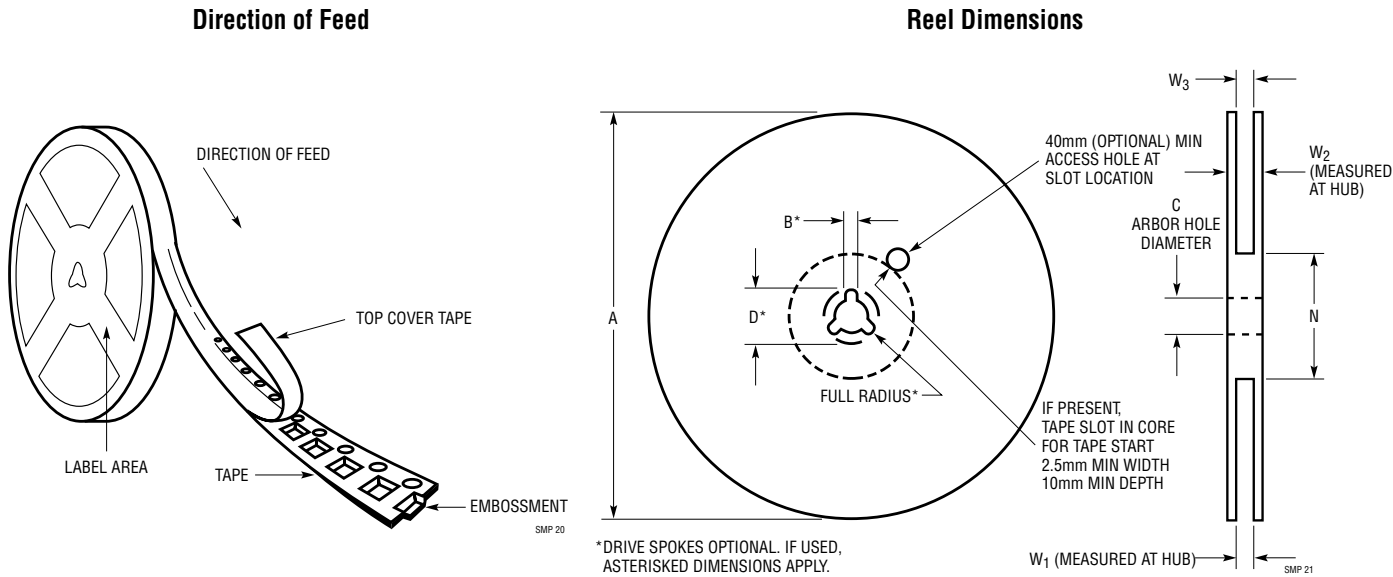
**F, FE, FW, G, GN, GW, S8, S, SW, MS8, MS, MS8E, MSE,  
SSOP, TSSOP, QFN, DFN, UTDFN and UTQFN Devices [except DFN (DCB)]**



SMP 19



**REEL DIMENSIONS—SURFACE MOUNT**



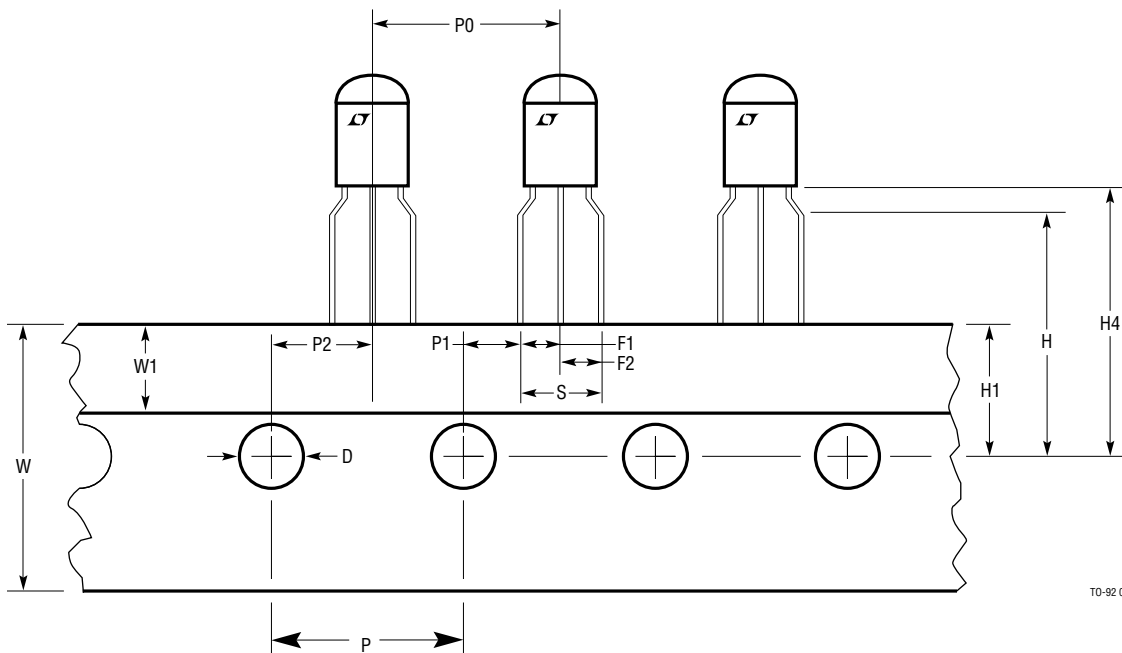
Tape Width	A Max	B Min	C	D* Min	N Min	W <sub>1</sub>	W <sub>2</sub> Max	W <sub>3</sub>
8mm	180	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	60	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4	Shall Accommodate Tape Width Without Interference
	330	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4	
12mm	180	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	60	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4	
	330	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4	
16mm	330	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	50	16.4 <sup>+2.0</sup> <sub>-0.00</sub>	22.4	
24mm	330	1.5	13.0 <sup>+0.5</sup> <sub>-0.2</sub>	20.2	60	24.4 <sup>+2.0</sup> <sub>-0.00</sub>	30.4	

**Note 1:** All dimensions in millimeters.

**Note 2:** See Table 1 for tape width and reel diameter of specific packages.

## TAPE AND REEL SPECIFICATIONS—TO-92

TO-92 Tape Dimension

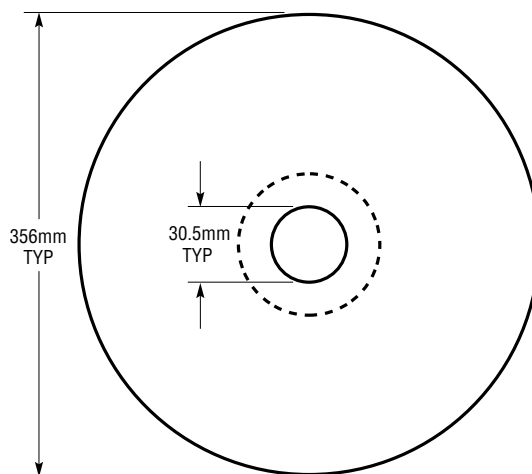


TO-92 01

TO-92 Reel Dimensions

Table 1

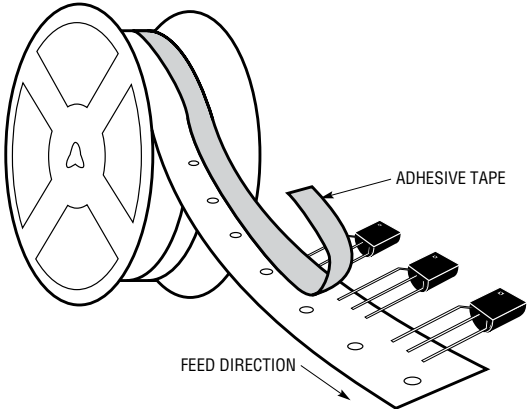
Symbol	Description	Dimension (mm)
D	Sprocket Hole Diameter	$4 \pm 0.2$
H	Length from Seating Plane	$16 \pm 0.5$
H1	Sprocket Hole Location	$9 \pm 0.5$
H4	Component Base Height	20 Max
P	Sprocket Hole Pitch	$12.7 \pm 0.2$
P0	Pitch of Component	$12.7 \pm 0.5$
P1	Lead Location	$3.85 \pm 0.5$
P2	Center of Seating Plane Location	$6.35 \pm 0.4$
S	Component Lead Spacing	$5 +0.8/-0.2$
W	Carrier Tape Width	$18 +1, -0.5$
W1	Adhesive Tape Width	$6.0 \pm 1.0$
F1, F2	Lead-to-Lead Distance	$2.5 +0.4, -0.1$



TO-92 02

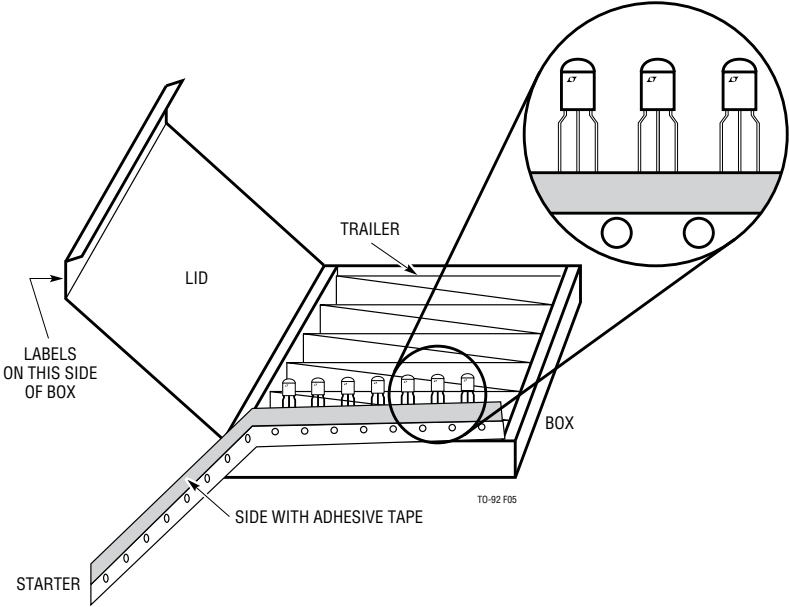
**TAPE AND REEL SPECIFICATIONS—TO-92**

**Reel Pak Tape Orientation on Reel**



TO-92 03

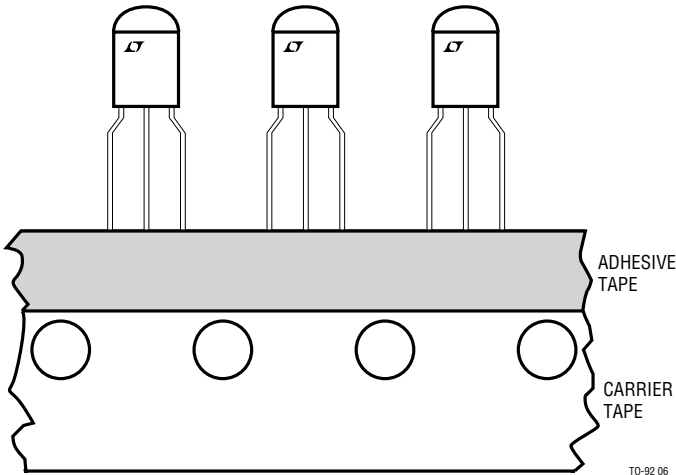
**Ammo Pak Tape Orientation Inside Box**



TO-92 F05

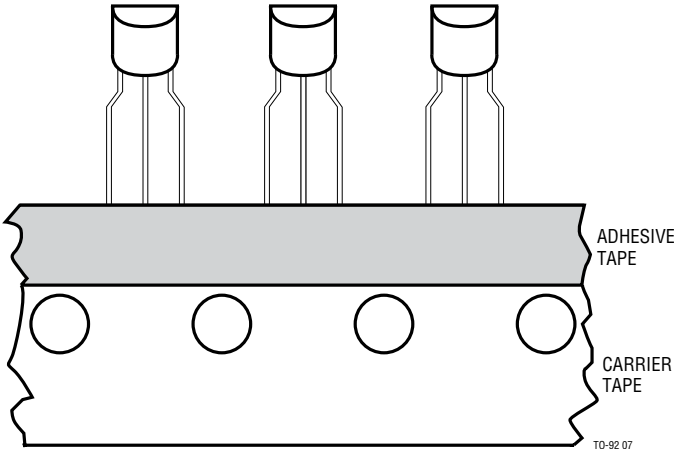
**Package Orientation on Tape**

**STYLE E: Standard Flow TR**  
(Flat Side of Package Faces Toward the Adhesive Tape)



TO-92 06

**STYLE A: Special Flow TRA**  
(Rounded Side of Package Faces Toward the Adhesive Tape)



TO-92 07