Setup description

We are interfacing the PGA970 as an SPI slave with an STM32H5 as the SPI master. SPI timing and communication have been verified and are functioning correctly.

During SPI reads, we consistently receive 0x05 (RVALID), indicating that the read transactions are valid.

Issue:

We are not able to generate the waveform, despite following the configuration and programming steps outlined in the datasheet.

For your reference, we've attached

1. Register write sequence and values
2. The schematic
3. Bypass capacitor values for AVDD, DVDD, REFCAP, and LVDT_PWR.
4. Measured voltage levels for AVDD, DVDD, REFCAP, and LVDT_PWR

Steps Followed:

Description	Register	DI Page	DI Offset	Value written
Reset the Microprocessor and Enable the Digital Interface	MICRO_INTERFACE_CONTROL	0x0	0x0C	0x03
Turn On the Accurate Reference Buffer (REFCAP Voltage)	ALPWR	0x2	0x50	0x14
Clear OSC_BAD bit	PSMON2		0x59	0x10
Turn off the waveform DAC	WAVEFORM_GEN_CTRL		0x78	0x00
Write 0x08 to DATA_WAVE_PAGE_ADDR	DATA_WAVE_PAGE_ADDR		0x19	0x08
Load the waveform RAM with quarter-waveform values Formula: amp × sin(2πfreq × (0.5 µs + n1 µs))	WAVEFORM_RAM	0x1	-	Waveform Table
Program N – 1, where N is quarter-waveform table length	WAVEFORM_TABLE_LEN	0x2	0x7A	0x31
Set waveform DAC offset round(DCValue / 1.25 × 16 384)	WAVEFORM_DAC_OFFSET		0x7C, 0x7D	0x2C08
1. Configure wave gain by writing to GAIN_CTRL 2. Configure differential/single ended waveform(SEM) 3. Configure differential common mode voltage by writing to DIFF_VOCM_CTRL 4. Internal or external connection between PE & PI (SKIP FILTER)	LVDT_OP_CTRL		0x3C	0x72
Connect the waveform DAC to WAVE GAIN	AMUX_CTRL		0x67	0xF1
Disable loopback	LVDT_LPBK_CTRL		0x3D	0x00
Enable the waveform DAC	WAVEFORM_GEN_CTRL		0x78	0x01
De assert MICRO_RESET bit	MICRO_INTERFACE_CONTROL	0x0	0x0C	0x00

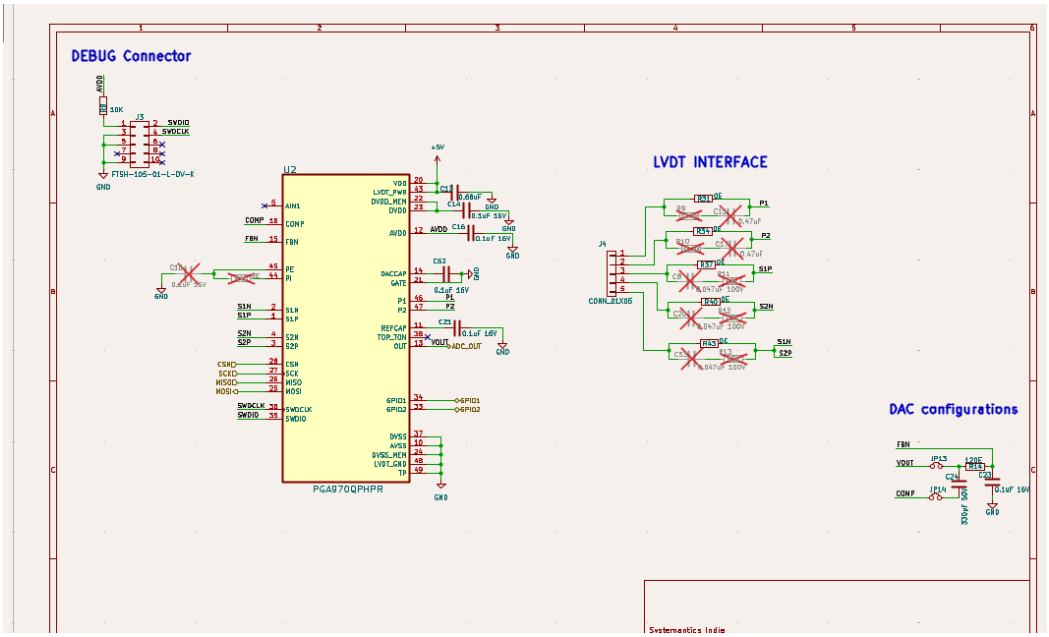
NOTE: After enabling the waveform generator, **WAVE_STATUS bit is 1** when we read WAVEFORM_GEN_CTRL (Waveform generator is enabled and running).

Waveform Table

Value obtained from **pga970_waveform.c** provided by TI
Firmware: **PGA970_FW_Release_1_6_Generic**

```
/*5KHz. For 5KHz, 50 samples are needed. Program 50-1=49 in the register*/
    Waveform_Table_size = 0x31;
    waveformTable[0] = 0x43;
    waveformTable[1] = 0xC9;
    waveformTable[2] = 0x14E;
    waveformTable[3] = 0x1D3;
    waveformTable[4] = 0x258;
    waveformTable[5] = 0x2DC;
    waveformTable[6] = 0x360;
    waveformTable[7] = 0x3E2;
    waveformTable[8] = 0x464;
    waveformTable[9] = 0x4E5;
    waveformTable[10] = 0x564;
    waveformTable[11] = 0x5E2;
    waveformTable[12] = 0x65E;
    waveformTable[13] = 0x6D9;
    waveformTable[14] = 0x752;
    waveformTable[15] = 0x7C9;
    waveformTable[16] = 0x83F;
    waveformTable[17] = 0x8B2;
    waveformTable[18] = 0x923;
    waveformTable[19] = 0x991;
    waveformTable[20] = 0x9FE;
    waveformTable[21] = 0xA67;
    waveformTable[22] = 0xACF;
    waveformTable[23] = 0xB33;
    waveformTable[24] = 0xB94;
    waveformTable[25] = 0xBF3;
    waveformTable[26] = 0xC4F;
    waveformTable[27] = 0xCA7;
    waveformTable[28] = 0xCFD;
    waveformTable[29] = 0xD4F;
    waveformTable[30] = 0xD9D;
    waveformTable[31] = 0xDE8;
    waveformTable[32] = 0xE30;
    waveformTable[33] = 0xE74;
    waveformTable[34] = 0xEB5;
    waveformTable[35] = 0xEF1;
    waveformTable[36] = 0xF2A;
    waveformTable[37] = 0xF60;
    waveformTable[38] = 0xF91;
    waveformTable[39] = 0xFBE;
    waveformTable[40] = 0xFE8;
    waveformTable[41] = 0x100D;
    waveformTable[42] = 0x102E;
    waveformTable[43] = 0x104B;
    waveformTable[44] = 0x1064;
    waveformTable[45] = 0x1079;
    waveformTable[46] = 0x108A;
    waveformTable[47] = 0x1097;
    waveformTable[48] = 0x109F;
    waveformTable[49] = 0x10A3;
```

Schematic:



Regulator Outputs:

Net	Bypass Cap value	As per datasheet recommendation?	Measured Voltage (V)
DVDD	100 nF 16 VDC	☑	1.91
AVDD	100 nF 16 VDC	☑	2.98
REFCAP	100 nF 16 VDC	☑	2.51
LVDT_PWR	680 nF 10 VDC	☑	5.01
DACCAP	100 nF 16 VDC	☑	0 (DACCAP disabled)