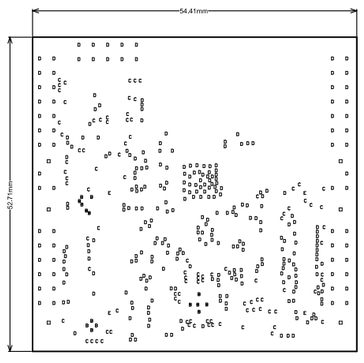
Drill Table: Top Layer to Bottom Layer

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair
B	15	7.87mil (0.200mm)	PTH	Round	-	-	Top Layer - Bottom Layer
C	96	10.00mil (0.254mm)	PTH	Round	-	-	Top Layer - Bottom Layer
D	331	12.20mil (0.310mm)	PTH	Round	-	-	Top Layer - Bottom Layer
E	4	40.16mil (1.020mm)	NPTH	Round	-	-	Top Layer - Bottom Layer
□	6	118.11mil (3.000mm)	PTH	Round	-	-	Top Layer - Bottom Layer
	452 Total						

FOR PTH +/- 3MIL
FOR NPTH +/- 2MIL
FOR 7.874MIL DRILL +0/-7.874MIL
FOR 10MIL DRILL +0/-10MIL
FOR 12.2MIL DRILL +0/-12.2MIL

Drill Table: Layer 1 To Layer 2

FOR 5.9MIL DRILL +0/-5.9MIL



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.80mil	1	
3	Top Layer	Copper	0.80mil		
4	Dielectric 1	R03003	5.00mil	3	
5	L2	Copper	1.20mil		
6	Dielectric 2	1080 X2 370HR	5.30mil	3.9	
7	L3	Copper	1.20mil		
8	Dielectric 3	4-7628 370HR	28.00mil	4.36	
9	L4	Copper	1.20mil		
10	Dielectric 4	1080 X2 370HR	5.26mil	3.9	
11	L5	Copper	1.20mil		
12	Dielectric 5	1-1652 370HR	5.00mil	4.34	
13	Bottom Layer	Copper	0.80mil		
14	Bottom Solder	Solder Resist	0.80mil	1	
15	Bottom Overlay				

NOTES:

1. THIS IS AN IMPEDANCE CONTROL BOARD
2. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
3. ALL VIAS ON PAD INCLUDING BGA AREA SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT
   BGA AREA VIAS SHOULD BE CAPPED WITH COPPER PLATING TO ENSURE FLAT SURFACE
   FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES.
   OTHER THAN BGA AND VIA'S ON THE PAD VIA FILLING REQUIREMENT CAN BE EXEMPTED
4. SOLDER MASK OPENING IS KEPT SAME SIZE AS PAD (1:1)
   THE MANUFACTURER IS REQUESTED TO RESIZE IT AS PER THEIR SOLDERMASK TOLERANCE EXCEPT NPTH DRILL AND FIDUCIALS.
5. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
6. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE
   OF THE BOARD.
7. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
8. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL
9. REFER STACKUP DOCUMENT FOR IMPEDANCE CONTROL TRACES ON LAYER 1 AND LAYER 6.
   100HM DIFFERENTIAL IMPEDANCE CONTROL TRACES.
10. LAYER 1 IMPEDANCE CONTROL TRACES:
    11.A. CPW: 11.625 WIDTH/ 9MIL GAP – 50 ohms (60GHz)
    11.B. MICROSTRIP: 12 MIL– 50 ohms (60GHz)
    11.C. DIFFERENTIAL: 6.25 MIL WIDTH/ 3.95MIL GAP– 100 ohms
11. FOR ACCURACY OF THE ANTENNA DIMENSION, NEED TO BE MEASURE THE ANTENNA DIMENSIONS ON ONE BAORD AS PER ANTENNA DOCUMENT(IWR 60Ghz).
12. INTENTIONAL ONE NET ANTENNA VIA IS PRESENT IN DESIGN

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 3 MIL
MIN. VIA PAD SIZE: 13.77 MIL
MINIMUM ANNULAR RING 0.099mm (3.9MIL)EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 58.2 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG
☒ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

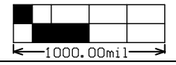
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 1 & 6 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

AINSTEIN TEXAS INSTRUMENTS

PROJECT TITLE: IWR6843ISK (INDUSTRIAL STARTER KIT)
DESIGNED FOR: Public Release
FILE NAME: PROC075A.PcbDoc



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC075	REV: A	SVN REV: Not In VersionControl
LAYER NAME = Mfr Board Outline	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 1/10/2019 3:59:37 PM		TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Faiz Ahmed	TESSOLVE
SCALE: 1.00	ALTIUM DESIGNER VERSION: 18.1.9.240