Title: AWR2243: ADC Data Format from MMWCAS-RF-EVM to CSI2

We are considering an FPGA design to evaluate signal processing using the radar output of the MMWCAS-RF-EVM.

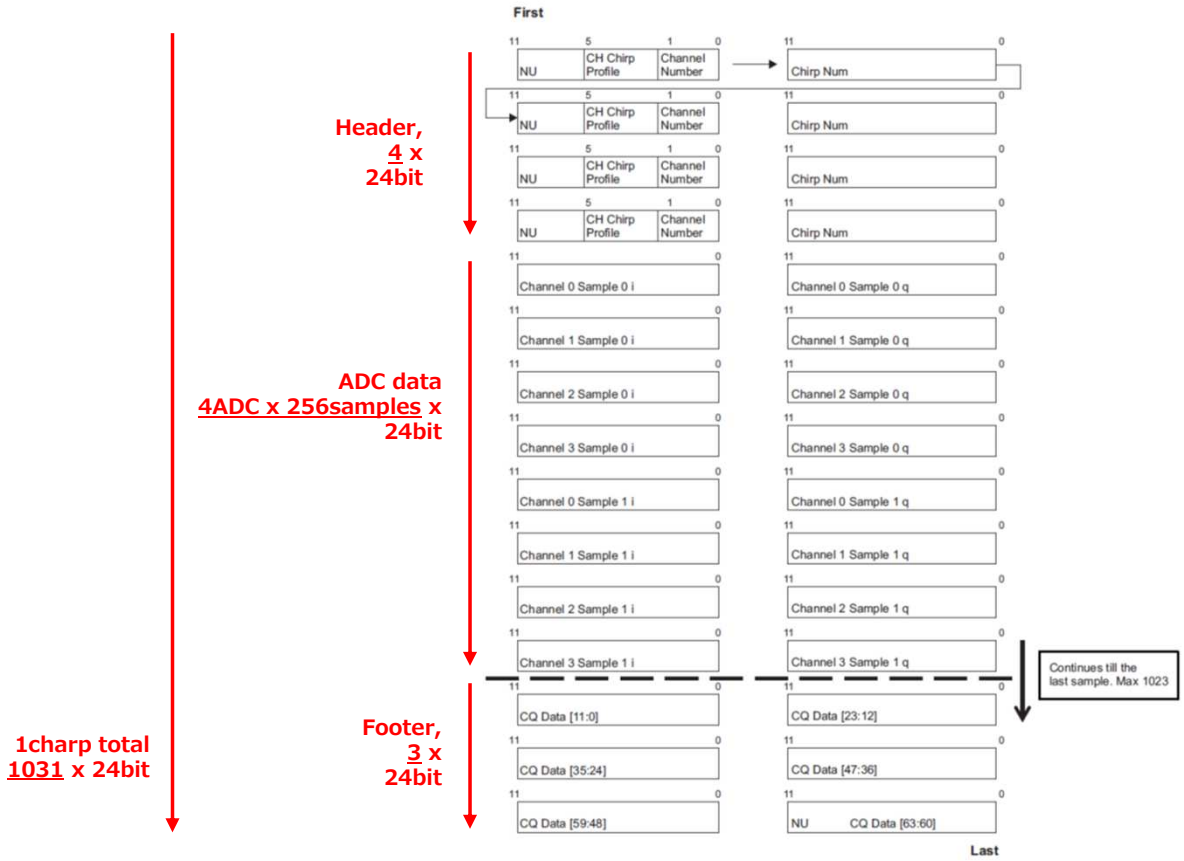
Below is a Lua script for mmWaveSDK. We use this configuration for MMWCAS-RF-EVM.

ti¥mmwave_studio_03_00_00_14¥mmWaveStudio¥Scripts¥Cascade¥Cascade_Configuration_MIMO.lua
adc_samples=256（256 samples)
metaImagePath =
C:¥¥ti¥¥mmwave_dfp_02_02_04_00¥¥firmware¥¥xwr22xx_metaImage.bin"

ti¥mmwave_studio_03_00_00_14¥mmWaveStudio¥Scripts¥Cascade¥Cascade_Capture.lua
data_packaging=1（raw 12bit mode)

We have the following question regarding the output from EVM to CSI2.

- Question
Figure 8-5, taken from the AWR2243 datasheet, is shown at right. From this figure, we assume that the size of the 1-chirp ADC that EVM outputs to CSI2 is 1031 x 12 bits, is this correct?
We checked the ADC data size with sample settings of 256 and 512, but the HostCPU connected via MIPI always outputs 2048 x 24 bits. Are there any possible reasons why this might happen?



https://www.ti.com/document-viewer/awr2243/datasheet
Figure 8-5. Data Packet Packing Format for 12-Bit Complex Configuration