

ADS131M04 4-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC

TI Information — Selective Disclosure

1 Features

- 4 Simultaneously-Sampling Differential Inputs
- Programmable Data Rate up to 32 kSPS
- Programmable Gain up to 128
- Noise Performance:
 - 100-dB Dynamic Range at Gain = 1, 4 kSPS
 - 81-dB Dynamic Range at Gain = 64, 4 kSPS
- Total Harmonic Distortion: –100 dB
- High-Impedance Inputs for Direct Sensor Connection
 - >100-k Ω Input Impedance for Gain = 1, 2, and 4
 - >1-M Ω Input Impedance for Gain = 8, 16, 32, and 64
- Programmable Channel-to-Channel Phase Delay Calibration With 244-ns Resolution at 4 kSPS
- Fast Startup: First Data Within 0.5 ms of Supply Ramp
- Integrated Negative Charge Pump Allows Input Signals Below Ground
- Crosstalk Between Channels: –110 dB
- Low-Drift Internal Voltage Reference
- Cyclic Redundancy Check (CRC) on Communications and Register Map
- 2.7-V – 3.6-V Analog and Digital Supplies
- Low Power Consumption: 3.3 mW at 3-V AVDD and DVDD
- Package: 20-Pin TSSOP or 20-Pin WQFN
- Operating Temperature Range: –40°C to +125°C

2 Applications

- Electricity Meter: Commercial and Residential
- Circuit Breaker
- Power Monitor
- Protection Relay
- Battery Test
- Battery Management System

3 Description

The ADS131M04 is a four-channel, simultaneously-sampling, 24-bit, delta-sigma ($\Delta\Sigma$), analog-to-digital converter (ADC) that offers wide dynamic range, and internal calibration features making it excellent for energy metering, power quality, protection relay and circuit breaker applications. The ADC inputs can be directly interfaced to a resistor-divider network, a transformer to measure voltage or current, or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low level signals. Additionally, this device integrates channel to channel phase calibration and offset and gain calibration registers to help remove signal chain errors.

A low-drift, 1.2-V reference is integrated into the device reducing printed circuit board (PCB) area. Cyclic redundancy check (CRC) options can be individually enabled on the data input, data output and register map to ensure communication integrity.

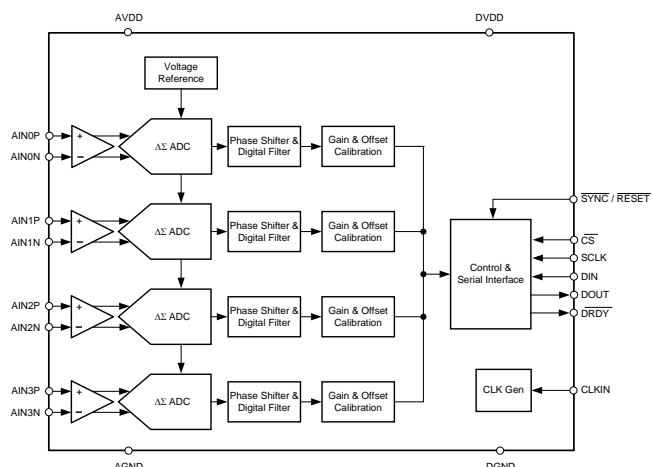
The complete analog front-end (AFE) solution is offered in a TSSOP-20 or leadless WQFN-20 package and are specified over the industrial temperature range of –40°C to +125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS131M04	TSSOP (20)	6.50 mm x 4.40 mm
	WQFN (20)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Table of Contents**

1 Features	1	7.2 Functional Block Diagram	8
2 Applications	1	7.3 Feature Description	9
3 Description	1	7.4 Device Functional Modes	18
4 Revision History	2	7.5 Programming	22
5 Pin Configuration and Functions	3	7.6 Registers	29
6 Specifications	4	8 Device and Documentation Support	50
6.1 Absolute Maximum Ratings	4	8.1 Receiving Notification of Documentation Updates ..	50
6.2 ESD Ratings	4	8.2 Community Resources	50
6.3 Recommended Operating Conditions	5	8.3 Trademarks	50
6.4 Thermal Information	5	8.4 Electrostatic Discharge Caution	50
6.5 Electrical Characteristics	6	8.5 Glossary	50
7 Detailed Description	8	9 Mechanical, Packaging, and Orderable Information	50
7.1 Overview	8	9.1 Package Option Addendum	51

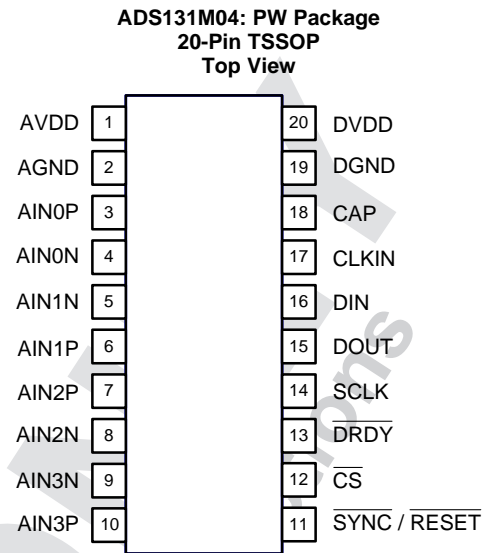
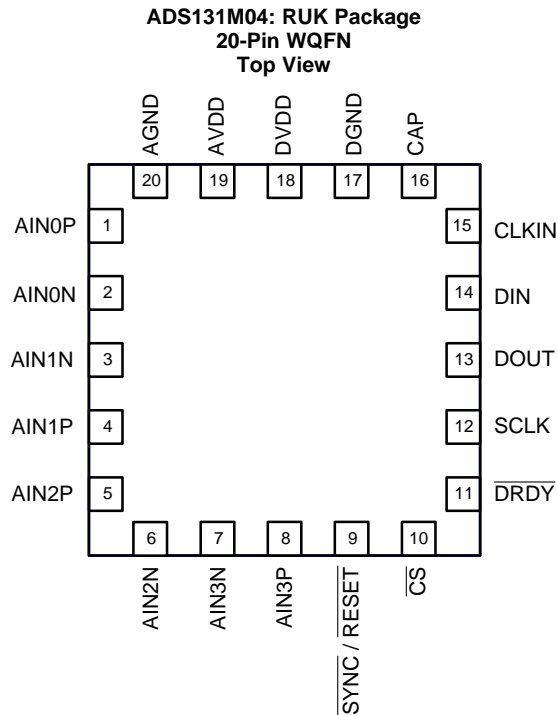
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2018	*	Initial release.

PRODUCT PREVIEW

5 Pin Configuration and Functions



Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	QFN-20	TSSOP-20		
AIN0N	2	4	Analog input	Negative analog input 1
AIN0P	1	3	Analog input	Positive analog input 1
AIN1N	3	5	Analog input	Negative analog input 2
AIN1P	4	6	Analog input	Positive analog input 2
AIN2P	5	7	Analog input	Positive analog input 3
AIN2N	6	8	Analog input	Negative analog input 3
AIN3P	8	10	Analog input	Positive analog input 4
AIN3N	7	9	Analog input	Negative analog input 4
AVDD	19	1	Supply	Analog supply. Connect a 1-μF capacitor to AGND.
AGND	20	2	Supply	Analog ground
\overline{CS}	10	12	Digital input	Chip select; active low
DGND	17	v19	Supply	Digital ground
DVDD	18	20	Supply	Digital I/O supply. Connect a 1-μF capacitor to DGND.
DIN	14	16	Digital input	Serial data input
DOUT	13	15	Digital output	Serial data output
\overline{DRDY}	11	13	Digital output	Data ready; active low
$\overline{SYNC} / \overline{RESET}$	9	11	Digital input	Conversion synchronization or system reset; active low
SCLK	12	14	Digital input	Serial data clock
CLKIN	15	17	Digital input	Master clock input
CAP	16	18	Analog output	Digital low-dropout (LDO) regulator output. Connect a 100-nF capacitor to DGND.

PRODUCT PREVIEW

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**6 Specifications****6.1 Absolute Maximum Ratings⁽¹⁾**

		MIN	MAX	UNIT
Power supply voltage	AVDD to AGND	–0.3	3.9	V
	AGND to DGND	–0.3	0.3	
	DVDD to DGND	–0.3	3.9	
Analog input voltage	AINxP, AINxN	AGND – 2.0	AVDD + 0.3	V
Digital input voltage	\overline{CS} , CLKIN, DIN, SCLK, $\overline{SYNC/RESET}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except supply pins	–10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	–60	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
Analog supply voltage	AVDD to AGND	2.7	3.0	3.6	V	
	AGND to DGND	−0.3	0	0.3	V	
Digital supply voltage	DVDD to DGND	2.7	3.0	3.6	V	
	DVDD to DGND, DVDD shorted to CAP	1.65	1.8	2	V	
ANALOG INPUTS						
V _{IN}	Differential input voltage	V _{IN} = V _{AINxP} − V _{AINxN}	−V _{REF} / Gain	V _{REF} / Gain	V	
V _{AINxP} , V _{AINxN} ⁽¹⁾	Absolute input voltage		AGND − 1.3	AVDD	V	
EXTERNAL CLOCK SOURCE						
f _{CLKIN}	External clock input frequency	High-resolution mode	1	8.192	8.3	MHz
		Low-power mode	1	4.096	4.15	
		Very low-power mode	0.2	2.048	2.08	
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Digital input voltage		DGND	DVDD	V	
TEMPERATURE						
T _A	Operating ambient temperature		−40		125	°C

- (1) The subscript "x" signifies the channel. For example, the positive analog input to channel 0 is named AIN0P. Refer to the section for the pin names.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS131M04		UNIT
		TBD (QFN)	TBD (TSSOP)	
		PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

6.5 Electrical Characteristics

Minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$. Typical specifications are at $T_A = 25^{\circ}\text{C}$. All specifications are at $AVDD = 3\text{ V}$, $DVDD = 3\text{ V}$, $f_{\text{CLKIN}} = 8.192\text{ MHz}$, high-resolution mode, data rate = 4 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
Z _{in}	Differential input impedance	Gain = 1, 2, or 4		240		kΩ
		Gain = 8, 16, 32, or 64		1		MΩ
		All other power modes		See TBD section		
ADC CHARACTERISTICS						
	Resolution			24		Bits
	Gain			1, 2, 4, 8, 16, 32, 64, 128		
	Data rate	High-resolution mode, f _{MOD} = 4.096 MHz	250		32000	SPS
		Low-power mode, f _{MOD} = 2.048 MHz	125		16000	
		Very low-power mode, f _{MOD} = 1.024 MHz	62.5		8000	
	Startup time	Measured from supplies at 90% to first $\overline{\text{DRDY}}$ signal		0.5		ms
DC PERFORMANCE						
INL	Integral nonlinearity	Best fit		5		ppm of FSR
V _{IO}	Input offset voltage			TBD		μV
	Offset drift			TBD		μV/°C
	Gain error	Including internal reference error		±0.2		%
	Gain drift	Including internal reference error		TBD		ppm/°C
DC CMRR	DC common-mode rejection ratio			90		dB
DC PSRR	DC power-supply rejection ratio	AVDD		TBD		dB
		DVDD		TBD		
AC PERFORMANCE						
	Dynamic range	Gain = 1	96	100		dB
		Gain = 64		81		
		All other settings		See TBD section		
	Crosstalk	f _{IN} = 50 Hz or 60 Hz		−110		dB
SNR	Signal-to-noise ratio	f _{IN} = 50 Hz or 60 Hz, Gain = 1, V _{IN} = −20 dBFS, normalized		101		dB
		f _{IN} = 50 Hz or 60 Hz, Gain = 64, V _{IN} = −20 dBFS, normalized		80		
THD	Total harmonic distortion	f _{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V _{IN} = −0.5 dBFS		−100		dB
SFDR	Spurious-free dynamic range	f _{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V _{IN} = −0.5 dBFS		100		dB
AC CMRR	AC common-mode rejection ratio	f _{CM} = 50 Hz or 60 Hz		90		dB
AC PSRR	AC power-supply rejection ratio	AVDD supply, f _{PS} = 50 Hz or 60 Hz		75		dB
		DVDD supply, f _{PS} = 50 Hz or 60 Hz		TBD		

Electrical Characteristics (continued)

Minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$. Typical specifications are at $T_A = 25^{\circ}\text{C}$. All specifications are at $AVDD = 3\text{ V}$, $DVDD = 3\text{ V}$, $f_{CLKIN} = 8.192\text{ MHz}$, high-resolution mode, data rate = 4 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE VOLTAGE						
V_{REF}	Reference voltage			1.2		V
	Accuracy			TBD		%
	Temperature drift			TBD		ppm/ $^{\circ}\text{C}$
DIGITAL INPUT/OUTPUT						
V_{IL}	Logic input level, low		DGND		0.2 DVDD	V
V_{IH}	Logic input level, high		0.8 DVDD		DVDD	V
V_{OL}	Logic output level, low	$I_{OL} = -1\text{ mA}$			0.2 DVDD	V
V_{OH}	Logic output level, high	$I_{OH} = 1\text{ mA}$		0.8 DVDD		V
I_{IN}	Input current	$0\text{ V} < V_{\text{Digital Input}} < DVDD$	-10		10	μA
POWER-SUPPLY						
I_{AVDD}	AVDD current	High-resolution mode		3.1	TBD	mA
		Low-power mode		1.6	TBD	
		Very low-power mode		0.9	TBD	
		Standby mode		1		μA
		All other gain settings		See TBD section		
I_{DVDD}	DVDD current	High-resolution mode		0.5	TBD	mA
		Low-power mode		0.3	TBD	
		Very low-power mode		0.2	TBD	
		Standby mode, CLKIN idle		TBD		μA
P_D	Power dissipation	High-resolution mode		11		mW
		Low-power mode		5.9		
		Very low-power mode		3.3		
		Standby mode		TBD		μW

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

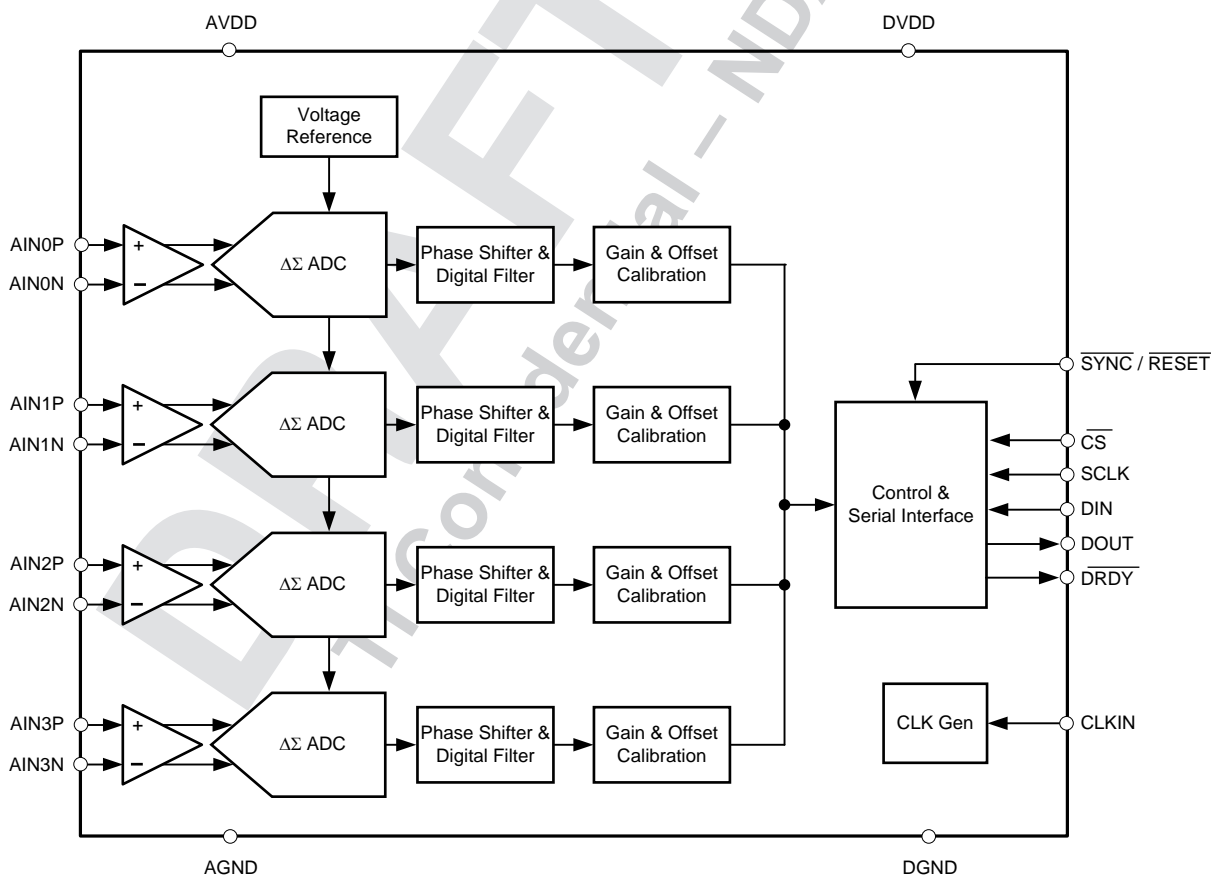
7 Detailed Description**7.1 Overview**

The ADS131M04 is a low-power, four-channel, simultaneously-sampling, 24-bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) with a low-drift internal reference voltage. The dynamic range, size, feature set and power consumption are optimized for cost-sensitive applications requiring simultaneous sampling.

The ADS131M04 requires both analog and digital supplies. The analog power supply (AVDD - AGND) can operate between 2.7 V and 3.6 V. An integrated negative charge pump allows absolute input voltages as low as 1.3 V below AGND which enables measurements of input signals varying around ground with a single-ended power supply. The digital power supply (DVDD - DGND) accepts both 1.8-V and 3.3-V supplies. The device features a programmable gain amplifier (PGA) with gains up to 128. An integrated input precharge circuit enabled at gains greater than 4 ensures high input impedance at high PGA gain settings. The ADC receives its reference voltage from an integrated 1.2-V reference. The device allows differential input voltages as large as the reference. Three power scaling modes allow designers to trade power for ADC dynamic range.

Each channel on the ADS131M04 contains a digital decimation filter which demodulates the output of the delta-sigma modulators. The filter enables data rates as high as 32 kSPS per channel in high resolution mode. The device allows configuration of the relative phase of the samples between channels enabling accurate compensation for sensor phase response. Offset and gain calibration registers can be programmed to automatically adjust output samples for measured offset and gain errors. A detailed diagram of the ADS131M04 is shown in the [Functional Block Diagram](#) section.

The device communicates via an SPI-compatible interface. Several SPI commands and internal registers control the operation of the ADS131M04. Other devices can easily be added to the same SPI bus by adding discrete CS control lines. The SYNC/RESET pin can be used to synchronize conversions between multiple ADS131M04 devices as well as to maintain synchronization with external events.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Input ESD Protection Circuitry

Basic electrostatic discharge (ESD) circuitry protects the ADS131M04 inputs from ESD and overvoltage events in conjunction with external circuits and assemblies. Figure 1 shows a simplified representation of the ESD circuit. The protection for input voltages exceeding AVDD can be modeled as a simple diode.

The ADS131M04 has an integrated negative charge pump that allows input voltages below AGND with a unipolar supply. Consequently, shunt diodes between the inputs and AGND cannot be used to clamp excessive negative input voltages. Instead, the negative charge pump voltage, V_{NCP} , controls the voltage at which the low-side protection devices begin conducting. The charge pump cannot provide a large amount of current. The mechanism shown in Figure 1 ensures current provided by the charge pump is limited in case of an undervoltage event. The vast majority of the current flows between the collector and emitter of the transistor. Take care to prevent input voltages or currents from exceeding the limits provided in the [Absolute Maximum Ratings](#) table.

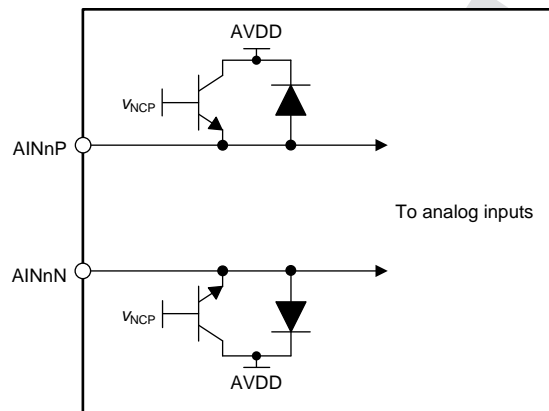


Figure 1. Input ESD Protection Circuitry

7.3.2 Input Multiplexer

Each channel of the ADS131M04 has a dedicated input multiplexer. The multiplexer controls which signals are routed to the ADC channels. Configure the input multiplexer using the MUXn[1:0] bits in the CHn_CFG register. The input multiplexer allows the following things to be connected to the ADC channel:

- The analog input pins corresponding to the given channel
- Shorted to AGND which is helpful for offset calibration
- AC test signal
- DC test signal

Refer to the [Internal Test Signals](#) section for more information about the test signals. Figure 2 shows a diagram of the input multiplexer on the ADS131M04.

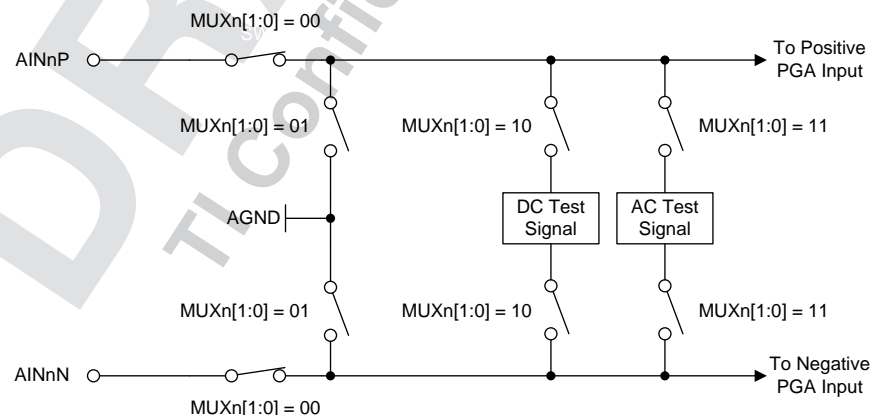


Figure 2. Input Multiplexer

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

Feature Description (continued)**7.3.3 Programmable Gain Amplifier (PGA)**

Each channel of the ADS131M04 features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, 4, 8, 16, 32, 64, and 128. The gains for all channels are individually controlled by the PGAGAINn bits for each channel in the GAIN1 register.

Varying the PGA gain will scale the differential full-scale input voltage range (FSR) of the ADC. Equation 1 describes the relationship between FSR and gain. Equation 1 uses the internal reference voltage, 1.2 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$\text{FSR} = \pm 1.2 \text{ V} / \text{Gain} \quad (1)$$

Table 1 shows the corresponding full-scale ranges for each gain setting.

Table 1. Full-Scale Range

GAIN SETTING	FSR
1	$\pm 1.2 \text{ V}$
2	$\pm 600 \text{ mV}$
4	$\pm 300 \text{ mV}$
8	$\pm 150 \text{ mV}$
16	$\pm 75 \text{ mV}$
32	$\pm 37.5 \text{ mV}$
64	$\pm 18.75 \text{ mV}$
128	$\pm 9.375 \text{ mV}$

The input impedance of the PGA dominates the input impedance characteristics of the ADS131M04. The PGA input impedance for gain settings up to 4 behaves according to Equation 2 without accounting for device tolerance and change over temperature. Minimize output impedance of the circuit which drives the ADS131M04 inputs to obtain the best possible gain error, INL, and distortion performance.

$$317 \text{ k}\Omega \times f_{\text{MOD}} / 4.096 \text{ MHz}$$

where

- f_{MOD} is the delta-sigma modulator frequency, $f_{\text{CLKIN}}/2$ (2)

The device utilizes an input precharge circuit for PGA gain settings of 8 and higher. There is no formula to govern the input impedance in these settings. The specified input impedance is based on characterization.

7.3.4 Voltage Reference

The ADS131M04 uses an internally-generated, low-drift bandgap voltage to supply the reference for the ADC. The reference has a nominal voltage of 1.2 V, allowing the differential input voltage to swing from -1.2 V to 1.2 V . The reference circuitry starts up very quickly to accommodate the fast-startup feature of this device. The device waits until after the reference circuitry is fully settled before generating conversion data. There is no need to wait extra time following the time the first conversion result is ready.

7.3.5 Clocking and Power Modes

A CMOS clock must be provided at the CLKIN pin continuously while the ADS131M04 is running in normal operation. The frequency of the clock can be scaled in conjunction with the power mode to provide a tradeoff between power and dynamic range.

The PWR[1:0] bits in the CLOCK register allow the device to be configured in one of three power modes: High Resolution (HR) mode, Low-Power (LP) mode, and Very Low-Power (VLP) mode. Changing the PWR[1:0] bits will scale bias internal currents to achieve the expected power levels. The external clock frequency must follow the guidance provided in the Recommended Operating Conditions corresponding to the intended power mode in order for the device to perform according to specified behavior.

7.3.6 $\Delta\Sigma$ Modulator

The ADS131M04 utilizes a delta-sigma modulator to convert the analog input voltage to a ones density modulated digital bit-stream. The delta-sigma modulator oversamples the input voltage at a frequency many times greater than the output data rate. The modulator frequency, f_{MOD} of the ADS131M04 is equal to half the frequency of the clock provided at the CLKIN pin.

The output of the modulator is fed back to the modulator input through a DAC as a means of error correction. This feedback mechanism shapes the modulator quantization noise in the frequency domain to make it more dense at higher frequencies and less dense in the band of interest. The digital decimation filter following the delta-sigma modulator significantly attenuates the out-of-band modulator quantization noise allowing the device to provide excellent dynamic range.

7.3.7 Digital Decimation Filter

The digital decimation filter significantly attenuates the out-of-band quantization noise from the delta-sigma modulator which is shaped in the frequency domain. The digital filter is a linear phase, finite impulse response (FIR), low-pass, third order sinc filter (sinc^3). The filter demodulates the output of the delta-sigma modulator by averaging. The data passed through the filter is decimated, or downsampled, to reduce the output frequency from the modulator frequency to the data rate. The decimation factor is called the oversampling ratio (OSR). The OSR is configurable and is set by the OSR[2:0] bits in the CLOCK register.

The OSR dictates the period for which the filter averages the modulator output which determines the filter bandwidth. The filter bandwidth directly affects the noise performance of the ADC because lower bandwidth results in lower noise while higher bandwidth results in higher noise. Refer to the TBD section for the noise specifications for various OSR settings. There are eight OSR settings in the ADS131M04 allowing eight different data rate settings for any given master clock frequency.

[Equation 3](#) shows the z-domain transfer function for the digital filter. [Equation 4](#) shows the transfer function in terms of the continuous-time frequency parameter f .

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3$$

where

- N is the OSR

$$|H(f)| = \left| \frac{\sin \left[\frac{N\pi f}{f_{MOD}} \right]}{N \times \sin \left[\frac{\pi f}{f_{MOD}} \right]} \right|^3$$

where

- N is the OSR

The filter has infinite attenuation at integer multiples of the data rate except for integer multiples of f_{MOD} . Like all digital filters, the digital filter response on the ADS131M04 repeats at integer multiples of the modulator frequency, f_{MOD} . The data rate and filter notch frequencies will scale with f_{MOD} .

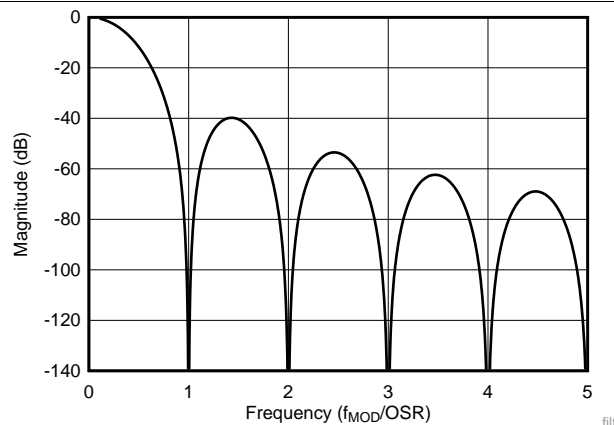
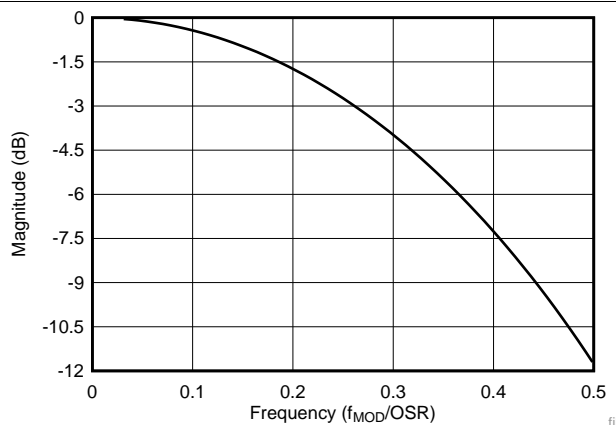
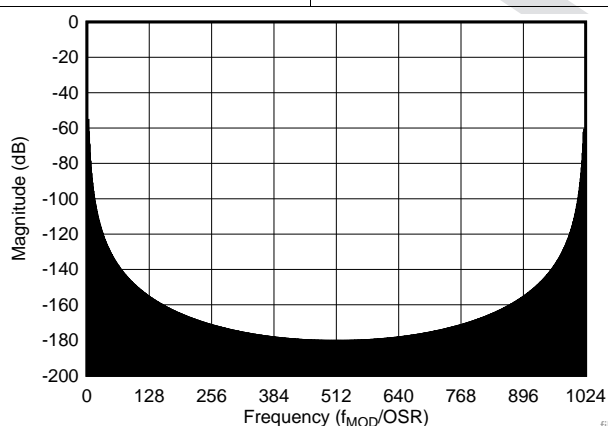
When possible, plan frequencies for unrelated periodic processes in the application for integer multiples of the data rate such that any parasitic effect they have on data acquisition is effectively cancelled by the notches of the digital filter. Avoid, whenever possible, frequencies near integer multiples of f_{MOD} because tones in those bands may alias to the band of interest.

[Figure 3](#) to [Figure 5](#) illustrate the digital filter response.

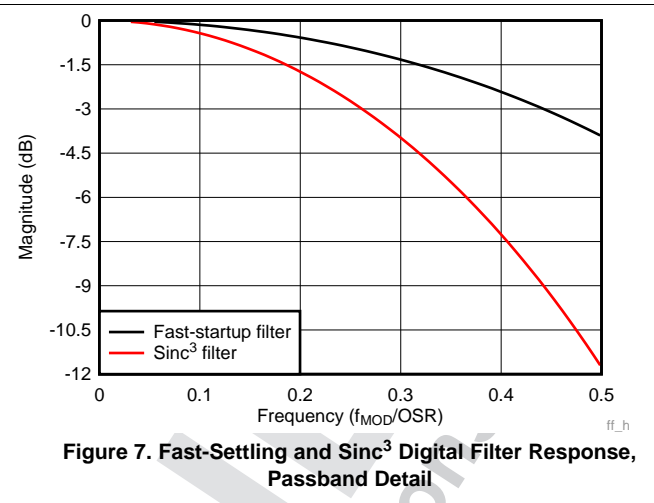
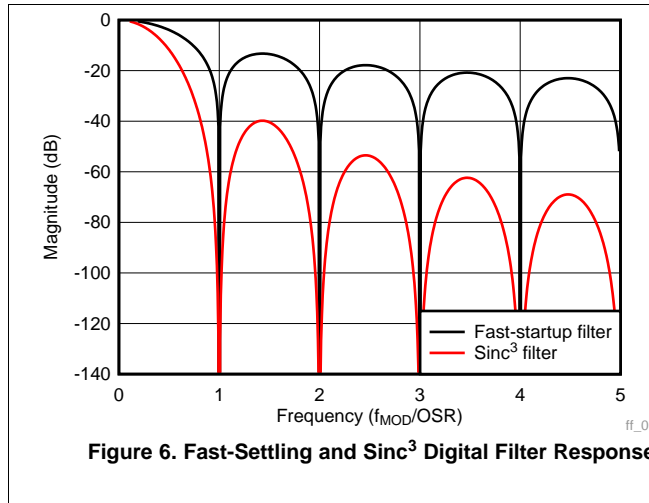
ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

**Figure 3. Sinc³ Digital Filter Response****Figure 4. Sinc³ Digital Filter Response, Passband Detail****Figure 5. Sinc³ Digital Filter Response, OSR 1024, Stopband Detail****7.3.7.1 Fast-Startup Response**

The ADS131M04 starts up and generates conversion data very quickly following supply ramp or reset. This is achieved in part by using a dual digital filter path. When the device first starts up, data is generated using a first-order sinc filter. After two samples, the device switches to the sinc³ filter where it remains until the next time the device is powered down or reset. and show the digital filter response of the fast-settling filter with the sinc³ filter response superimposed to illustrate the contrast. The fast-settling filter's superior settling time is counterbalanced by wider bandwidth and less stopband attenuation. Consequently, the noise performance obtainable from using this digital filter is not as high as with the sinc³ filter. The first two samples available from the ADS131M04 after supply ramp or reset have noise performance and frequency response corresponding to the fast-settling filter, whereas subsequent samples have noise performance and frequency response consistent with the sinc³ filter. Refer to the [Fast Startup](#) section for more details about the fast startup capabilities of the ADS131M04.



7.3.8 Internal Test Signals

The ADS131M04 features two internal analog test signal generators that are useful for troubleshooting and diagnosis. Both AC and DC test signals can be applied to the channel inputs through the input multiplexer. The multiplexer is controlled through the MUXn[1:0] bits in the CHn_CFG register. The test signals are created by internally dividing the reference voltage.

The DC test signal is nominally $2/15 \times V_{REF}$. The test signal automatically adjusts its voltage level with the gain setting such that the ADC always measures a signal which is $2/15 \times V_{Diff_Max}$. For example, at a gain of 1, this equates to 160 mV. At a gain of 2, this voltage is 80 mV.

The AC test signal has the same magnitude as the DC test signal, but appears as a square wave at a frequency of $f_{MOD} / 4096$. For example, if CLKIN is driven with a 8.192 MHz clock, f_{MOD} is 4.096 MHz. Therefore, the AC test signal has a frequency of 1 kHz when f_{MOD} is 4.096 MHz.

A square wave is composed of the fundamental frequency and the sum of an infinite number of harmonics with magnitudes which decrease with frequency. Consequently, the test signal's various frequency components are low-pass filtered according to the frequency response of the digital decimation filter on the ADS131M04.

7.3.9 Channel Phase Calibration

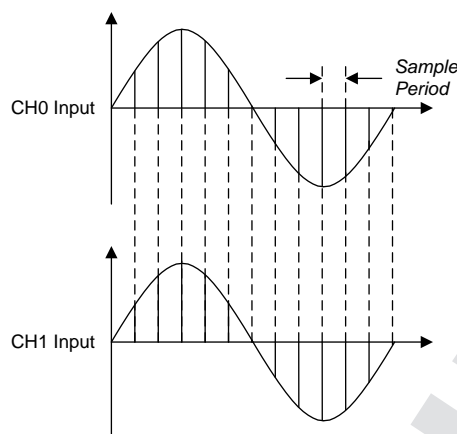
The ADS131M04 allows fine adjustment of the sample period between channels through the use of channel phase calibration. This feature is helpful when different channels are measuring the outputs of different types of sensors which have different phase responses. For example, in power metrology applications, voltage may be measured by a voltage divider, whereas current is measured using a current transformer which exhibits a phase difference between its input and output signals. The differences in phase between the voltage and current measurement must be compensated to measure the power and related parameters accurately.

The phase setting of channels is configured by the PHASEn[9:0] bits in the CHn_CFG register corresponding to the channel whose phase adjustment is desired. The register value is a 10-bit two's complement value corresponding to the number of modulator clock cycles of phase offset compared to a reference phase of 0.

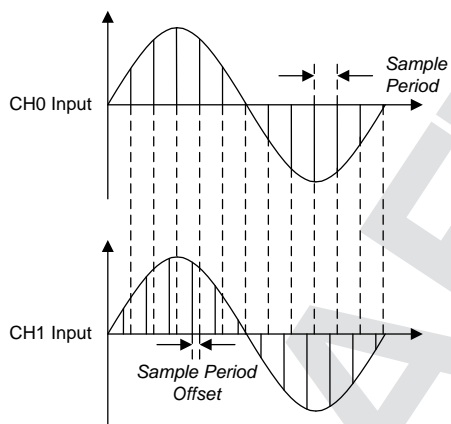
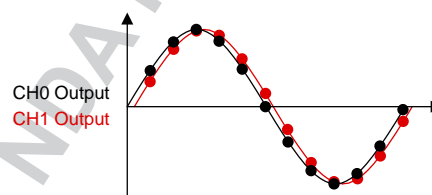
The mechanism for achieving phase adjustment derives from the delta-sigma architecture. The delta-sigma modulator produces samples continuously at the modulator frequency, f_{MOD} . Those samples are filtered and decimated to the output data rate by the digital filter. The ratio between f_{MOD} and the data rate is the oversampling ratio (OSR). Each conversion result corresponds to an OSR number of modulator samples provided to the digital filter. When the different channels of the ADS131M04 have no programmed phase offset between them, the modulator clock cycles corresponding to the conversion results of the different channels are aligned in the time domain. Figure 8 shows an example scenario where the voltage input to channel 1 has no phase offset from channel 0.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Figure 8. Two Channel Outputs with Equal Phase Settings**

However, the sample period of one channel can be shifted with respect to another. If the inputs to both channels are sinusoids of the same frequency and the samples for those channels are retrieved by the host at the same time, the effect is that the phase of the channel whose sample period has been modified appears "shifted". [Figure 9](#) illustrates how the modulator clocks corresponding to the samples are shifted between channels. [Figure 10](#) illustrates how the samples appear as having generated a phase shift when they are retrieved by the host.

**Figure 9. Channel 1 With Positive Sample Phase Shift with Respect to Channel 0****Figure 10. Channels 1 and 0 from the Perspective of the Host**

The valid range of settings is $-\text{OSR} / 2$ to $(\text{OSR} / 2) - 1$, except for OSRs greater than 1024, where the phase calibration setting is limited to -512 to 511 . If a value outside of $-\text{OSR} / 2$ and $(\text{OSR} / 2) - 1$ is programmed, the device internally clips the value to the nearest limit. For example, if the OSR setting is programmed to 64 and the PHASEn[9:0] bits are programmed to 0001100100b corresponding to 100 modulator clock cycles, the device will adjust the phase of the channel by 31 because that is the upper limit of phase calibration for that OSR setting. [Table 2](#) gives the range of phase calibration settings for various OSR settings.

Table 2. Phase Calibration Setting Limits for Different OSR Settings

OSR Setting	Phase Offset Range (t_{MOD})	PHASE[9:0] Bits Range
128	–64 to 63	11 1100 0000b to 00 0011 1111b
256	–128 to 127	11 1000 0000b to 00 0111 1111b
512	–256 to 255	11 0000 0000b to 00 1111 1111b
1024	–512 to 511	10 0000 0000b to 01 1111 1111b
2048	–512 to 511	10 0000 0000b to 01 1111 1111b
4096	–512 to 511	10 0000 0000b to 01 1111 1111b
8192	–512 to 511	10 0000 0000b to 01 1111 1111b
16384	–512 to 511	10 0000 0000b to 01 1111 1111b

To create a phase shift larger than half the sample period for OSRs less than 2048, create an integer multiple sample period phase shift by modifying the indexes of the data points between channels with respect to one another in software. Subsequently, use the internal phase calibration function on the ADS131M04 to create the remaining fractional sample period phase shift. For example, to create a phase shift of 2.25 samples between channels 0 and 1, create a phase shift of 2 samples by aligning sample N in channel 0's output data stream with sample N+2 in channel 1's output datastream in the host software. Make the remaining 0.25 sample adjustment using the ADS131M04 phase calibration function.

The phase calibration settings of the channels affect the timing of the new data interrupt signal \overline{DRDY} . Refer to the [DRDY](#) section for more details about how phase calibration affects \overline{DRDY} .

7.3.10 Calibration Registers

The calibration registers allow for the automatic computation of calibrated ADC conversion results from pre-programmed values. The host can rely on the device to automatically correct for system gain and offset after the error correction terms have been programmed into the corresponding device registers.

The offset calibration registers are used to correct for system offset error, otherwise known as zero error. Offset error corresponds to the ADC output when the input to the system is zero. The ADS131M04 corrects for offset errors by subtracting the contents of the $OCALn[23:0]$ register bits in the CHn_OCAL_MSB and CHn_OCAL_LSB registers from the conversion result for that channel prior to delivering it to the interface for retrieval by the host. There are separate CHn_OCAL_MSB and CHn_OCAL_LSB registers for each channel, which allows the programming of separate offset calibration terms for each channel. The contents of the $OCALn[23:0]$ bits are interpreted by the device as 24-bit 2's complement values, the form of which corresponds exactly to that of the ADC data.

The gain calibration registers are used to correct for system gain error. Gain error corresponds to the deviation of gain of the system from its ideal value. The ADS131M04 corrects for gain errors by multiplying the ADC conversion result by a value resulting from the contents of the $GCALn[23:0]$ register bits in the CHn_GCAL_MSB and CHn_GCAL_LSB registers prior to delivering it to the interface for retrieval by the host. There are separate CHn_GCAL_MSB and CHn_GCAL_LSB registers for each channel, allows the programming of separate gain calibration terms for each channel. The contents of the $GCALn[23:0]$ bits are interpreted by the device as 24-bit unsigned values corresponding to linear steps ranging from gains of 0 to $2 - (2^{24} - 1) / 2^{24}$. [Table 3](#) describes the relationship between the $GCALn[23:0]$ bit values and the realized gain calibration factor.

Table 3. $GCALn[23:0]$ Bit Mapping

$GCALn[23:0]$ VALUE	GAIN CALIBRATION FACTOR
000000h	0
000001h	1.19×10^{-7}
800000h	1
FFFFFFEh	$2 - 2.38 \times 10^{-7}$
FFFFFFFh	$2 - 1.19 \times 10^{-7}$

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

There is no need to enable the calibration registers. They are always in use. The $\text{OCALn}[23:0]$ bits have a default value of 000000h resulting on no offset correction. Similarly, the $\text{GCALn}[23:0]$ bits default to 800000h resulting in a gain calibration factor of 1.

Figure 11 shows a block diagram illustrating the mechanics of the calibration registers on one channel of the ADS131M04.

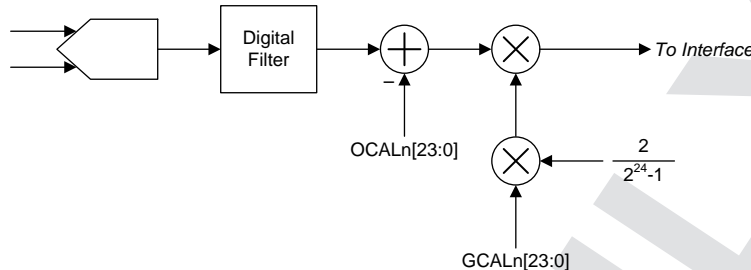


Figure 11. Calibration Block Diagram

7.3.11 Fast Startup

The ADS131M04 begins generating conversion data very soon after startup. This feature is useful for applications such as circuit breakers powered from the mains which require a fast determination of the input voltage shortly after power is applied to the device. Fast startup is accomplished via two mechanisms. First, the device's internal power supply circuitry is designed specifically to enable fast startup. Second, the digital decimation filter dynamically switches from a fast-settling filter to a sinc^3 filter once the sinc^3 filter has had time to settle.

After supplies have ramped to 90% of their final value, the device requires t_{POR} for the internal circuitry to settle. The end of t_{POR} is indicated by a transition of $\overline{\text{DRDY}}$ from low to high. The transition of $\overline{\text{DRDY}}$ from low to high also indicates the SPI interface is ready to accept commands.

The delta-sigma modulators of the ADS131M04 begin sampling the input signal after a modulator settling time of $8 \times t_{\text{MOD}}$ following the end of t_{POR} . The device waits until CLKIN is toggling after t_{POR} for the modulators to begin settling. Therefore, provide a valid clock signal on CLKIN as soon as possible after supply ramp to achieve the fastest possible startup time.

The data generated by the delta-sigma modulators are fed to the digital filter blocks following the modulator settling. The data is provided to both the fast-settling filters and the sinc^3 filters. The fast-settling filter requires only one data rate period to provide settled data. Meanwhile, the sinc^3 filter requires three data rate periods to settle. The fast-settling filter generates the output data for the two interim ADC output samples indicated by $\overline{\text{DRDY}}$ transitioning from high to low while the sinc^3 filter is settling. The device disables the fast-settling filter and provides conversion data from the sinc^3 filter for the third and following samples.

The fast-settling filter provides conversion data which is significantly noisier than that which comes from the sinc^3 filter, but allows the device to provide settled conversion data during the lengthy settling time of the more accurate sinc^3 digital filter. Table TBD provides the noise specifications of the ADS131M04 when using the fast-settling filter. and compare the frequency domain transfer functions of the fast-settling filter to the sinc^3 filter. If the level of precision provided by the fast-settling filter is insufficient even for the first samples immediately following startup, ignore the first two instances of $\overline{\text{DRDY}}$ toggling from high to low and begin collecting data on the third.

7.3.11.1 Startup Following Reset

The process of startup is similar following a RESET command or a pin reset using the $\overline{\text{SYNC/RESET}}$ pin from what occurs at power up. There is no t_{POR} in the case of command or pin reset because the supplies have already ramped. However, in either case, the device waits the modulator settling time of $8 \times t_{\text{MOD}}$ before providing modulator samples to the two digital filters. The fast-settling filter is enabled for the first two output samples.

7.3.12 Communication Cyclic Redundancy Check (CRC)

The ADS131M04 features a cyclic redundancy check engine on both input and output data to mitigate SPI communication errors. The CRC word is 16 bits wide in the case of either input or output CRC. Coverage includes all words in the frame where the CRC occurs, including padded bits in the case of a 32-bit word size.

Input CRC is optional and can be enabled and disabled by writing the RX_CRC_EN bit in the MODE register. Input CRC is disabled by default. The device checks the provided input CRC against the CRC it generates based on the input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands in case of a failed CRC check if the recieved command was any besides WREG. The device writes registers as the data is shifted into the device during a WREG command. Therefore, the registers are written before the input CRC is provided during a WREG command. The device sets the CRC_ERR bit in the STATUS register in all cases of a CRC error.

Output CRC is not optional. It always appears at the end of the output frame. The host can ignore the data if it does not wish to use output CRC.

There are two types of CRC available: CCITT CRC and ANSI CRC (CRC-16). The CRC setting determines the algorithm for both the input and output CRC. The CRC type is programmed by the CRC_TYPE bit in the MODE register. Table 4 shows the details of the two CRC types.

Table 4. CRC Types

CRC Type	Polynomial	Binary Polynomial
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

7.3.13 Register Map CRC

The ADS131M04 performs a CRC on its own register map as a means to check for unintended changes to the registers. Enable the register map CRC by setting the REG_CRC_EN bit in the MODE register. Once enabled, the device constantly calculates the register map CRC using each bit in the writable register space.

The calculated CRC is a 16-bit value and is stored in the REGMAP_CRC register. The calculation is done using one register map bit per modulator clock period and constantly checks the result against the previous calculation. The REG_MAP bit in the STATUS register is set to flag the host if the register map CRC changes, including due to register writes. The bit is cleared by reading the STATUS register, or by the STATUS register being output as a response to the NULL command.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.4 Device Functional Modes**

Figure 12 shows a state diagram depicting the major functional modes of the ADS131M04 and the transitions between them.

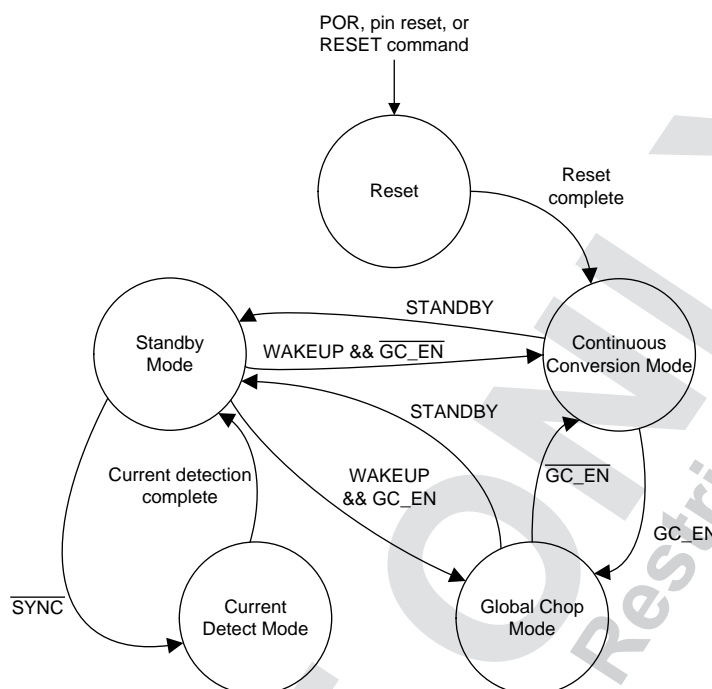


Figure 12. State Diagram Depicting Device Functional Modes

7.4.1 Power-Up and Reset

The ADS131M04 is reset in one of three ways: either by a power-on reset (POR), by the $\overline{\text{SYNC/RESET}}$ pin, or by a RESET command. After a reset occurs, the configuration registers are reset to the default values and the device begins generating conversion data as soon as it is available.

7.4.1.1 Power-On Reset

Power-On Reset (POR) is the reset which occurs when a valid operating voltage is first applied to the supplies. The POR process requires t_{POR} from when the supply voltages have reached 90% of their nominal value. Internal circuitry powers up and the registers are set to their default state during this time. The $\overline{\text{DRDY}}$ pin transitions from low to high immediately after t_{POR} indicating the SPI interface is ready for communication. The device ignores SPI communication before this point.

7.4.1.2 $\overline{\text{SYNC/RESET}}$ Pin

The $\overline{\text{SYNC/RESET}}$ pin is an active low, dual function pin that generates a reset if it is held low for more than t_{SRLRST} . The device maintains a reset state until $\overline{\text{SYNC/RESET}}$ is returned high. The host must wait at least t_{REGACQ} after the time $\overline{\text{SYNC/RESET}}$ is brought high for the registers to assume their default values before communicating with the device via SPI. Conversion data are generated immediately after the registers have been reset to their default values as described in [Startup Following Reset](#).

7.4.1.3 RESET Command

The ADS131M04 can be reset via an SPI command (0011h). The device communicates in frames of fixed length. Refer to the [SPI Communication Frames](#) section for details about SPI data framing on the ADS131M04. The RESET command occurs in the first word of the data frame, but the command is not latched by the device until the entire frame is complete. Six words are required to complete a frame on the ADS131M04.

Device Functional Modes (continued)

Reset occurs immediately after the command is latched. The host must wait t_{REGACQ} before communicating with the device to ensure the registers have assumed their default settings. Conversion data are generated immediately after the registers have been reset to their default values as described in [Startup Following Reset](#).

7.4.2 Conversion Mode

There are two ADC conversion modes on the ADS131M04: Continuous Conversion and Global Chop mode. Continuous Conversion mode is a mode where ADC conversions are generated constantly by the ADC at a rate defined by $f_{\text{MOD}} / \text{OSR}$. Global Chop mode differs from Continuous Conversion mode because it periodically chops, or swaps, the inputs which reduces system offset errors at the cost of settling time between when the inputs are swapped. In either Continuous Conversion or Global Chop mode, there are three power modes which provide flexible options to scale power with bandwidth and dynamic range.

7.4.2.1 Continuous Conversion Mode

Continuous Conversion mode is the mode in which ADC data are generated constantly at the rate of $f_{\text{MOD}} / \text{OSR}$. New data are indicated by a $\overline{\text{DRDY}}$ falling edge at this rate. Continuous Conversion mode is intended for measuring AC signals because it allows for higher output data rates than Global Chop mode.

7.4.2.2 Global Chop Mode

In Global Chop mode, the ADC swaps its inputs prior to generating each sample in order to reduce the offset error inherent to the inputs caused by slight mismatch in the internal circuitry. This mode is intended for applications which measure DC input signals due to its very low offset error.

This mode always utilizes the sinc^3 digital filter which requires $3 \times \text{OSR} / f_{\text{MOD}}$ to generate a settled result. Therefore, the device waits $3 \times \text{OSR} / f_{\text{MOD}}$ after the modulator begins sampling for the filter to settle before providing a sample result to the host.

The ADS131M04 allows a programmable delay between the end of the previous sample period and the beginning of the subsequent sample period after the inputs have been chopped. This delay is to allow for the external input circuitry to settle because the chopping switches interface directly with the pins. The $\text{GC_DLY}[3:0]$ bits in the CFG register configure the delay after chopping. The delay is measured in modulator clock periods from 2 to 65,536.

Phase calibration is automatically disabled in Global Chop mode. A $\overline{\text{DRDY}}$ falling edge is generated each time a new sample is generated. [Equation 5](#) describes the sample period in Global Chop mode.

$$t_{\text{SAMPLE}} = t_{\text{GC_DLY}} + 3 \times \text{OSR} / f_{\text{MOD}} \quad (5)$$

7.4.2.3 Power Modes

In both Continuous Conversion and Global Chop modes, there are three selectable power modes that allow the scaling of power with bandwidth and performance: High-Resolution (HR) mode, Low-Power (LP) mode, and Very Low-Power (VLP) mode. The mode is selected by the $\text{PWR}[1:0]$ bits in the CLOCK register. Refer to the [Recommended Operating Conditions](#) section for restrictions on the CLKIN frequency for each power mode.

7.4.3 Standby Mode

Standby mode is a low-power state in which all the channels are disabled, and the reference and other non-essential circuitry are powered down. This mode differs from completely powering down the device because the device will retain its register settings. Enter Standby Mode by sending the STANDBY command (0022h). Stop toggling CLKIN while the device is in Standby mode to minimize device power consumption. Exit Standby mode by sending the WAKEUP command (0033h). The device waits $t_{\text{MODESETTLE}}$ before beginning conversions after exiting Standby mode.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Device Functional Modes (continued)****7.4.4 Current Detect Mode**

Current Detect mode is a special mode which is helpful for applications which require tamper detection when the equipment is in a low-power state. In this mode, the ADS131M04 collects a configurable number of samples at 2.7 kSPS and compares the absolute value of the results to a programmable threshold. If a configurable number of the results exceed the threshold, the host is notified via a DRDY falling edge and the device returns to Standby mode. Enter Current Detect mode by providing a negative pulse on SYNC/RESET with a pulse width less than t_{SRLRST} while in Standby Mode. Current Detect Mode can only be entered from Standby Mode.

The device uses a limited power operating mode to generate conversions in Current Detect mode. The conversion results are only used for comparison by the internal digital threshold comparator and are not accessible by the host. The device uses an internal oscillator which enables the device to capture the data without the use of the external clock input. Do not toggle CLKIN while in Current Detect mode to minimize device power consumption.

Current Detect mode is configured in the CFG, THRS_HLD_MSB, and THRS_HLD_LSB registers. Enable and disable Current Detect mode by toggling the CD_EN bit in the CFG register. The THRS_HLD_MSB and THRS_HLD_LSB registers contain the CD_THRSH[23:0] bits which represent the digital comparator threshold value during current detection.

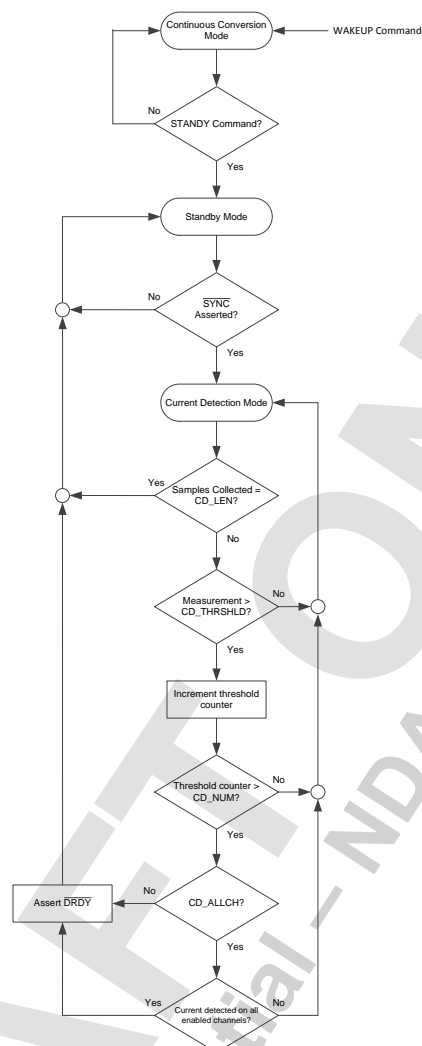
The CD_NUM[2:0] bits configure the number of samples that must exceed the threshold in order for detection to occur. The programmable values in CD_NUM[2:0] configure the number of samples which need to exceed the threshold for detection to occur. The purpose of requiring multiple samples for detection is to control for noisy values that may exceed the threshold, but do not represent a high enough power level to warrant action by the host. In summary, the conversion result must exceed the value programmed in CD_THRSH[23:0] a number of times that is represented by the value stored in CD_NUM[2:0].

The number of samples used for current detection are programmed by the CD_LEN[2:0] bits in the CFG register. The number of samples used for current detection range from 128 to 3584.

The device can be configured to notify the host based on any of the results from either individual channels, all channels, or any combination of channels. The CD_ALLCH bit in the CFG register determines how many channels are required to exceed the programmed thresholds to trigger current detection. When the bit is 1, all enabled channels are required to meet the current detection requirements in order for the host to be notified. If the bit is 0, any enabled channel will trigger a current detection notification if the requirements are met. Enable and disable channels using the CHn_EN bits in the CLK register to control which combination of channels must meet the requirements to trigger a current detection notification.

Figure 13 shows a flow chart which illustrates the current detection process on the ADS131M04.

Device Functional Modes (continued)



PRODUCT PREVIEW

Figure 13. Current Detect Mode Flow Chart

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.5 Programming****7.5.1 Interface**

The ADS131M04 uses an SPI-compatible interface for configuration and conversion data retrieval. The device always behaves as an SPI slave; SCLK and \overline{CS} are inputs to the interface. The interface behaves with negative SCLK edge latch polarity (CPOL = 0) and output data begins on the first rising edge of SCLK (CPHA = 1). The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: SCLK, \overline{CS} , DIN (MOSI), and DOUT (MOSI). In addition, there are two other digital pins which provide additional functionality. The \overline{DRDY} pin serves as a flag to the host to indicate new data. The SYNC/RESET pins is a dual function pin which allows synchronization of conversions to an external event and allows for a hardware device reset.

7.5.1.1 \overline{CS}

The \overline{CS} pin is an active low input signal which selects the device for communication. The device ignores any communication and DOUT is high impedance when \overline{CS} is held high. Hold \overline{CS} low for the duration of a communication frame without toggling to ensure proper communication. The interface is reset each time \overline{CS} is brought from low to high.

7.5.1.2 SCLK

The SCLK pin is an input which serves as the serial clock for the interface. Output data on the DOUT pin transitions on the rising edge of SCLK and input data on DIN is latched on the falling edge of SCLK.

7.5.1.3 DIN

The DIN pin is the "master out, slave in (MOSI)" pin for the device. This pin is where serial commands are shifted in by the device with each SCLK falling edge when the \overline{CS} pin is low.

7.5.1.4 DOUT

The DOUT pin is the "master in, slave out (MISO)" pin for the device. The device will shift out command responses and ADC conversion data serially with each rising SCLK edge when the \overline{CS} pin is low. This pin assumes a high-impedance state when \overline{CS} is high.

7.5.1.5 \overline{DRDY}

The \overline{DRDY} pin is an active low output which indicates that data is ready in Conversion mode or that the requirements have been met for current detection while in Current Detect mode. Connect the \overline{DRDY} pin to an input on the host to trigger periodic data retrieval in Conversion mode. The period between each \overline{DRDY} falling edge is the data rate period.

The timing of \overline{DRDY} with respect to the sampling of a given channel on the ADS131M04 depends on the phase calibration setting of the channel and the state of the $\overline{DRDY_SEL}[1:0]$ bits in the MODE register. Setting the bits to 00b configures \overline{DRDY} to assert when the channel with the largest positive phase setting, or the most lagging, has a ready conversion result. When the bits are 01b, the device will assert \overline{DRDY} each time any channel's data is ready. Finally, setting the bits to either 10b or 11b configures the device to assert \overline{DRDY} when the channel with the most negative phase setting, or the most leading, has ready conversion data. Changing bits have no effect on \overline{DRDY} behavior in Global Chop mode because phase calibration is automatically disabled in Global Chop mode.

The $\overline{DRDY_HIZ}$ bit in the MODE register configures the state of the \overline{DRDY} pin when deasserted. By default, the bit is 0b meaning the pin remains high. When the bit is 1b, \overline{DRDY} behaves like an open drain digital output. Use a 100 k Ω pull-up resistor to keep the pin high when \overline{DRDY} is not asserted.

The $\overline{DRDY_FMT}$ bit in the MODE register determines the format of the \overline{DRDY} signal. When the bit is 0b, new data is indicated by \overline{DRDY} changing from high to low and remaining low until either all of the conversion data is shifted out of the device, or immediately before the next time \overline{DRDY} is scheduled to transition low. When the $\overline{DRDY_FMT}$ bit is 1b, new data is indicated by a short negative pulse on the \overline{DRDY} pin. If the host does not read conversion data after the \overline{DRDY} pulse when $\overline{DRDY_FMT}$ is 1b, the device will not provide another \overline{DRDY} pulse until the second following instance data is ready due to the mechanism for how the pulse is generated.

Programming (continued)

7.5.1.6 SYNC/RESET

The $\overline{\text{SYNC/RESET}}$ pin is a multi-function digital input pin which serves primarily to allow the host to synchronize conversions to an external process or to reset the device. Refer to the [Synchronization](#) section for more details regarding the synchronization function. Refer to the [SYNC/RESET Pin](#) section for more details regarding pin reset.

7.5.1.7 SPI Communication Frames

SPI communication on the ADS131M04 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16-bits, 24-bits, or 32-bits by programming the WLENGTH[1:0] bits in the MODE register.

The interface is full duplex, meaning it is capable of transmitting data on DOUT while simultaneously receiving data on DIN. The input frame which the host writes on DIN always begins with a command. The first word on the output frame which the device writes on DOUT always begins with the response to the command that was written on the previous input frame. The number of words in a command depends on the command provided. For most commands, there are six words in a frame. The host provides on DIN the command, the command's CRC if input CRC is enabled or a word of zeros if it is disabled, and four additional words of zeros. The device outputs simultaneously on DOUT the response from the previous frame's command, four words of ADC data representing the four ADC channels, and a CRC word. [Figure 14](#) illustrates a typical single word command frame structure.

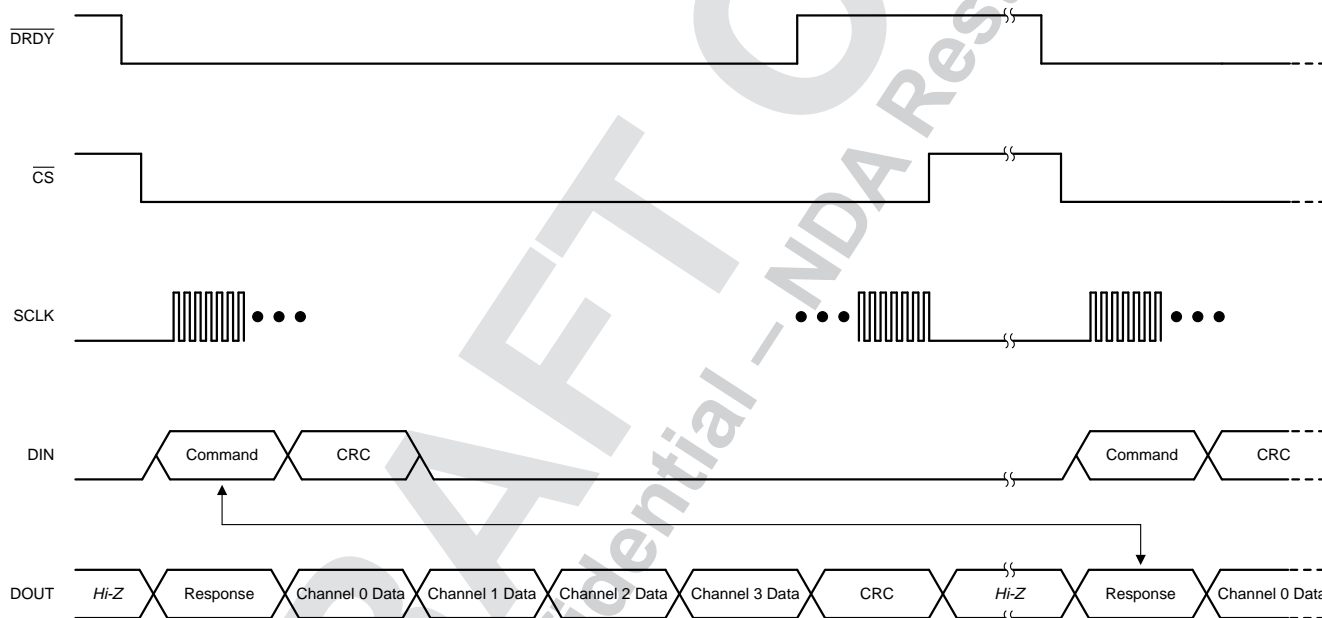


Figure 14. Typical Data Frame

There are some commands which require more than six words. In the case of a read register (RREG) command where more than a single register is read, the response to the command contains the acknowledgment of the command followed by the register contents requested, which may require a larger frame depending on how many registers are read. Refer to the [RREG \(011a aaaa annn nnnn\)](#) section for more details on the RREG command.

In the case of a write register (WREG) command where more than a single register is written, the frame extends to accommodate the additional data required to communicate the register data that is to be written. Refer to the [WREG \(011a aaaa annn nnnn\)](#) section for more details on the WREG command.

[Table 6](#) contains a list of all the valid commands and their corresponding responses on the ADS131M04.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com

Programming (continued)**7.5.1.8 SPI Communication Words**

A SPI communication frame with the ADS131M04 is made of words. Words on DIN may contain commands, register settings during a register write, or a CRC of the input data. Words on DOUT can contain command responses, register settings during a register read, ADC conversion data, or CRC of the output data.

Words can be 16-, 24- or 32-bits. The word size is configured by the WLENGTH[1:0] bits in the MODE register. The device defaults to 24-bit word size. Commands, responses, CRC, and registers always contain 16-bits of actual data. Those words are always most significant bit (MSB) aligned, therefore the least significant bits (LSBs) are zero-padded to accommodate 24- or 32-bit word sizes. ADC conversion data is nominally 24-bits. The ADC data has its 8 LSBs truncated when the device is configured for 16-bit communication. There are two options for 32-bit communication available for ADC data in the WLENGTH[1:0] bits in the MODE register. Either the ADC data can be LSB padded with zeros or the data can be MSB sign extended.

7.5.1.9 ADC Conversion Data

The device provides conversion data for each channel at the data rate. The time when the data is available relative to DRDY asserting is determined by the channel phase calibration setting and the DRDY_SEL[1:0] bits in the MODE register while in Continuous Conversion mode. All data are available immediately following DRDY assertion in Global Chop mode. The conversion status of all channels is available as the DRDY[3:0] bits in the STATUS register. The STATUS register contents are automatically output as the response to the NULL command.

Conversion data is 24-bits. The data's LSBs are truncated while the device is operating with a 16-bit word size. The LSBs may be zero padded or the MSBs sign extended while operating with a 32-bit word size by configuring the WLENGTH[1:0] bits in the MODE register.

The data is given in binary two's complement. Use Equation 6 to calculate the size of one code (LSB).

$$1 \text{ LSB} = (2.4 / \text{Gain}) / 2^{24} = +\text{FS} / 2^{23} \quad (6)$$

A positive full-scale input [$V_{\text{IN}} \geq (+\text{FS} - 1 \text{ LSB}) = 1.2 / \text{Gain} - 1 \text{ LSB}$] produces an output code of 7FFFFFFh and a negative full scale input ($V_{\text{IN}} \leq -\text{FS} = -1.2 / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 5 summarizes the ideal output codes for different input signals.

Table 5. Ideal Output Code versus Input Signal

INPUT SIGNAL, $V_{\text{IN}} = V_{\text{AINP}} - V_{\text{AINN}}$	IDEAL OUTPUT CODE
$\geq \text{FS} (2^{23} - 1) / 2^{23}$	7FFFFFFh
$\text{FS} / 2^{23}$	000001h
0	000000h
$-\text{FS} / 2^{23}$	FFFFFFFh
$\leq -\text{FS}$	800000h

Figure 15 shows the mapping of the analog input signal to the output codes.

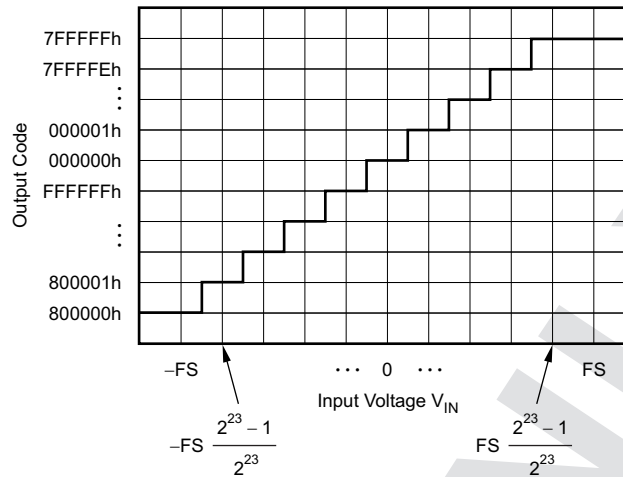


Figure 15. Code Transition Diagram

7.5.1.10 Commands

Table 6 contains a list of all valid commands, a short description of their functionality, their binary opcode, and the expected response which comes in the following frame.

Table 6. Command Definitions

COMMAND	DESCRIPTION	OPCODE	RESPONSE
NULL	No operation	0000 0000 0000 0000	STATUS register
RESET	Reset the device	0000 0000 0001 0001	1111 1111 0010 0100
RREG	Read nnn nnnn minus 1 registers beginning at address a aaaa a	101a aaaa annn nnnn	dddd dddd dddd dddd or 111a aaa annn nnnn ⁽¹⁾
WREG	Write nnn nnnn minus 1 registers beginning at address a aaaa a	011a aaaa annn nnnn	010a aaaa ammm mmmm ⁽²⁾
STANDBY	Place the device into Standby mode	0000 0000 0010 0010	0000 0000 0010 0010
WAKEUP	Wake the device from Standby mode to Conversion mode	0000 0000 0011 0011	0000 0000 0011 0011
LOCK	Lock the interface such that only NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101	0000 0101 0101 0101
UNLOCK	Unlock the interface after the interface was locked	0000 0110 0101 0101	0000 0110 0101 0101

(1) When nnn nnnn is 0, the response is the requested register's data dddd dddd dddd dddd. When nnn nnnn is greater than 0, the response will begin with 111a aaaa annn nnnn, followed by the register data.

(2) In this case mmm mmmm represents the number of registers which were actually written minus one. This value may be less than nnn nnnn in some cases.

7.5.1.10.1 NULL (0000 0000 0000 0000)

The NULL command is the "no-operation" command which results in no registers read or written, and the state of the device remains unchanged. The intended use case for the NULL command is that it is provided during typical ADC data capture.

The command response for the NULL command is the contents of the STATUS register which is read in the first word of the frame which follows the frame in which the command was provided.

7.5.1.10.2 RESET (0000 0000 0001 0001)

The RESET command will reset the ADC to its register defaults. The command is latched by the device at the end of the frame. Reset occurs immediately after the command is latched. The host must wait t_{REGACQ} before communicating with the device to ensure the registers have assumed their default settings. Refer to the [RESET Command](#) section for more information about the operation of the reset command.

ADS131M04

SBAS890 – SEPTEMBER 2018

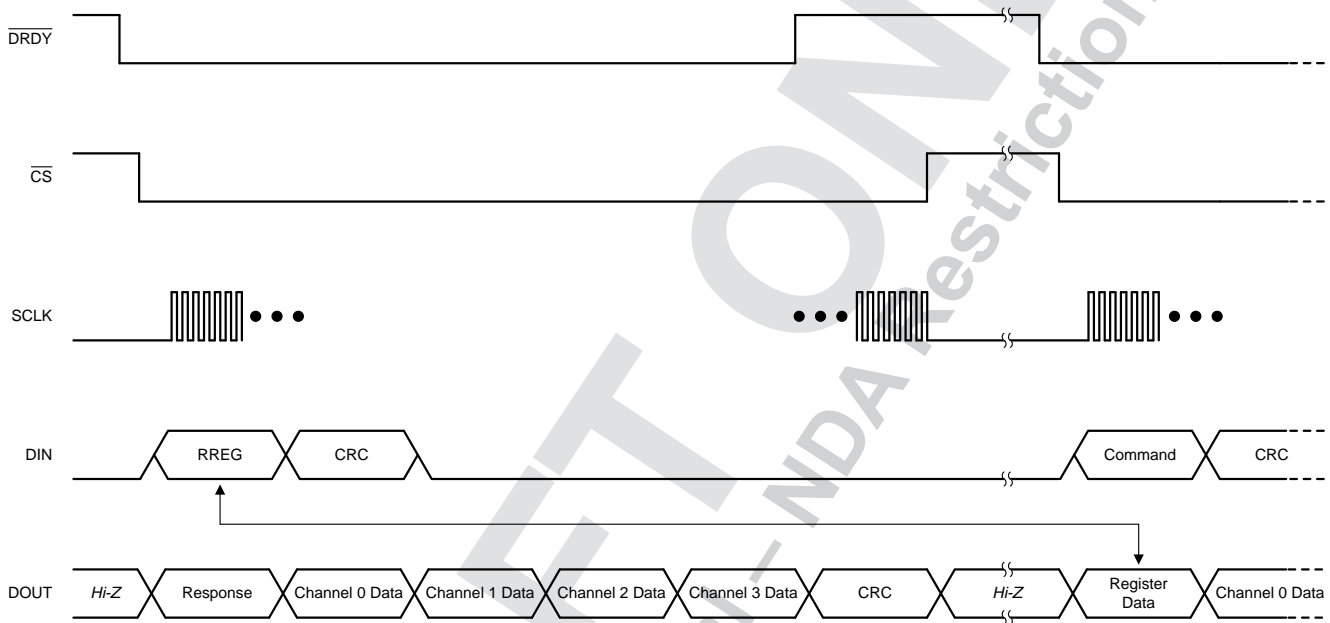
www.ti.com

7.5.1.10.3 RREG (101a aaaa annn nnnn)

The RREG command allows the reading of device registers. The binary format of the opcode is 101a aaaa annn nnnn, where a aaaa a is the binary address of the register to begin reading and nnn nnnn is the unsigned binary number of consecutive registers to read minus one. There are two cases for reading registers on the ADS131M04. When reading a single register (nnn nnnn = 000 0000b), the device outputs the register contents in the command response word of the following frame. If multiple registers are read using a single command (nnn nnnn > 000 0000b), the device forgoes outputting the ADC conversion data and instead outputs the requested register data sequentially in order of address.

7.5.1.10.3.1 Reading a Single Register

A single register is read from the device when nnn nnnn is specified as zero in the RREG opcode. Like all SPI commands on the ADS131M04, the response occurs on the output in the frame following the command. Instead of a unique acknowledgment word, the response word is the contents of the register whose address was specified in the opcode. [Figure 16](#) illustrates an example of reading a single register.

**Figure 16. Reading a Single Register****7.5.1.10.3.2 Reading Multiple Registers**

A single register is read from the device when nnn nnnn is specified as a number greater than zero in the RREG opcode. Like all SPI commands on the ADS131M04, the response occurs on the output in the frame following the command. Instead of a single acknowledgment word, the response spans multiple words in order to shift out all the requested registers. Continue toggling SCLK to accommodate the entire data stream. ADC conversion data is not output in the frame following a command to read multiple registers. [Figure 16](#) illustrates an example of reading multiple registers.

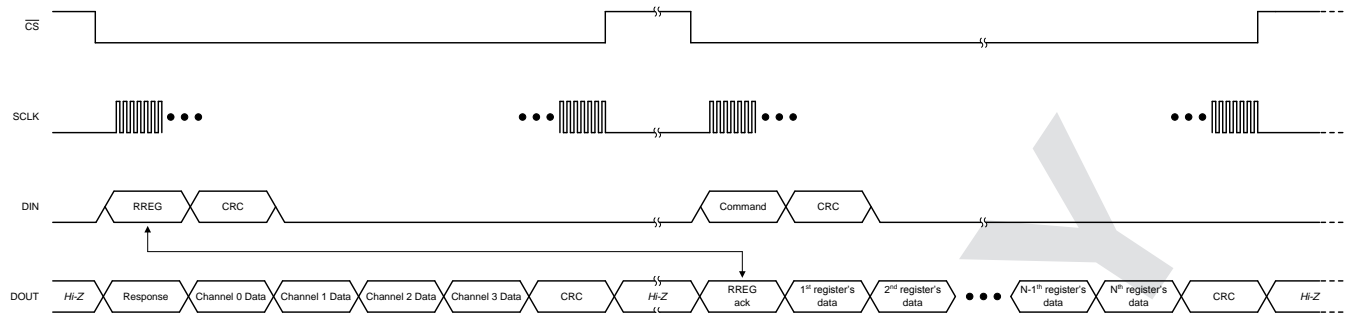


Figure 17. Reading Multiple Registers

7.5.1.10.4 WREG (011a aaaa annn nnnn)

The WREG command allows writing an arbitrary number of contiguous device registers. The binary format of the opcode is 011a aaaa annn nnnn, where a aaaa a is the binary address of the register to begin writing and nnn nnnn is the unsigned binary number of consecutive registers to write minus one. Insert the data to be written immediately following the command opcode. Write each register's intended contents into individual words, MSB aligned.

If the input CRC is enabled, write it at the end of the frame. The registers are written to the device as they are shifted into DIN. Therefore, a CRC error does not prevent an erroneous value from being written to a register. An input CRC error during a WREG command causes the CRC_ERR bit in the STATUS register to be set.

The device ignores writes to read-only registers or to out-of-bounds addresses. The response to the WREG command which occurs in the following frame appears as 010a aaaa ammm mmmm where mmm mmmm is the number of registers actually written minus one. This number can be checked by the host against nnn nnnn to ensure the expected number of registers were written.

Figure 18 illustrates a typical WREG sequence. In this example, the number of registers to write is larger than the number of ADC channels and therefore the frame is extended beyond the ADC channels and output CRC word. Extend the frame to complete shifting out ADC data output and output CRC when the host writes fewer registers than the number of ADC channels.

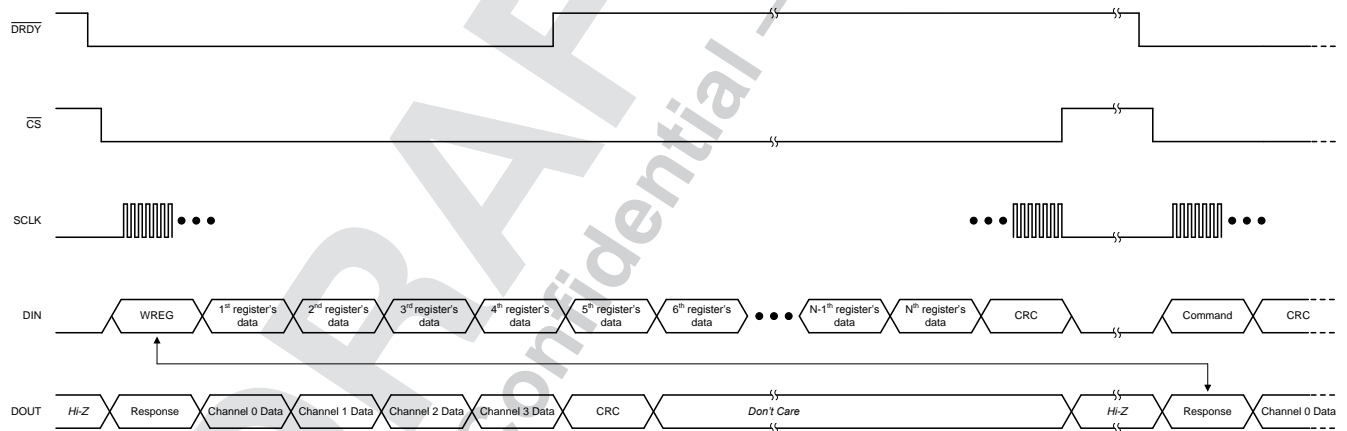


Figure 18. Writing Registers

7.5.1.10.5 STANDBY (0000 0000 0010 0010)

The STANDBY command places the device in a low power standby mode. The command is latched by the device at the end of the frame. The device enters standby mode immediately after the command is latched. Refer to the [Standby Mode](#) section for more information about standby mode. The command has no effect if the device is already in STANDBY mode.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.5.1.10.6 WAKEUP (0000 0000 0011 0011)**

The WAKEUP command returns the device to conversion mode from standby mode. The command has no effect if the device is already in conversion mode.

7.5.1.10.7 LOCK (0000 0101 0101 0101)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands which can change the state of the device. When the interface is locked, the device will only respond to the NULL, RREG, and UNLOCK commands. The device will continue to output conversion data during this time.

7.5.1.10.8 UNLOCK (0000 0110 0110 0110)

The UNLOCK command unlocks the interface which was locked by the LOCK command.

7.5.2 Synchronization

Synchronization can be performed by the host to ensure the ADC conversions are synchronized to an external event. For example, it can realign the data capture to the expected timing of the host if a glitch on the clock causes the host and device to become out of synchronization. Synchronization is not available in global chop mode.

Provide a negative pulse on the $\overline{\text{SYNC/RESET}}$ pin whose width is less than t_{SRLRST} but greater than a CLKIN period to use the synchronization feature. The device internally compares the leading negative edge of the pulse to its internal clock which tracks the data rate. The internal data rate clock has timing equivalent to the $\overline{\text{DRDY}}$ pin if it were configured to assert with a phase calibration setting of 0b. If the negative edge on $\overline{\text{SYNC/RESET}}$ aligns with the internal data rate clock, the device is determined to be synchronized and therefore no action is taken. If there is misalignment, the digital filters on the device reset to be synchronized with the pulse.

The phase calibration settings on all channels are retained during synchronization. This means channels with non-zero phase calibration settings generate conversion results less than a data rate period after the synchronization event occurs. However, the results may be corrupted and are not settled until the respective channels have had at least three conversion cycles for the sinc³ filter to settle.

7.6 Registers

Table 7 lists the memory-mapped registers for the ADS131M04 registers. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. ADS131M04 Registers

Address	Acronym	Register Name	Section
0h	ID	ID Register	ID Register (Address = 0h) [reset = 2400h]
1h	STATUS	Status Register	STATUS Register (Address = 1h) [reset = 500h]
2h	MODE	Mode Register	MODE Register (Address = 2h) [reset = 510h]
3h	CLOCK	Clock Register	CLOCK Register (Address = 3h) [reset = F0Eh]
4h	GAIN1	Gain Register	GAIN1 Register (Address = 4h) [reset = 0h]
6h	CFG	Configuration Register	CFG Register (Address = 6h) [reset = 600h]
7h	THRSHLD_MSB	Threshold MSB Register	THRSHLD_MSB Register (Address = 7h) [reset = 0h]
8h	THRSHLD_LSB	Threshold LSB Register	THRSHLD_LSB Register (Address = 8h) [reset = 0h]
9h	CH0_CFG	Channel 0 Configuration Register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
Ah	CH0_OCAL_MSB	Channel 0 Offset Calibration MSB Register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
Bh	CH0_OCAL_LSB	Channel 0 Offset Calibration LSB Register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
Ch	CH0_GCAL_MSB	Channel 0 Gain Calibration MSB Register	CHn_GCAL_MSB Register (Address = Ch, 11h, 15h, 1Bh) [reset = 0h]
Dh	CH0_GCAL_LSB	Channel 0 Gain Calibration LSB Register	CHn_GCAL_LSB Register (Address = Dh, 12h, 16h, 1Ch) [reset = 0h]
Eh	CH1_CFG	Channel 1 Configuration Register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
Fh	CH1_OCAL_MSB	Channel 1 Offset Calibration MSB Register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
10h	CH1_OCAL_LSB	Channel 1 Offset Calibration LSB Register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]

PRODUCT PREVIEW

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Table 7. ADS131M04 Registers (continued)**

Address	Acronym	Register Name	Section
11h	CH1_GCAL_MSB	Channel 1 Gain Calibration MSB Register	CHn_GCAL_MSB Register (Address = Ch, 11h, 15h, 1Bh) [reset = 0h]
12h	CH1_GCAL_LSB	Channel 1 Gain Calibration LSB Register	CHn_GCAL_LSB Register (Address = Dh, 12h, 16h, 1Ch) [reset = 0h]
13h	CH2_CFG	Channel 2 Configuration Register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
14h	CH2_OCAL_MSB	Channel 2 Offset Calibration MSB Register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
15h	CH2_OCAL_LSB	Channel 2 Offset Calibration LSB Register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
16h	CH2_GCAL_MSB	Channel 2 Gain Calibration MSB Register	CHn_GCAL_MSB Register (Address = Ch, 11h, 15h, 1Bh) [reset = 0h]
17h	CH2_GCAL_LSB	Channel 2 Gain Calibration LSB Register	CHn_GCAL_LSB Register (Address = Dh, 12h, 16h, 1Ch) [reset = 0h]
18h	CH3_CFG	Channel 3 Configuration Register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
19h	CH3_OCAL_MSB	Channel 3 Offset Calibration MSB Register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
1Ah	CH3_OCAL_LSB	Channel 3 Offset Calibration LSB Register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
1Bh	CH3_GCAL_MSB	Channel 3 Gain Calibration MSB Register	CHn_GCAL_MSB Register (Address = Ch, 11h, 15h, 1Bh) [reset = 0h]
1Ch	CH3_GCAL_LSB	Channel 3 Gain Calibration LSB Register	CHn_GCAL_LSB Register (Address = Dh, 12h, 16h, 1Ch) [reset = 0h]
3Eh	REGMAP_CRC	Register Map CRC Register	REGMAP_CRC Register (Address = 3Eh) [reset = 0h]
3Fh	RESERVED	Reserved Register	RESERVED Register (Address = 3Fh) [reset = 0h]

Complex bit access types are encoded to fit into small table cells. [Table 8](#) shows the codes that are used for access types in this section.

Table 8. ADS131M04 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
n		When this variable is used in a register name, an offset, or an address, it refers to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.1 ID Register (Address = 0h) [reset = 2400h]**ID is shown in [Figure 19](#) and described in [Table 9](#).Return to [Summary Table](#).**Figure 19. ID Register**

15	14	13	12	11	10	9	8
RESERVED			RESERVED	CHANCNT			
R-1h			R-0h	R-4h			
7	6	5	4	3	2	1	0
REVID							
R-0h							

Table 9. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	1h	Reserved
12	RESERVED	R	0h	Reserved
11:8	CHANCNT	R	4h	Channel Count, always read 4h
7:0	REVID	R	0h	Revision ID, always read 00h

7.6.2 STATUS Register (Address = 1h) [reset = 500h]

STATUS is shown in [Figure 20](#) and described in [Table 10](#).

Return to [Summary Table](#).

Figure 20. STATUS Register

15	14	13	12	11	10	9	8
LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH	
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	DRDY3	DRDY2	DRDY1	DRDY0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-0h

Table 10. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOCK	R	0h	SPI interface lock indicator 0b = Unlocked (reset) 1b = Locked
14	F_RESYNC	R	0h	ADC resynchronization fault indicator 0b = No fault (reset) 1b = Fault occurred
13	REG_MAP	R	0h	Register map CRC fault 0b = No change in the register map CRC (reset) 1b = Register map CRC changed
12	CRC_ERR	R	0h	SPI input CRC error indicator 0b = No CRC error (reset) 1b = Input CRC error occurred
11	CRC_TYPE	R	0h	CRC type 0b = 16-bit CCITT (reset) 1b = 16-bit ANSI
10	RESET	R	1h	Reset status 0b = No reset 1b = Reset occurred (reset)
9:8	WLENGTH	R	1h	Data word length 0b = 16 bits 1b = 24 bits (reset) 10b = 32 bits - LSB zero padding 11b = 32 bits - MSB sign extension
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	DRDY3	R	0h	ADC data from channel 3 available indicator 0b = No new data available 1b = New data is available
2	DRDY2	R	0h	ADC data from channel 2 available indicator 0b = No new data available 1b = New data is available

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Table 10. STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
1	DRDY1	R	1h	ADC data from channel 1 available indicator 0b = No new data available 1b = New data is available
0	DRDY0	R	0h	ADC data from channel 0 available indicator 0b = No new data available 1b = New data is available

DRAFT ONLY
 TI Confidential – NDA Restrictions

PRODUCT PREVIEW

7.6.3 MODE Register (Address = 2h) [reset = 510h]

MODE is shown in Figure 21 and described in Table 11.

Return to [Summary Table](#).

Figure 21. MODE Register

15	14	13	12	11	10	9	8
RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET		WLENGTH
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-1h
7	6	5	4	3	2	1	0
RESERVED	RESERVED		TIMEOUT		DRDY_SEL	DRDY_HiZ	DRDY_FMT
R/W-0h		R/W-0h	R/W-1h		R/W-0h	R/W-1h	R/W-1h

Table 11. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	0h	Reserved
13	REG_CRC_EN	R/W	0h	Register Map CRC enable 0b = Register map CRC disabled (default) 1b = Register map CRC enabled
12	RX_CRC_EN	R/W	0h	SPI input CRC enable 0b = Disabled (default) 1b = Enabled
11	CRC_TYPE	R/W	0h	SPI input and output, register map CRC type 0b = 16 bit CCITT (default) 1b = 16 bit ANSI
10	RESET	R/W	1h	Reset 0b = No reset 1b = Reset occurred (reset)
9:8	WLENGTH	R/W	1h	Data word length 0b = 16 bits 1b = 24 bits (reset) 10b = 32 bits - LSB zero padding 11b = 32 bits - MSB sign extension
7:6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	TIMEOUT	R/W	1h	SPI Timeout enable 0b = Disabled 1b = Enabled (default)
3:2	DRDY_SEL	R/W	0h	DRDY pin signal source selection 0b = Most lagging enabled channel (default) 1b = Logic OR of all the enabled channels 10b = Most leading enabled channel 11b = Most leading enabled channel
1	DRDY_HiZ	R/W	1h	DRDY pin state when conversion data is not available 0b = Logic high (default) 1b = High impedance
0	DRDY_FMT	R/W	1h	DRDY signal format when conversion data is available 0b = Logic low (default) 1b = Negative pulse with a fixed width

PRODUCT PREVIEW

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.4 CLOCK Register (Address = 3h) [reset = F0Eh]**CLOCK is shown in [Figure 22](#) and described in [Table 12](#).Return to [Summary Table](#).**Figure 22. CLOCK Register**

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	OSR			PWR	
R/W-0h	R/W-0h	R/W-0h	R/W-3h			R/W-2h	

Table 12. CLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	CH3_EN	R/W	0h	Enable channel 3 ADC 0b = Disabled 1b = Enabled (default)
10	CH2_EN	R/W	0h	Enable channel 2 ADC 0b = Disabled 1b = Enabled (default)
9	CH1_EN	R/W	0h	Enable channel 1 ADC 0b = Disabled 1b = Enabled (default)
8	CH0_EN	R/W	0h	Enable channel 0 ADC 0b = Disabled 1b = Enabled (default)
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4:2	OSR	R/W	3h	The oversampling ratio of the modulator for a 4 and 8 ch silicon 0b = 128 1b = 256 10b = 512 11b = 1024 (default) 100b = 2048 101b = 4096 110b = 8192 111b = 16256
1:0	PWR	R/W	2h	Power mode 0b = Very Low-Power 1b = Low-Power 10b = High-Resolution (default) 11b = High-Resolution

7.6.5 GAIN1 Register (Address = 4h) [reset = 0h]

GAIN1 is shown in [Figure 23](#) and described in [Table 13](#).

Return to [Summary Table](#).

Figure 23. GAIN1 Register

15	14	13	12	11	10	9	8
RESERVED	PGAGAIN3			RESERVED	PGAGAIN2		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PGAGAIN1			RESERVED	PGAGAIN0		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 13. GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14:12	PGAGAIN3	R/W	0h	PGA gain for channel 3 0b = Gain of 1 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
11	RESERVED	R/W	0h	Reserved
10:8	PGAGAIN2	R/W	0h	PGA gain for channel 2 0b = Gain of 1 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
7	RESERVED	R/W	0h	Reserved
6:4	PGAGAIN1	R/W	0h	PGA gain for channel 1 0b = Gain of 1 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
3	RESERVED	R/W	0h	Reserved

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Table 13. GAIN1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
2:0	PGAGAIN0	R/W	0h	PGA gain for channel 0 0b = Gain of 1 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128

DRAFT ONLY
 TI Confidential – NDA Restrictions

PRODUCT PREVIEW

7.6.6 CFG Register (Address = 6h) [reset = 600h]

CFG is shown in [Figure 24](#) and described in [Table 14](#).

Return to [Summary Table](#).

Figure 24. CFG Register

15	14	13	12	11	10	9	8
RESERVED			GC_DLY			GC_EN	
R/W-0h			R/W-3h			R/W-0h	
7	6	5	4	3	2	1	0
CD_ALLCH	CD_NUM			CD_LEN			CD_EN
R/W-0h	R/W-0h			R/W-0h			R/W-0h

Table 14. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	0h	Reserved
12:9	GC_DLY	R/W	3h	Global chop delay in modulator clock periods before measurement begins 0b = 2 1b = 4 10b = 8 11b = 16 (default) 100b = 32 101b = 64 110b = 128 111b = 256 1000b = 512 1001b = 1024 1010b = 2048 1011b = 4096 1100b = 8192 1101b = 16484 1110b = 32768 1111b = 65536
8	GC_EN	R/W	0h	Global chop enable 0b = Disabled (default) 1b = Enabled
7	CD_ALLCH	R/W	0h	Current detect channels required to trigger detect 0b = Any channel (default) 1b = All channels
6:4	CD_NUM	R/W	0h	Current detect number of threshold exceeds to trigger detect 0b = 1 (default) 1b = 2 10b = 4 11b = 8 100b = 16 101b = 32 110b = 64 111b = 128

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**Table 14. CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3:1	CD_LEN	R/W	0h	Current detect measurement length in conversion periods 0b = 128 (default) 1b = 256 10b = 512 11b = 768 100b = 1280 101b = 1792 110b = 2560 111b = 3584
0	CD_EN	R/W	0h	Current detect mode enable 0b = Disabled (default) 1b = Enabled

PRODUCT PREVIEW

7.6.7 THRSHLD_MSB Register (Address = 7h) [reset = 0h]

THRSHLD_MSB is shown in [Figure 25](#) and described in [Table 15](#).

Return to [Summary Table](#).

Figure 25. THRSHLD_MSB Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD_TH_MSB															
R/W-0h															

Table 15. THRSHLD_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CD_TH_MSB	R/W	0h	Current Detect mode threshold MSB

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.8 THRSHLD_LSB Register (Address = 8h) [reset = 0h]**THRSHLD_LSB is shown in [Figure 26](#) and described in [Table 16](#).Return to [Summary Table](#).**Figure 26. THRSHLD_LSB Register**

15	14	13	12	11	10	9	8
CD_TH_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 16. THRSHLD_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CD_TH_LSB	R/W	0h	Current Detect mode threshold LSB
7:0	RESERVED	R	0h	Reserved

7.6.9 CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]

CHn_CFG is shown in [Figure 27](#) and described in [Table 17](#).

Return to [Summary Table](#).

Figure 27. CHn_CFG Register

15	14	13	12	11	10	9	8
PHASEn							
R/W-0h							
7	6	5	4	3	2	1	0
PHASEn		RESERVED				MUXn	
R/W-0h		R-0h				R/W-0h	

Table 17. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASEn	R/W	0h	Channel n Phase Delay
5:2	RESERVED	R	0h	Reserved
1:0	MUXn	R/W	0h	Channel n Input Select 0b = AINnP and AINnN (default) 1b = ADC inputs shorted 10b = DC diagnostic signal 11b = AC diagnostic signal

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.10 CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]**CHn_OCAL_MSB is shown in [Figure 28](#) and described in [Table 18](#).Return to [Summary Table](#).**Figure 28. CHn_OCAL_MSB Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCALn_MSB															
R/W-0h															

Table 18. CH0_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCALn_MSB	R/W	0h	Channel n Offset Calibration register bits [23:8]

7.6.11 CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]

CHn_OCAL_LSB is shown in [Figure 29](#) and described in [Table 19](#).

Return to [Summary Table](#).

Figure 29. CHn_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCALn_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 19. CHn_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCALn_LSB	R/W	0h	Channel n Offset Calibration register bits [7:0]
7:0	RESERVED	R	0h	Reserved

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.12 CHn_GCAL_MSB Register (Address = Ch, 11h, 15h, 1Bh) [reset = 0h]**CHn_GCAL_MSB is shown in [Figure 30](#) and described in [Table 20](#).Return to [Summary Table](#).**Figure 30. CHn_GCAL_MSB Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GCALn_MSB															
R/W-0h															

Table 20. CHn_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCALn_MSB	R/W	0h	Channel n Gain Calibration register bits [23:8]

7.6.13 CHn_GCAL_LSB Register (Address = Dh, 12h, 16h, 1Ch) [reset = 0h]

CHn_GCAL_LSB is shown in [Figure 31](#) and described in [Table 21](#).

Return to [Summary Table](#).

Figure 31. CHn_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCALn_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 21. CH0_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCALn_LSB	R/W	0h	Channel n Gain Calibration register bits [7:0]
7:0	RESERVED	R	0h	Reserved

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**7.6.14 REGMAP_CRC Register (Address = 3Eh) [reset = 0h]**REGMAP_CRC is shown in [Figure 32](#) and described in [Table 22](#).Return to [Summary Table](#).**Figure 32. REGMAP_CRC Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_CRC															
R-0h															

Table 22. REGMAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_CRC	R	0h	Register map CRC

7.6.15 RESERVED Register (Address = 3Fh) [reset = 0h]

RESERVED is shown in [Figure 33](#) and described in [Table 23](#).

Return to [Summary Table](#).

Figure 33. RESERVED Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0h															

Table 23. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0h	Reserved

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

E2E is a trademark of Texas Instruments.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Package Option Addendum

9.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
ADS131M04	PREVIEW	WQFN	RUK	20						
ADS131M04	PREVIEW	TSSOP	PW	20						

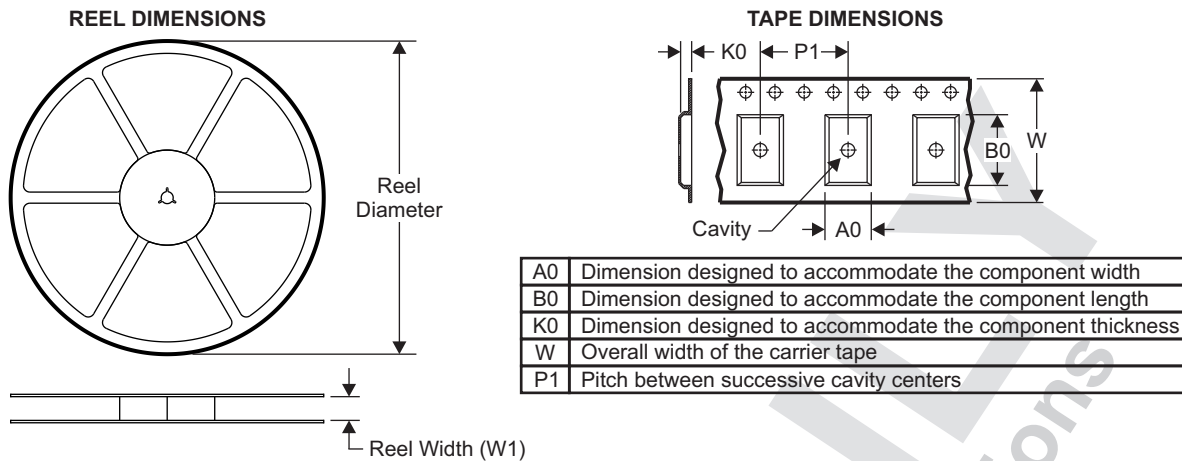
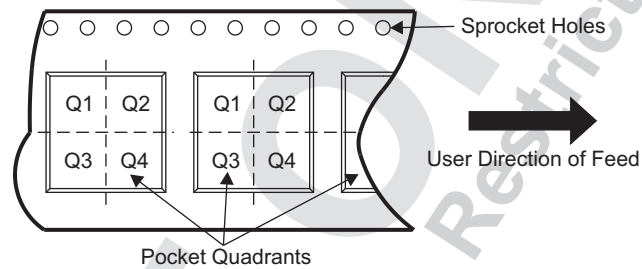
- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

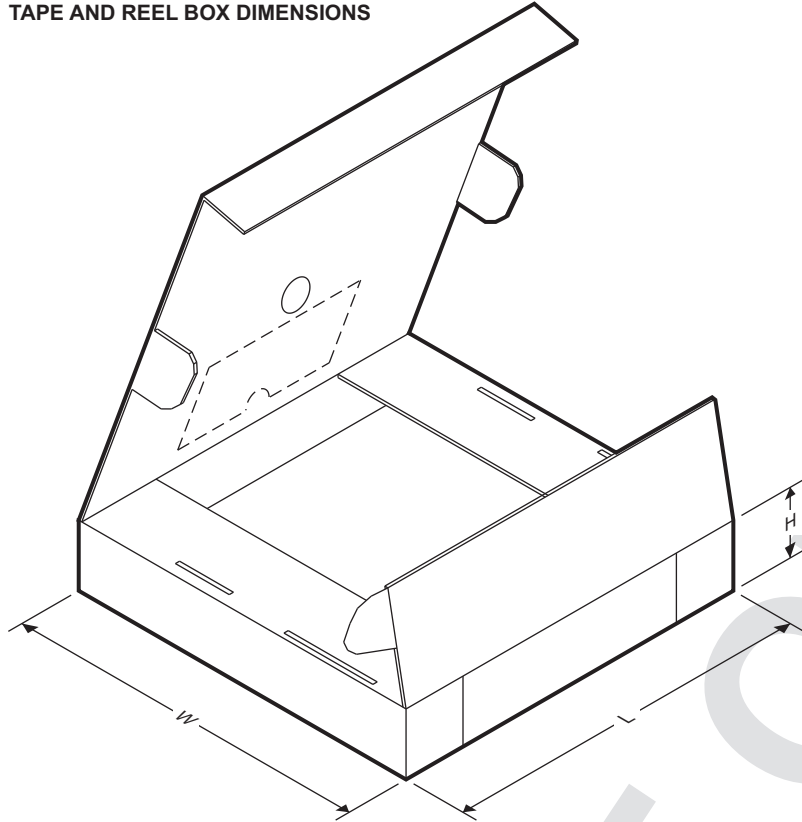
ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**9.1.2 Tape and Reel Information****QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS131M04	WQFN	RUK	20									
ADS131M04	TSSOP	PW	20									

TAPE AND REEL BOX DIMENSIONS



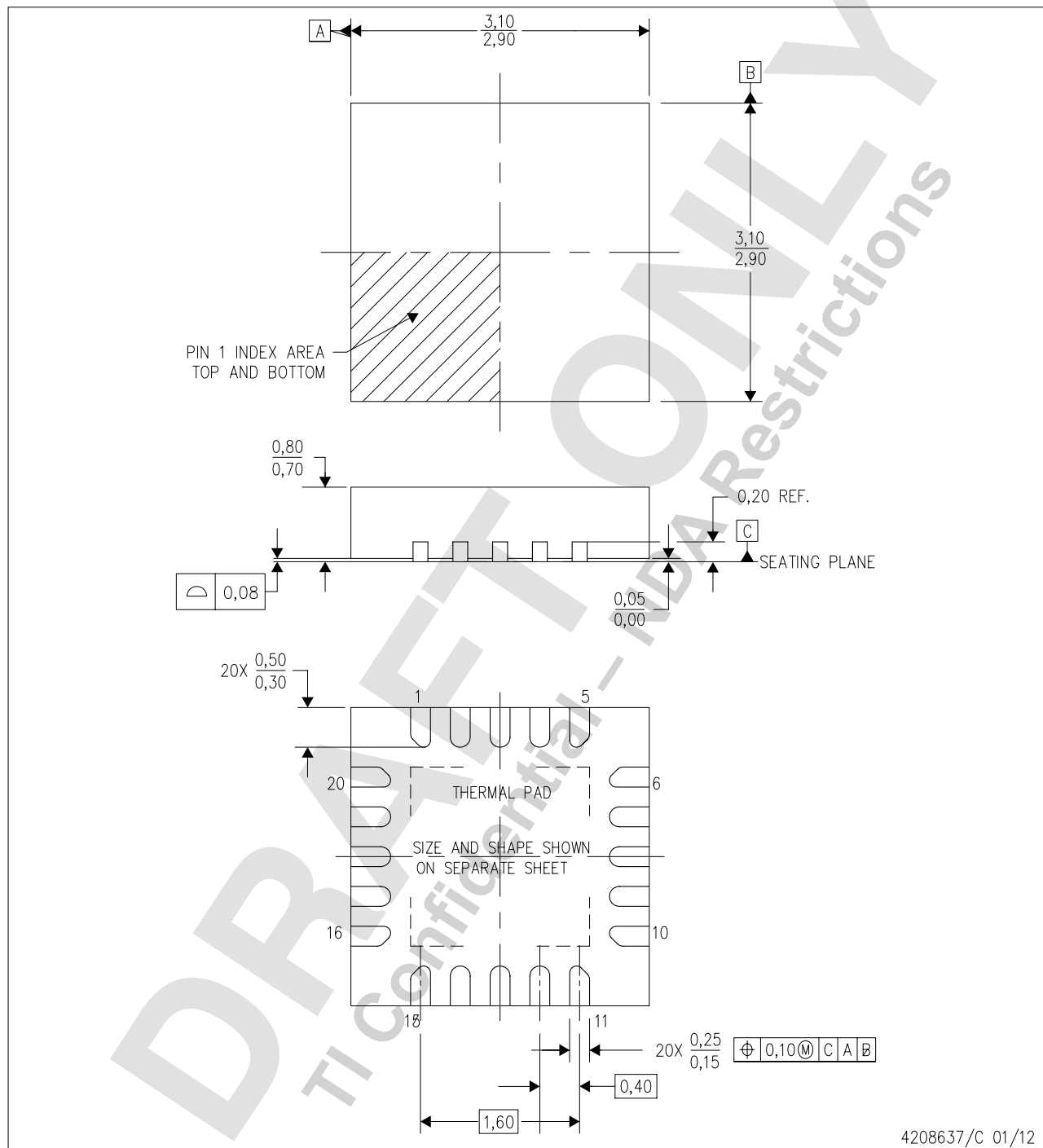
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS131M04	WQFN	RUK	20				
ADS131M04	TSSOP	PW	20				

PRODUCT PREVIEW

MECHANICAL DATA

RUK (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

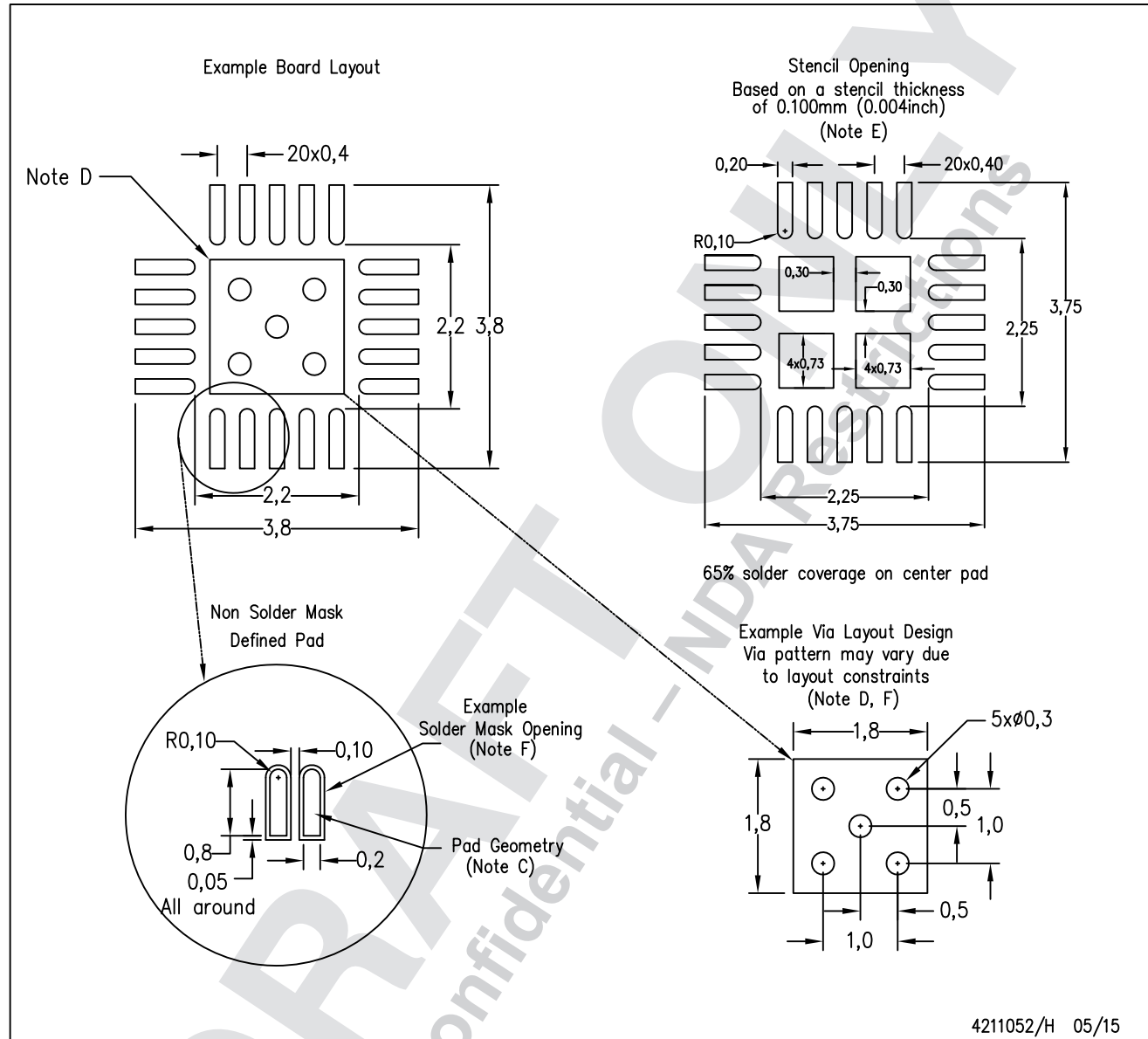


- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

LAND PATTERN DATA

RUK (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



PRODUCT PREVIEW

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

ADS131M04

SBAS890 – SEPTEMBER 2018

www.ti.com**THERMAL PAD MECHANICAL DATA**

RUK (S–PWQFN–N20)

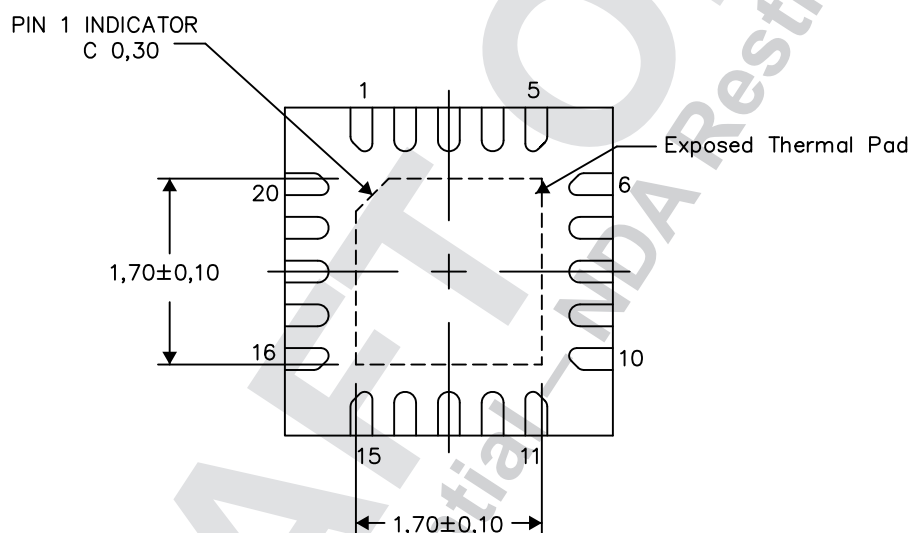
PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4209762/1 05/15

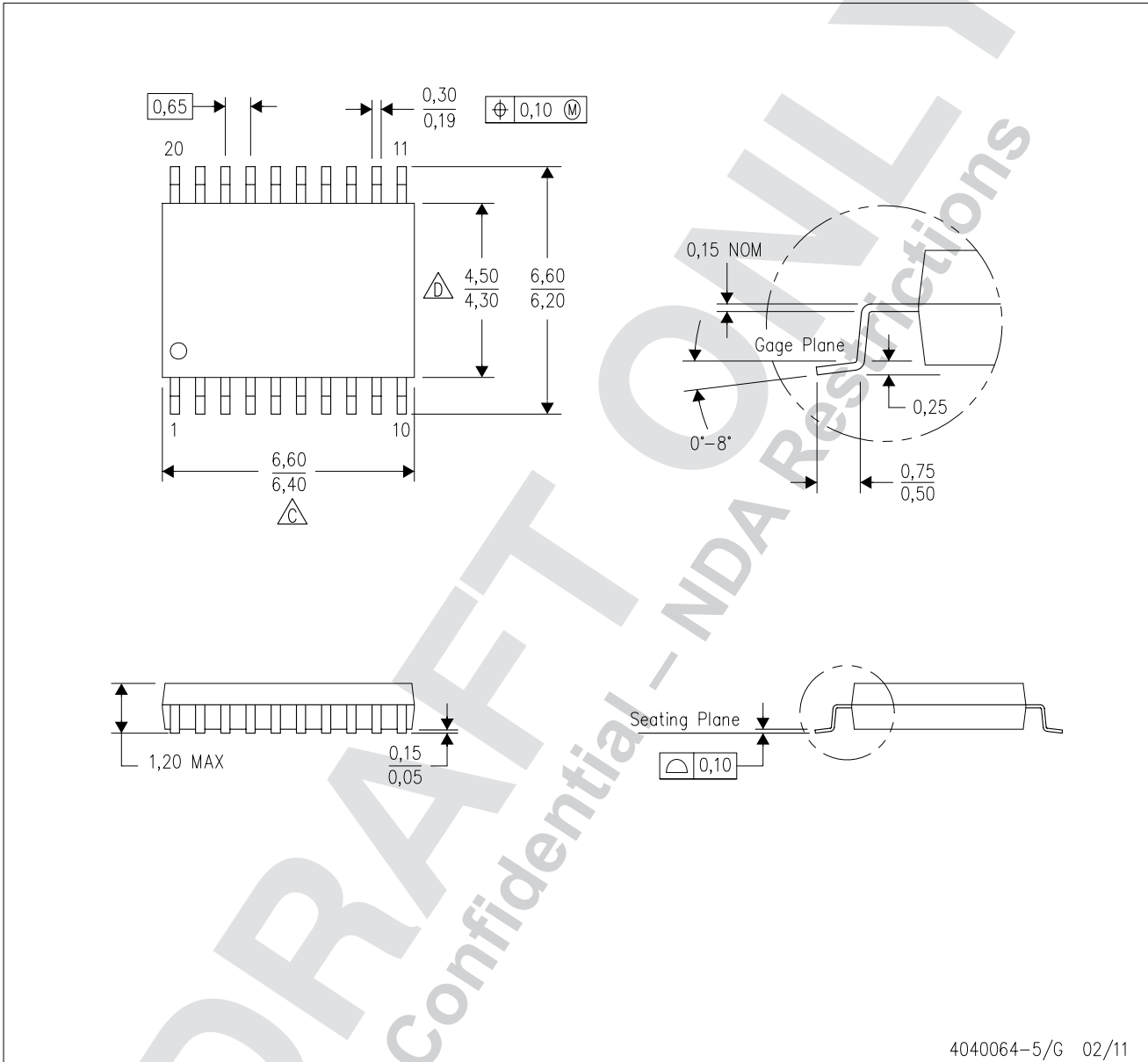
NOTE: All linear dimensions are in millimeters

PRODUCT PREVIEW

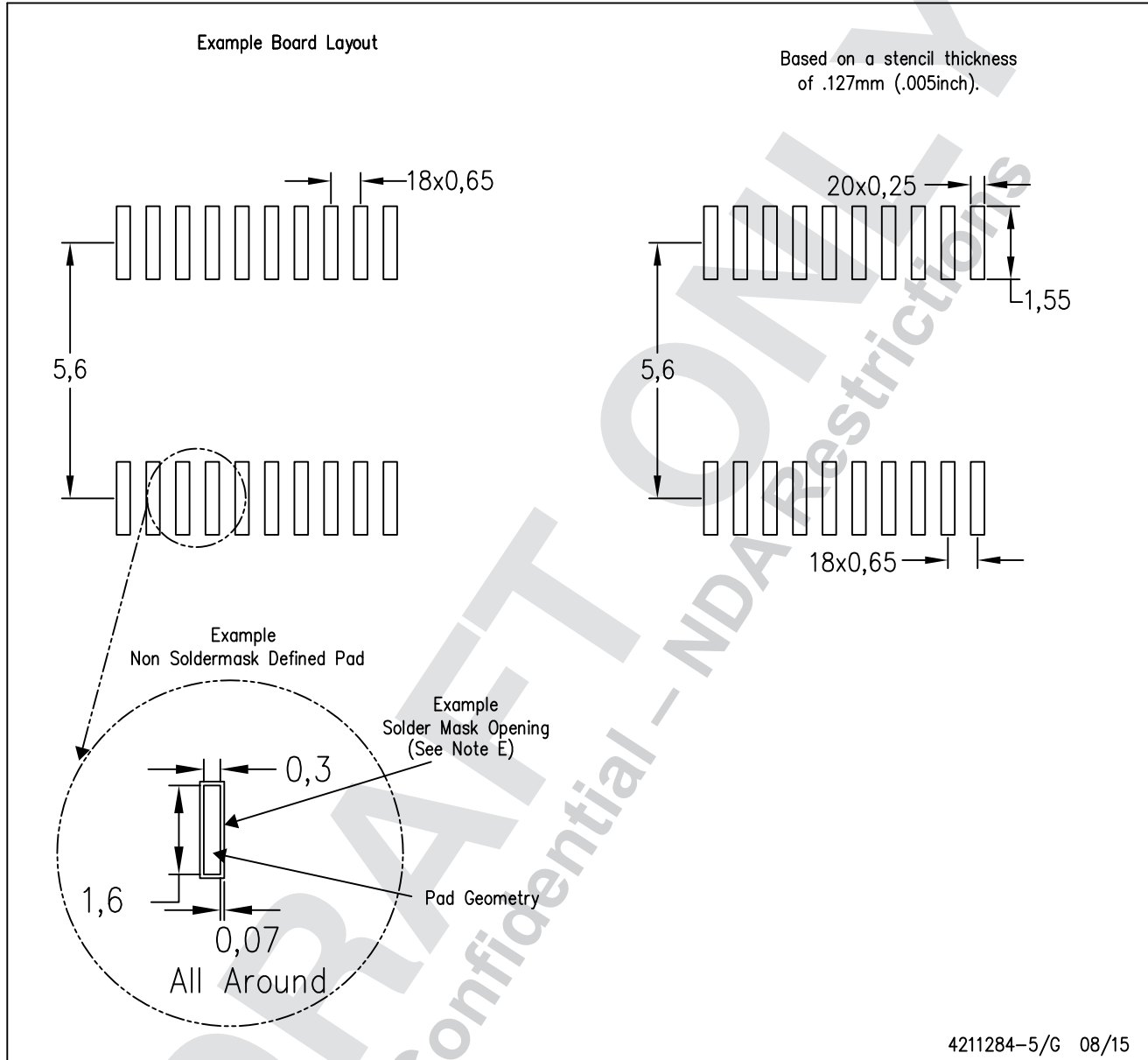
MECHANICAL DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



PRODUCT PREVIEW

LAND PATTERN DATA**PW (R-PDSO-G20)****PLASTIC SMALL OUTLINE****NOTES:**

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated