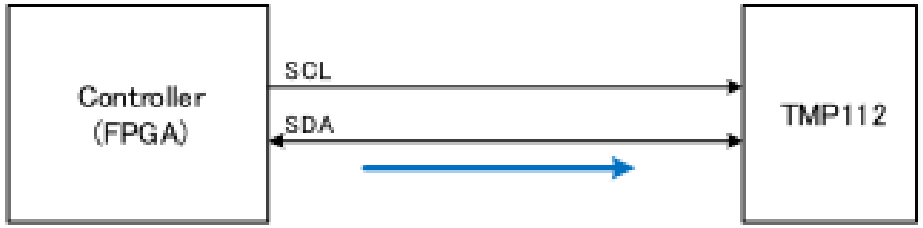
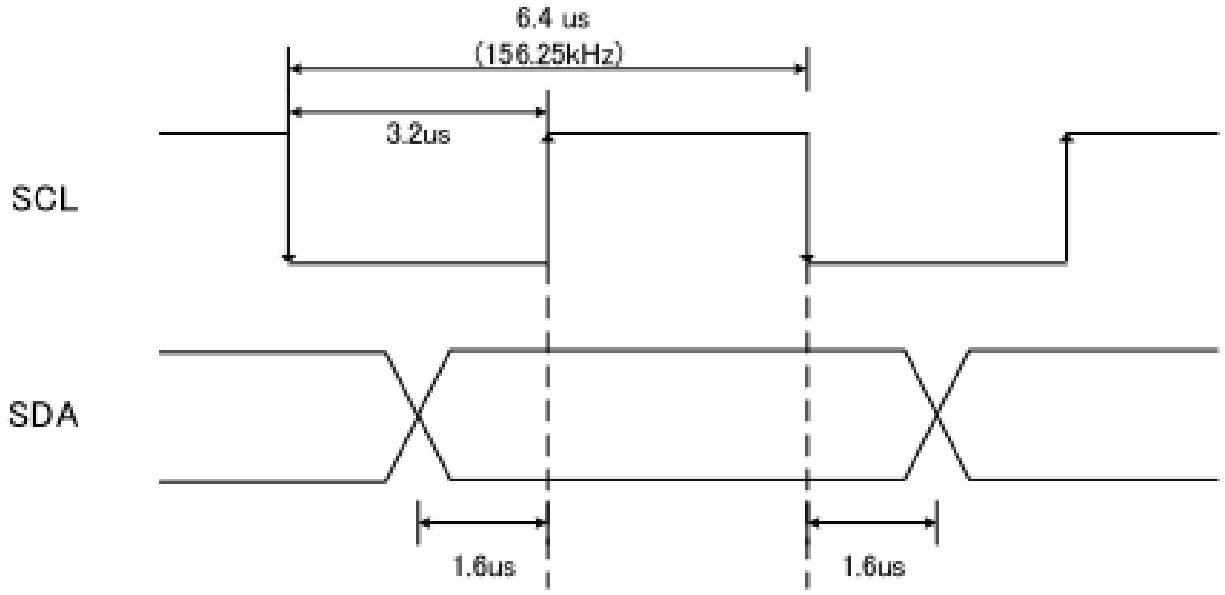
TMP112 WRITE



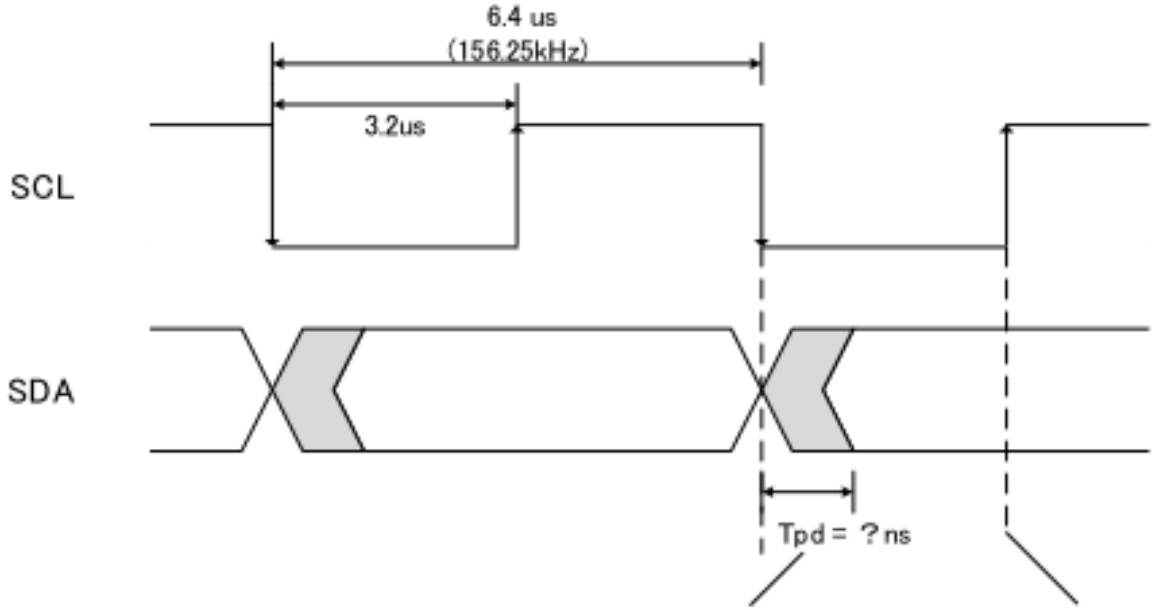
I2C Timing at TMP112



Pattern delay is not described due to very small

■ TMP112 READ

I2C Timing at FPGA



SDA output trigger is
SCL falling edge.

FPGA Data Capture Timing