TSM12

12-Channel Self Calibration Capacitive Touch Sensor

SPECIFICATION V1.0

1 Specification

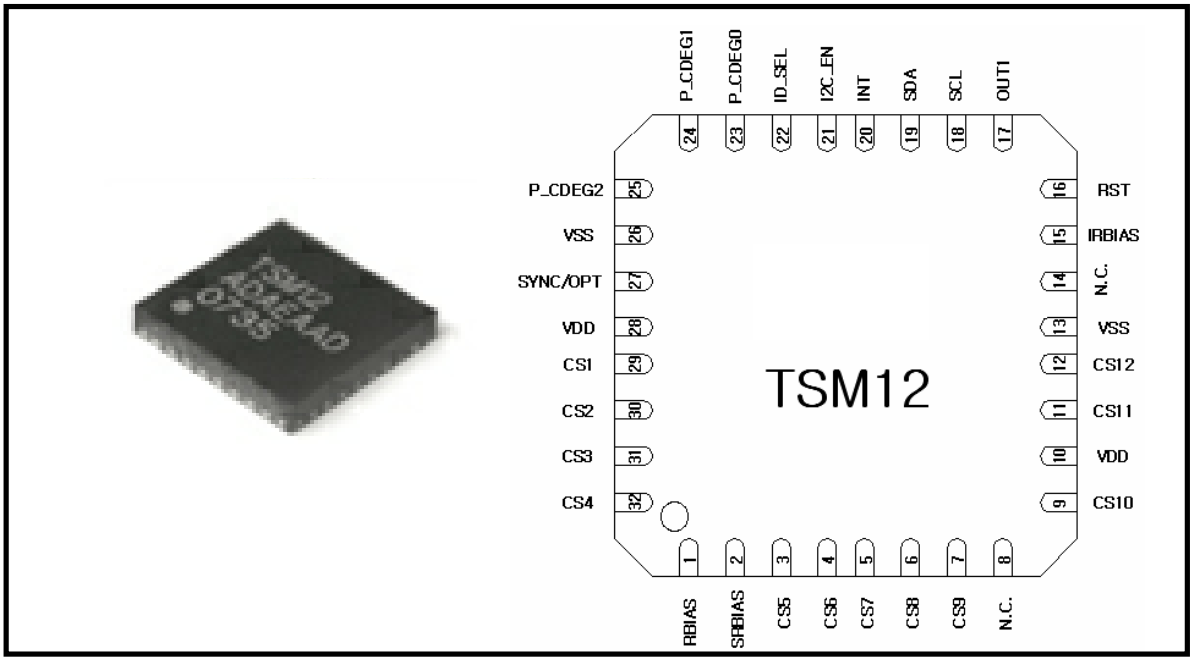
1.1 General Feature

- 12-Channel capacitive sensor with auto sensitivity calibration
- Selectable output operation (single mode / multi-mode)
- Independently adjustable in 8 step sensitivity
- Sync function for multi chip application
- Touch intensity can be detectable within 3 steps (Low, Middle and High)
- Adjustable internal frequency with external resister
- Adjustable response time and interrupt level by the control registers
- I2C serial interface
- Embedded high frequency noise elimination circuit
- IDLE mode to save the consumption
- Embedded power key function on channel 1 for mobile phone application
- RoHS compliant 32QFN package

1.2 Application

- Mobile application (mobile phone / PDA / PMP etc)
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application
- Touch screen replacement application

1.3 Package (32QFN)



TSM12 32QFN (Drawings not to scale)

2 Pin Description (32QFN)

PIN No.	Name	I/O	Description	Protection
1	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
2	SRBIAS	Analog Input	IDLE Mode Internal bias adjust input	VDD/GND
3	CS5	Analog Input	CH5 capacitive sensor input	VDD/GND
4	CS6	Analog Input	CH6 capacitive sensor input	VDD/GND
5	CS7	Analog Input	CH7 capacitive sensor input	VDD/GND
6	CS8	Analog Input	CH8 capacitive sensor input	VDD/GND
7	CS9	Analog Input	CH9 capacitive sensor input	VDD/GND
8	N.C.	–	No Connection	–
9	CS10	Analog Input	CH10 capacitive sensor input	VDD/GND
10	VDD	Digital Input	–	VDD/GND
11	CS11	Analog Input	CH11 capacitive sensor input	VDD/GND
12	CS12	Analog Input	CH12 capacitive sensor input	VDD/GND
13	VSS	Ground	Supply ground	VDD
14	NC	–	No Connection	–
15	IRBIAS	Analog Input	Internal I2C clk frequency adjust input	VDD/GND
16	RST	Digital Input	System reset (High reset)	VDD/GND
17	OUT1	Digital Output	CH1 output (Open drain)	VDD/GND
18	SCL	Digital Input	I2C clock input	VDD/GND
19	SDA	Digital Input/Output	I2C data (Open drain)	VDD/GND
20	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
21	I2C_EN	Digital Input	I2C enable(Low enable)	VDD/GND
22	ID_SEL	Digital Input	I2C address selection	VDD/GND
23	P_CDEG0	Digital Input	Ch1 sensitivity selection bit0	VDD/GND
24	P_CDEG1	Digital Input	Ch1 sensitivity selection bit1	VDD/GND
25	P_CDEG2	Digital Input	Ch1 sensitivity selection bit2	VDD/GND
26	VSS	Digital Input	–	VDD/GND
27	SYNC/OPT	Digital Input/Output	Output mode selection (Single Output / Multi Output Note 1) Sync pulse input /output	VDD/GND
28	VDD	Power	Power (2.5V~5.0V)	GND
29	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
30	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
31	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
32	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND

Note 1 : Refer to 6.3 SYNC/OPT implementation

3 Absolute Maximum Rating

Battery supply voltage	5.0V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	2000V	VDD
		2000V	VSS
		2000V	P to P
M.M	Pos / Neg	200V	VDD
		200V	VSS
		200V	P to P
C.D.M	Pos / Neg	500V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Max	Test Step
I Test	Positive	200mA	25mA
	Negative	−200mA	
V supply over 5.0V	Positive	8.0V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.3V, Rb=510k, Sync Mode (Rsync = 2MΩ) (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.0	V
Current consumption Note1	I_{DD}	V_{DD}= 3.3V R_B=510k R_SB=0	–	80	130	μA
		V_{DD}= 5.0V R_B=510k R_SB=0	–	200	315	
		V_{DD}= 3.3V R_B=510k R_SB=3M	–	7	–	
		V_{DD}= 5.0V R_B=510k R_SB=3M	–	15	–	
	I_{DD_I2C}	V_{DD}= 3.3V R_B=510k R_{I2C} =20k	–	1.5	–	mA
		V_{DD}= 5.0V R_B=510k R_{I2C} =30k	–	2.3	–	
		IDD_I2C Disable	–	–	1	μA
Output maximum sink current	I_{OUT}	T_A = 25℃	–	–	4.0	mA
Sense input capacitance range Note2	C_S		–	10	100	pF
Sense input resistance range	R_S		–	200	1000	Ω
Minimum detective capacitance difference	ΔC	Cs = 10pF, C_{DEG} = 200pF (I2C default sensitivity select)	0.2	–	–	pF
Output impedance (open drain)	Zo	ΔC > 0.2pF, Cs = 10pF, (I2C default sensitivity select)	–	12	–	Ω
		ΔC < 0.2pF, Cs = 10pF, (I2C default sensitivity select)	–	30M	–	
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.3V R_B = 510k	–	100	–	ms
		V_{DD} = 5.0V R_B = 510k	–	80	–	
Recommended bias resistance range Note3	R_B	V_{DD} = 3.3V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
Maximum bias capacitance	C_{B_MAX}		–	820	1000	pF
Recommended sync resistance range	R_{SYNC}		1	2	20	MΩ

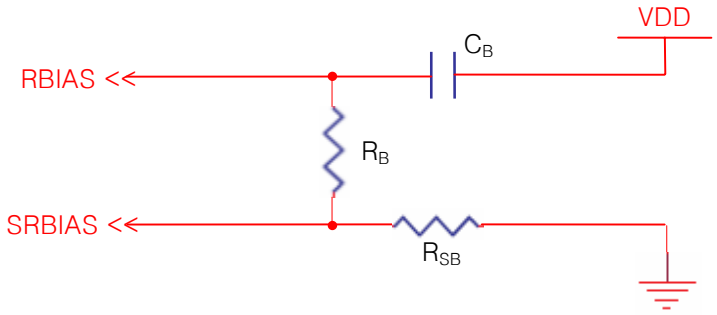
Note 1 : In case of SCL frequency is 500kHz.

Note 2 : The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

Note 3 : The lower R_B is recommended in noisy condition.

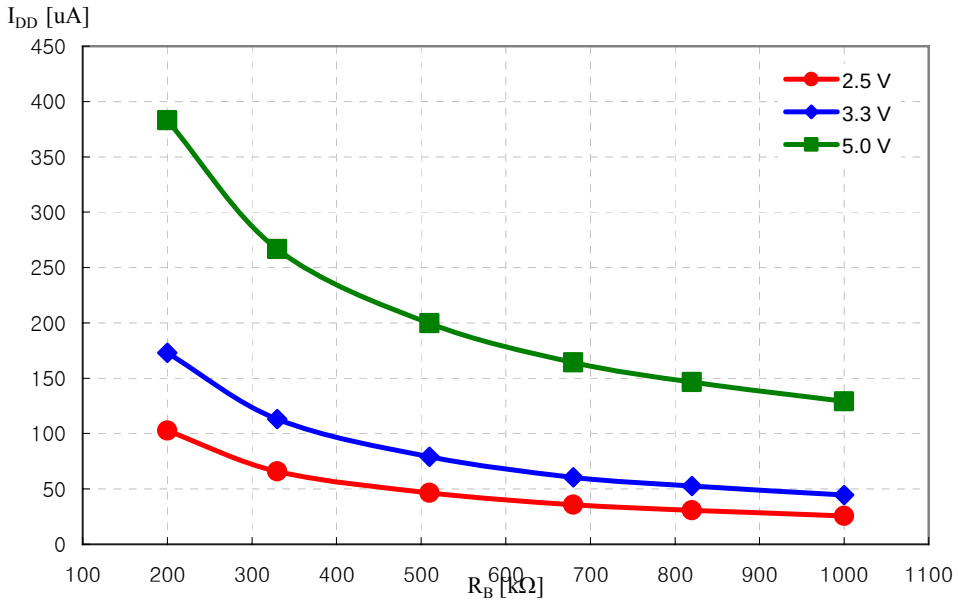
6 Implementation of TSM12

6.1 RBIAS & SRBIAS implementation



The RBIAS is connecting to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B. A voltage ripple on RBIAS can make critical internal error, so C_B is connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)

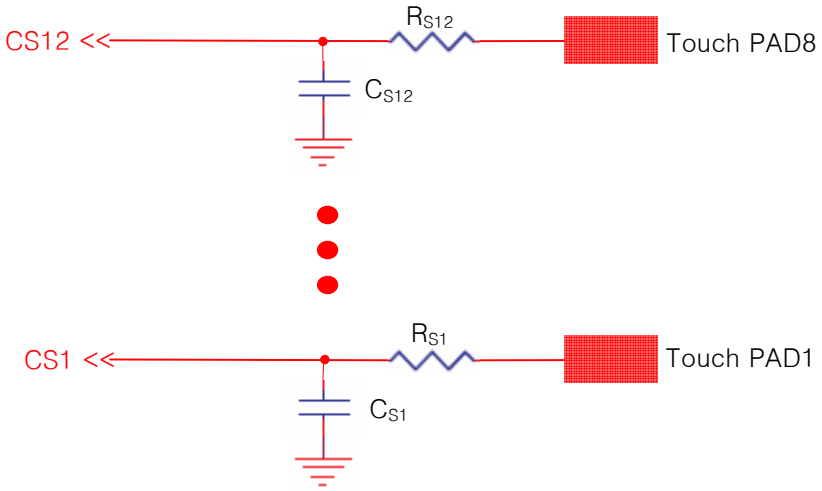
The R_{SB} should be connected as above figure when the TSM12 operates in IDLE Mode to save the current consumption. In this case, the consumption depends on the sum of the serial resistors and the response time might be longer.



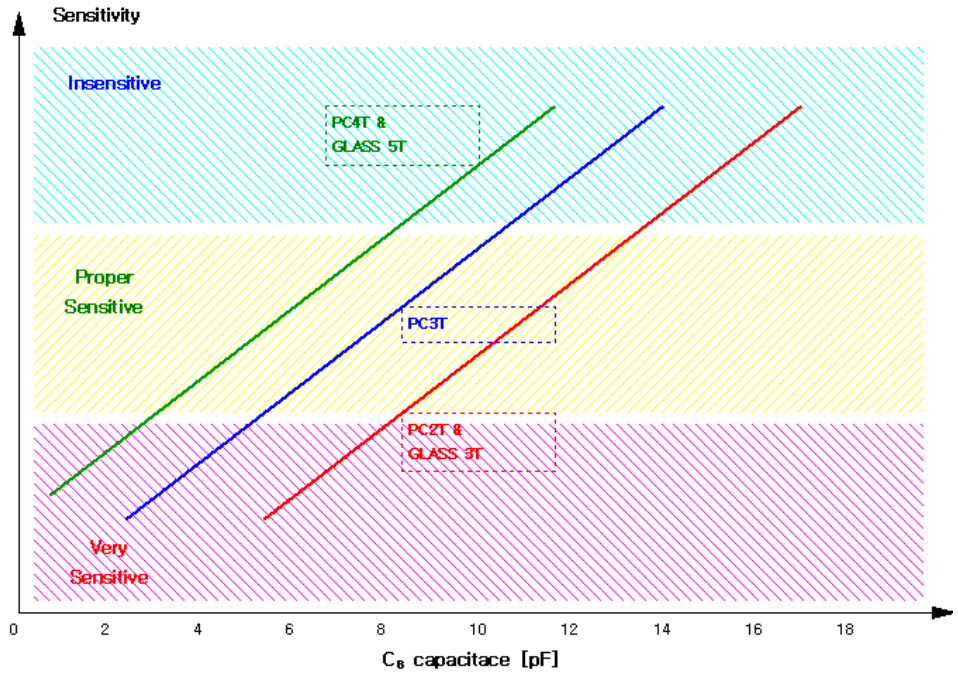
Normal operation current consumption curve (Pin21 I2C_EN is High)

The current consumption curve of TSM12 is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation



The TSM12 has basically eight steps sensitivity, which is available to control with internal register by I2C interface. The parallel capacitor C_{S1} is added to CS1 and C_{S12} to CS12 to adjust sensitivity. The sensitivity will be increased when smaller value of C_S is used. (Refer to the below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The internal touch decision process of each channel is separated from each other. The twelve channel touch key board application can therefore be designed by using only one TSM12 without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 ~ CS12 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.



Sensitivity example figure with default sensitivity selection

6.3 SYNC/OPT implementation

6.3.1 Output Mode Option

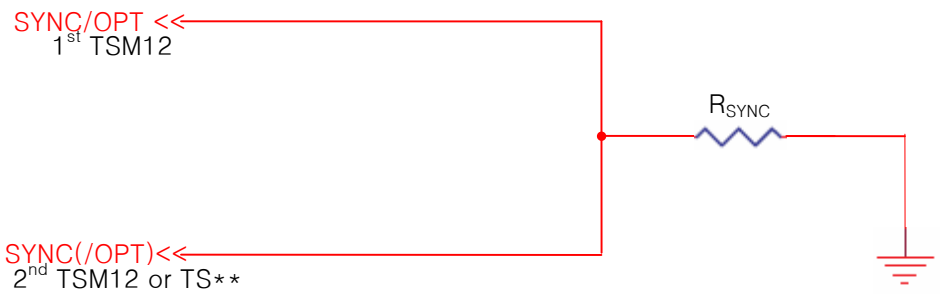
This pin will be assigned for the output mode option selection. It will decide that TSM12 is working on single or multi touch detection mode. It should be implemented as below for these.

(Single Output Mode Implementation)

(Multi Output Mode Implementation)

6.3.2 Multi Chip Application

Over two TSM12 can work on the one application at the same time thanks to SYNC function with this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. R_{SYNC} is pull-down resistor of SYNC/OPT pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. Typical value of R_{SYNC} is 2MΩ.The Sync pin should be implemented as below. The TSM12 can also be used with the other TSxx series by employing this SYNC function. The TSM12 could only operate on multi output mode in this configuration.



6.4 P_CDEG2 , P_CDEG1, P_CDEG0 implementation

The P_CDEG0, 1 and 2 are only for the CS1 to control the sensitivity. The sensitivity of channel 1 will be controlled by the register (refer to the "sensitivity control register" chapter) same as the other channel if the P_CDEG(2:0) value is 011. But it should be fixed as following table if the P_CDEG(2:0) value is not 011.

The sensitivity table of channel 1

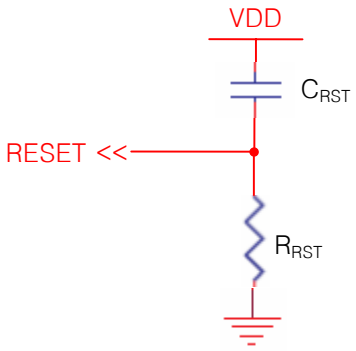
P_CDEG(2:0)	Sensitivity of Channel 1 (@Cs = 0pF)
011	Respect the register value (refer to the I2C register description)
000	14~16T
001	12~14T
010	10~12T
100	7~9T
101	6~8T
110	5~7T
111	3~5T

Note 1: The unit T represents the thickness (mm) of a panel in case of poly-carbonate.
Note 2: The above table data is compatible with a pad size that is approximately an half of the first knuckle. (it's about 10 ㎜ x 7 ㎜)

The channel 1 provides the output with two ways whether the I2C or the out1 (pin17) directly.

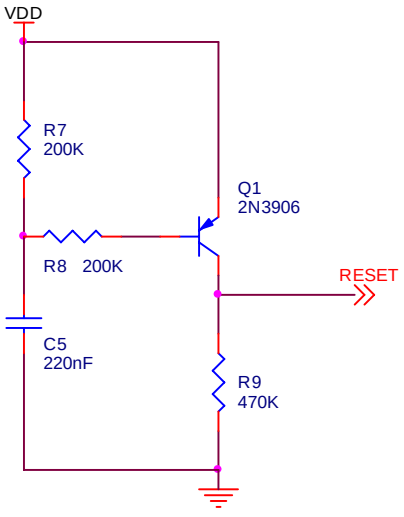
6.5 RESET implementation

TSM12 has internal data latches, so initial state of these latches must be reset by external reset pulse before normal operation starts. The reset pulse can be controlled by host MCU directly or other reset device. If not, the circuit should be composed as below figure. The reset pulse must have high pulse duration about a few msec to cover power VDD rising time. The recommended value of R_{RST} and C_{RST} are 330KΩ and 100nF.



Recommended reset circuits 1

The better performance is warranted with below reset circuit. The Q1 is turned on and makes reset pulse when power is on and VDD is raised to operating voltage. After a few msec (duration time is determined by R7, R8, C5), Q1 is turned off and TSM12 can be operated with normal sensitivity.

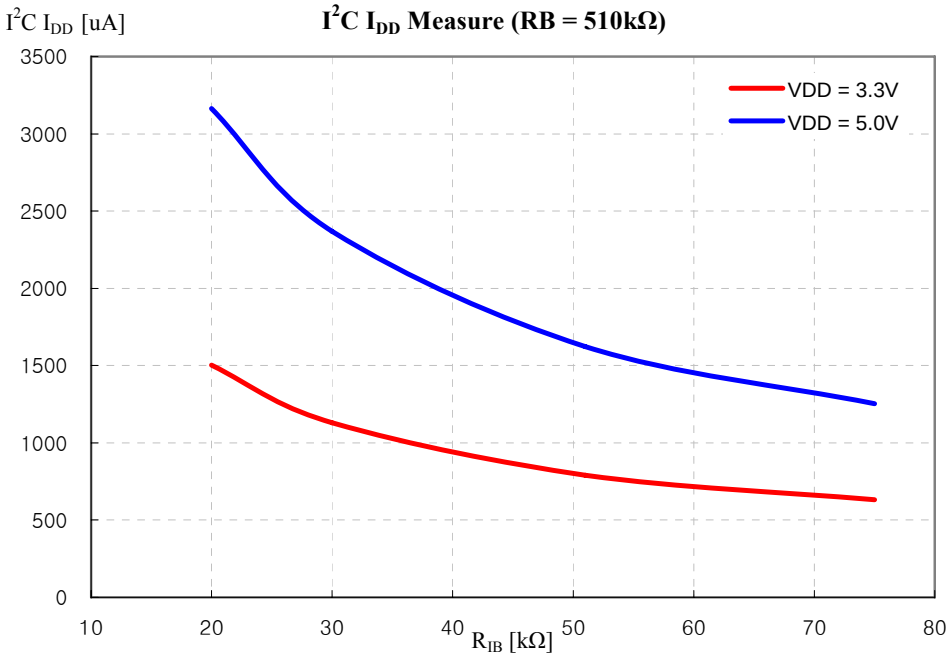


Recommended reset circuits 2

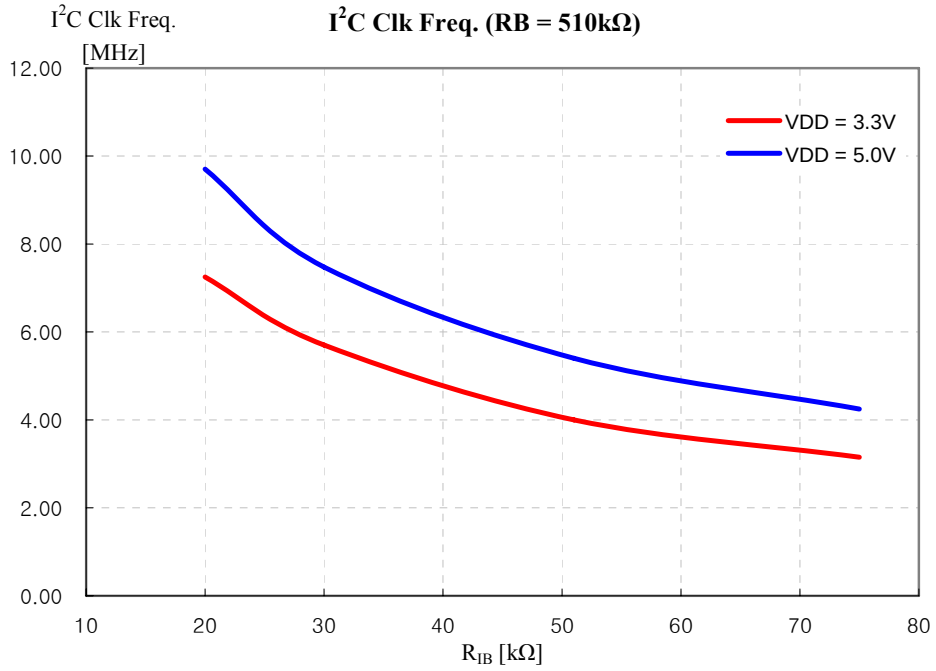
7 I²C Interface

7.1 IRBIAS Implementation

The R_{IB} is only charged in making the I2C internal clock and should be implemented as above figure. The smaller R_{IB} will increase the I2C internal clock frequency and current consumption. (Refer to the following consumption curve)



I2C Block operation current consumption curve

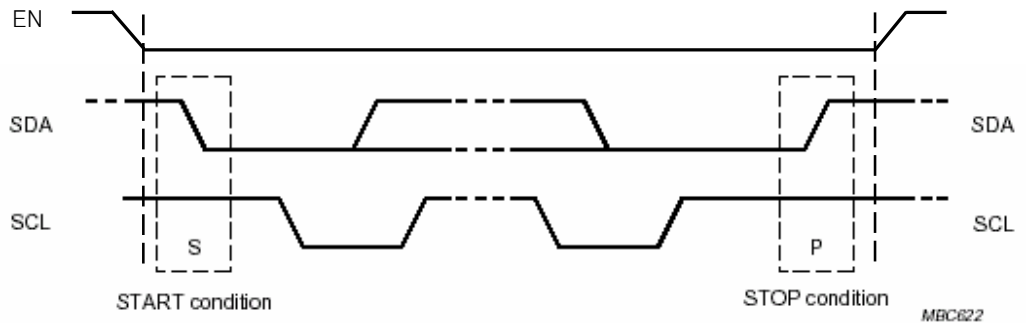


I2C clock frequency curve

7.2 Start & Stop Condition

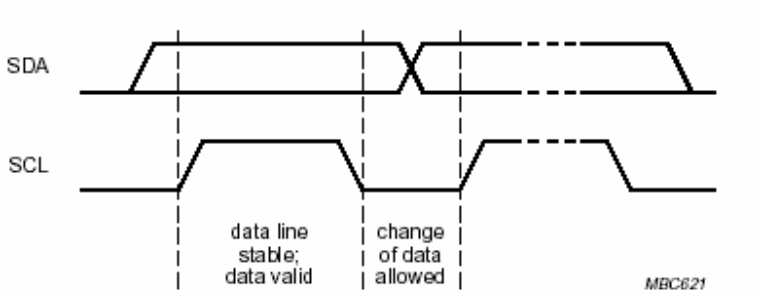
- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)

The EN (Pin21) should be low before START condition and be high after STOP condition.



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

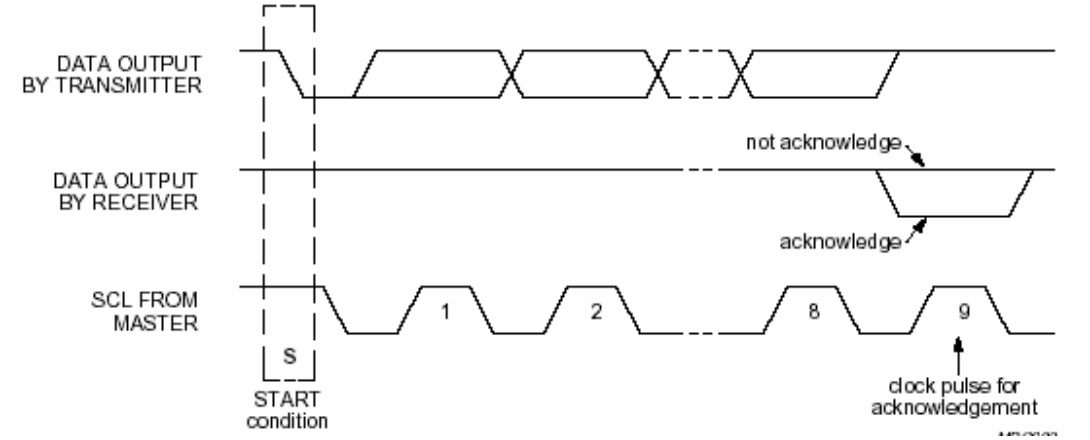


7.4 Byte Format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.6 First Byte

7.6.1 Slave Address

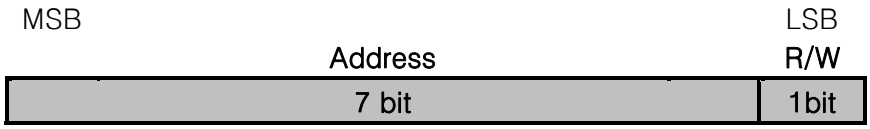
It is the first byte from the start condition. It is used to access the slave device.

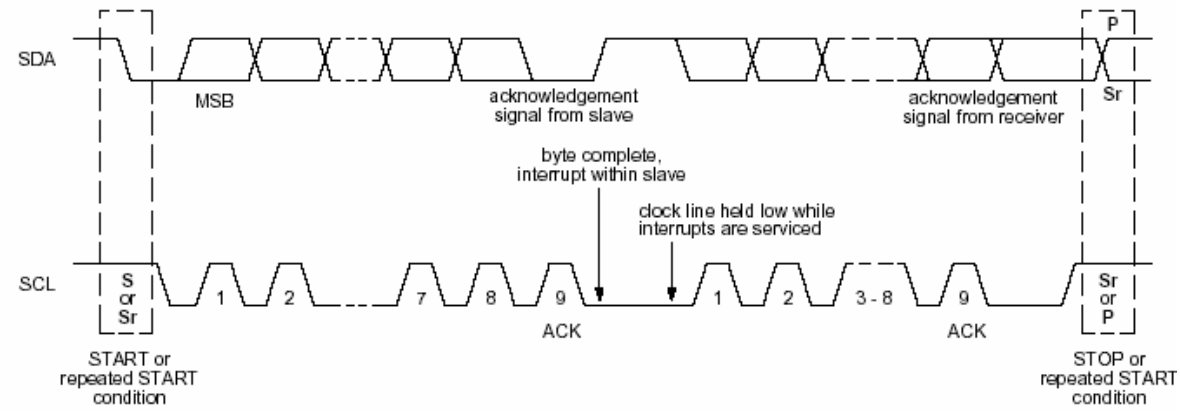
TSM12 Chip Address : 7bit

ID_SEL	Address
GND	0xD0
VDD	0xF0

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.



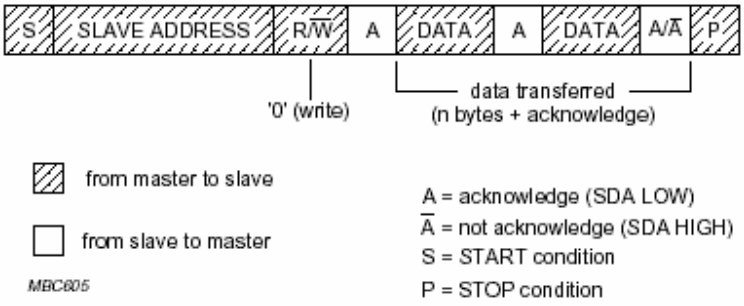


7.7 Transferring Data

7.7.1 Write Operation

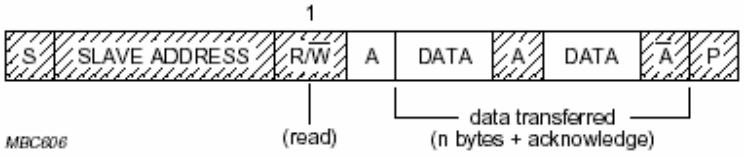
The byte sequence is as follows:

■ the first byte gives the device address plus the direction bit (R/W = 0).
■ the second byte contains the internal address of the first register to be accessed.
■ the next byte is written in the internal register. Following bytes are written in successive internal registers.
■ the transfer lasts until stop conditions are encountered.
■ the TSM12 acknowledges every byte transfer.

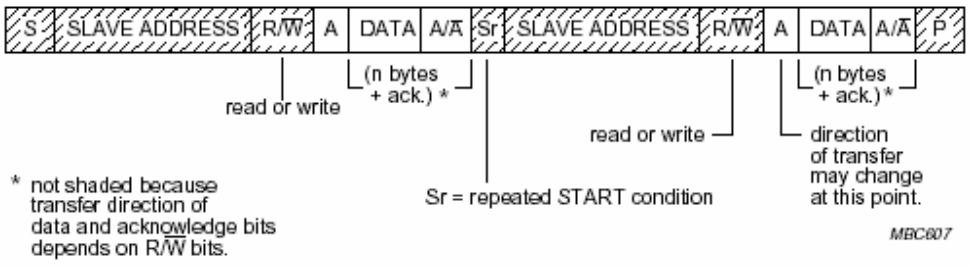


7.7.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD1	ACK	Data Read AA	ACK	Data Read BB	ACK	Stop

From Master to Slave

From Slave to Master

8 TSM12 Register List

◂ Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
◂ Note: The bit0 and bit1 of CTRL2 register must be written by 0b11 after power on during an initialize phase. (Refer to the chapter 9. initialize flow)
◂ Note: HS (High Sensitivity) / MS (Middle Sensitivity) / LS (Low Sensitivity)
◂ Note: Low Output (light touch) / Middle Output (middle touch) / High Output (hard touch)

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity1	02h	1011 1011	Ch2HL	Ch2M			Ch1HL	Ch1M		
Sensitivity2	03h	1011 1011	Ch4HL	Ch4M			Ch3HL	Ch3M		
Sensitivity3	04h	1011 1011	Ch6HL	Ch6M			Ch5HL	Ch5M		
Sensitivity4	05h	1011 1011	Ch8HL	Ch8M			Ch7HL	Ch7M		
Sensitivity5	06h	1011 1011	Ch10HL	Ch10M			Ch9HL	Ch9M		
Sensitivity6	07h	1011 1011	Ch12HL	Ch12M			Ch11HL	Ch11M		
CTRL1	08h	0010 0010	MS	FTC		ILC		RTC		
CTRL2	09h	0000 01XX	0	0	0	0	SRST	IDLE	1	1
Ref_rst1	0Ah	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ref_rst2	0Bh	0000 1111	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Ch_hold1	0Ch	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ch_hold2	0Dh	0000 1111	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Cal_hold1	0Eh	0000 0000	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Cal_hold2	0Fh	0000 0000	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Output1	10h	0000 0000	OUT4		OUT3		OUT2		OUT1	
Output2	11h	0000 0000	OUT8		OUT 7		OUT6		OUT5	
Output3	12h	0000 0000	OUT12		OUT11		OUT10		OUT9	

8.2 Sensitivity Control Register

Sensitivity1 Channel 1 & 2 Sensitivity Control

Address (hex): 02h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch2HL	Ch2M[2:0]			Ch1HL	Ch1M[2:0]		

Description

The sensitivity of channel 1 and 2 are adjustable by Sensitivity_1 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

Sensitivity2 Channel 3 & 4 Sensitivity Control

Address (hex): 03h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch4HL	Ch4M[2:0]			Ch3HL	Ch3M[2:0]		

Description

The sensitivity of channel 3 and 4 are adjustable by Sensitivity_2 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

Sensitivity3 Channel 5 & 6 Sensitivity Control

Address (hex): 04h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch6HL	Ch6M[2:0]			Ch5HL	Ch5M[2:0]		

Description

The sensitivity of channel 5 and 6 are adjustable by Sensitivity_3 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

Sensitivity4 Channel 7 & 8 Sensitivity Control

Address (hex): 05h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch8HL	Ch8M[2:0]			Ch7HL	Ch7M[2:0]		

Description

The sensitivity of channel 7 and 8 are adjustable by Sensitivity_4 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

Sensitivity5 Channel 9 & 10 Sensitivity Control

Address (hex): 06h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch10HL	Ch10M[2:0]			Ch9HL	Ch9M[2:0]		

Description

The sensitivity of channel 9 and 10 are adjustable by Sensitivity_5 register.ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

Sensitivity6 Channel 11 & 12 Sensitivity Control

Address (hex): 07h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch12HL	Ch12M[2:0]			Ch11HL	Ch11M[2:0]		

Description

The sensitivity of channel 11 and 12 are adjustable by Sensitivity_6 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000: 14~16T 001: 12~14T 010: 10~12T 011: 08~10T 100: 7~9T 101: 6~8T 110: 5~7T 111: 3~5T
ChxHL	1	High and Low sensitivity selection for channel x 0: HS = MS - (MS * 0.2) LS = MS + (MS * 0.2) 1: HS = MS - (MS * 0.3) LS = MS + (MS * 0.3)

8.3 General Control Register1

CTRL1 TSM12 General Control Register1

Address (hex): 08h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MS	FTC[1:0]		ILC[1:0]		RTC[2:0]		

Description

The calibration speed just after power on reset is very high during the time which is defined by FTC[1:0] to have a good adoption against unstable external environment.

Bit name	Reset	Function
MS	0	Mode Selection 0: auto alternate (fast/slow) mode 1: fast mode
FTC[1:0]	01	First Touch Control Below time stands on VDD = 3V / Rb = 300KΩ 00: 5 sec 01: 10 sec 10: 15 sec 11: 20 sec
ILC[1:0]	00	Interrupt Level Control 00: Interrupt is on middle or high output. 01: Interrupt is on low or middle or high output. 10: Interrupt is on middle or high output. 11: Interrupt is on high output.
RTC[2:0]	011	Response Time Control Response period = RTC[2:0] + 2

8.4 General Control Register2

CTRL2 TSM12 General Control Register2

Address (hex): 09h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	SRST	SLEEP	1	1

Description

All the digital blocks except analog and I2C block are reset when SRST is set. The SLEEP function allows getting very low current consumption when it is set. But the response time will be longer than normal operation. The bit0 and bit1 must be written with 0b'11 by host MCU.

Bit name	Reset	Function
SRST	0	Software Reset 0: Disable Software Reset 1: Enable Software Reset
SLEEP	1	Sleep Mode Enable 0: Disable Sleep Mode 1: Enable Sleep Mode
Bit[1:0]	XX	These bits must be written by 0b'11 during a system initialize phase. (refer to the chapter 9 "initialize flow example")

8.5 Channel Reference Reset Control Register

Ref_rst1 Channel1~8 Reference Reset Control

Address (hex): 0Ah
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Description
The reference value of each channel will be renewing when Chx is set.

Bit name	Reset	Function
Chx	1	0: Disable reference reset 1: Enable reference reset
Ch1	0	0: Disable reference reset 1: Enable reference reset

Ref_rst2 Channel9~12 Reference Reset Control

Address (hex): 0Bh
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Ch12	Ch11	Ch10	Ch9

Description
The reference value of each channel will be renewing when Chx is set.

Bit name	Reset	Function
Chx	1	0: Disable reference reset 1: Enable reference reset

8.6 Channel 1~8 Sensing Control Register

Ch_hold1 Channel 1 ~ 8 Hold Enable Register

Address (hex): 0Ch

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Description

The operation of each channel is independently available to control. A channel doesn't be worked and the calibration is paused when it is set.

Bit name	Reset	Function
Chx	1	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)
Ch1	0	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)

8.7 Channel 9~12 Sensing Control Register

Ch_hold2 Channel 9 ~ 12 Hold Enable Register

Address (hex): 0Dh

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Ch12	Ch11	Ch10	Ch9

Description

The operation of each channel is independently available to control. A channel doesn't be worked and the calibration is paused when it is set.

Bit name	Reset	Function
CEx	1	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)

8.8 Channel 1~8 Calibration Control Register

Cal_hold1 Channel 1 ~ 8 Calibration Enable Register

Address (hex): 0Eh

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset	Function
Chx	0	0: Enable reference calibration (sensing + calibration) 1: Disable reference calibration (sensing + No calibration)

8.9 Channel 9~12 Calibration Control Register

Cal_hold2 Channel 9 ~ 12 Calibration Enable Register

Address (hex): 0Fh

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Ch12	Ch11	Ch10	Ch9

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset	Function
Chx	0	0: Enable reference calibration (sensing + calibration) 1: Disable reference calibration (sensing + No calibration)

8.10 Output Register

Output1 Channel 1 ~ 4 Output Register

Address (hex): 10h
Type: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT4[1:0]		OUT3[1:0]		OUT2[1:0]		OUT1[1:0]	

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

Bit name	Reset	Function
OUT4[1:0]	00	Output of channel 4 00: No output 01: low output 10: middle output 11: high output
OUT3[1:0]	00	Output of channel 3 00: No output 01: low output 10: middle output 11: high output
OUT2[1:0]	00	Output of channel 2 00: No output 01: low output 10: middle output 11: high output
OUT1[1:0]	00	Output of channel 1 00: No output 01: low output 10: middle output 11: high output

Output2 Channel 5 ~ 8 Output Register

Address (hex): 11h

Type: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT8[1:0]		OUT7[1:0]		OUT6[1:0]		OUT5[1:0]	

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

Bit name	Reset	Function
OUT8[1:0]	00	Output of channel 8 00: No output 01: low output 10: middle output 11: high output
OUT7[1:0]	00	Output of channel 7 00: No output 01: low output 10: middle output 11: high output
OUT6[1:0]	00	Output of channel 6 00: No output 01: low output 10: middle output 11: high output
OUT5[1:0]	00	Output of channel 5 00: No output 01: low output 10: middle output 11: high output

Output3 Channel 9~ 12 Output Register

Address (hex): 12h

Type: R

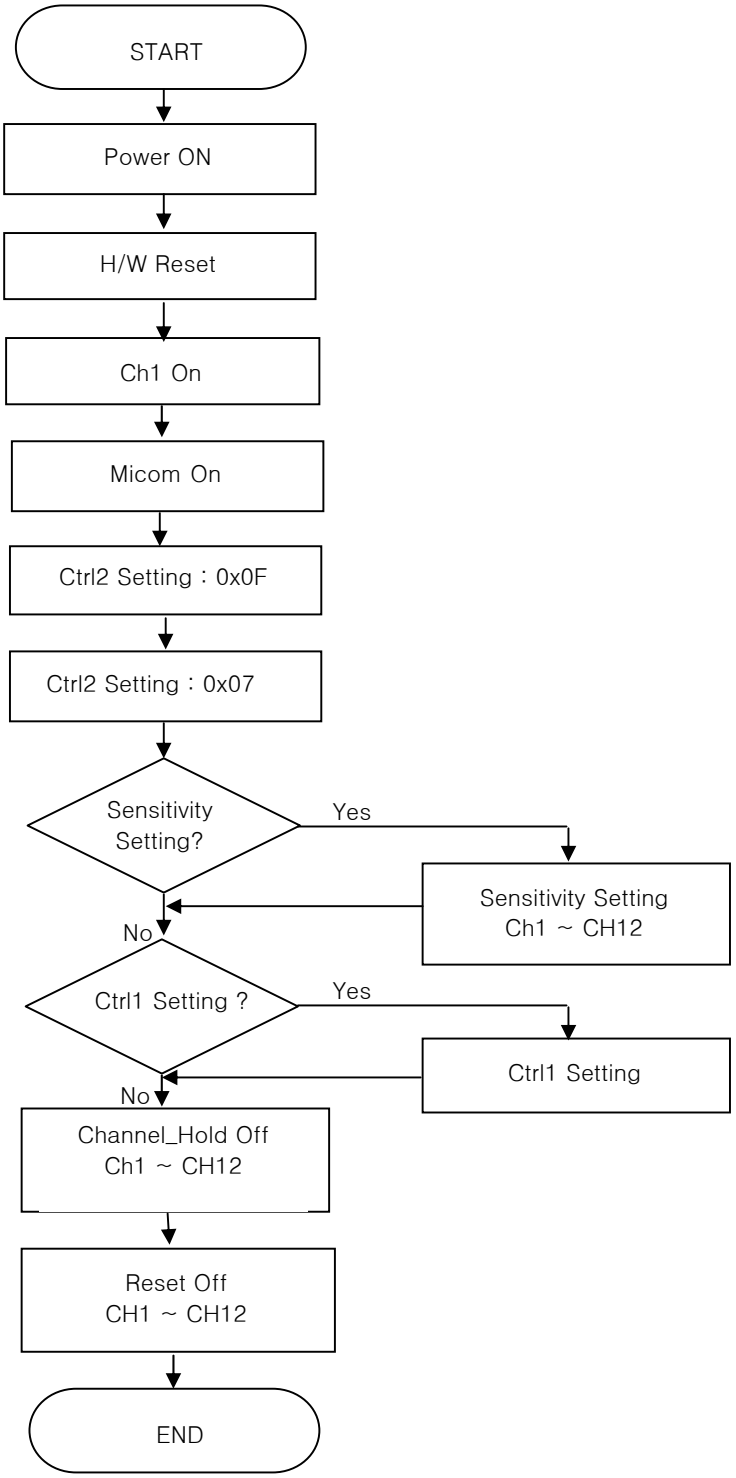
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT12[1:0]		OUT11[1:0]		OUT10[1:0]		OUT9[1:0]	

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

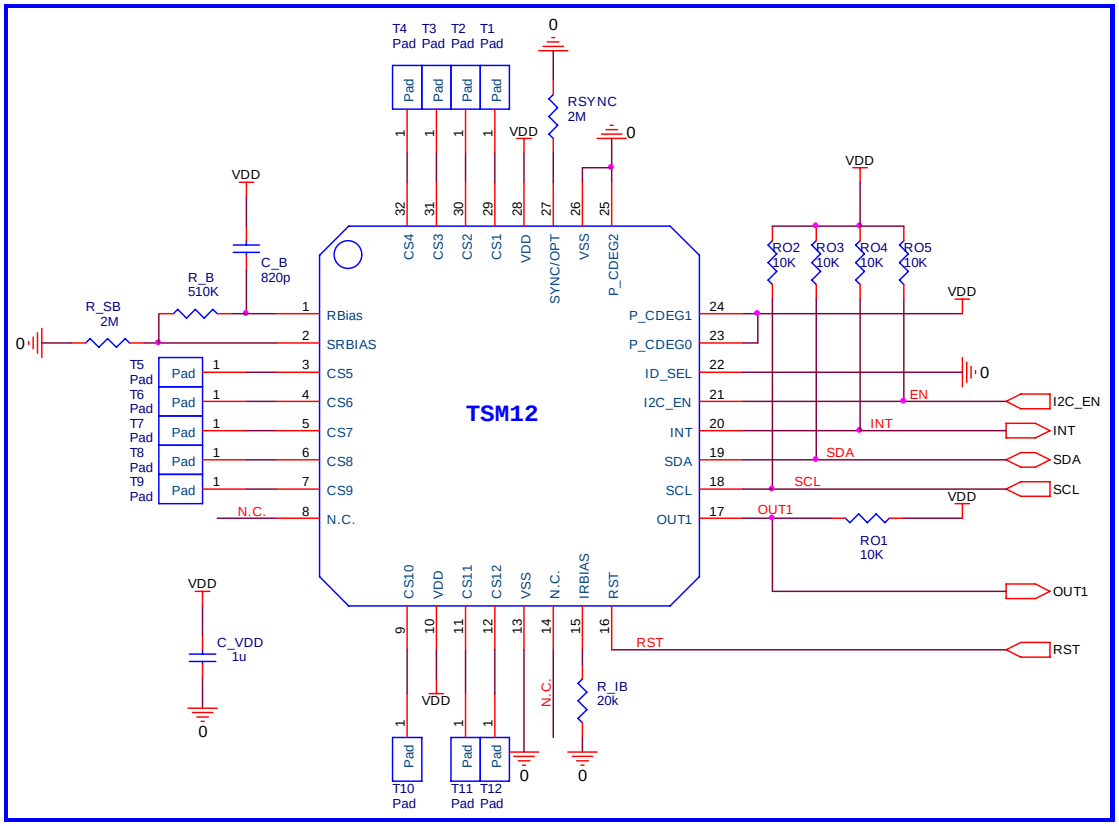
Bit name	Reset	Function
OUT12[1:0]	00	Output of channel 12 00: No output 01: low output 10: middle output 11: high output
OUT11[1:0]	00	Output of channel 11 00: No output 01: low output 10: middle output 11: high output
OUT10[1:0]	00	Output of channel 10 00: No output 01: low output 10: middle output 11: high output
OUT9[1:0]	00	Output of channel 9 00: No output 01: low output 10: middle output 11: high output

9 Recommended TSM12 Initialize Flow (Example)



10 Recommended Circuit Diagram

10.1 **Application Example in clean power environment**



TSM12 Application Example Circuit (Clean power environment)

- In PCB layout, R_B should not be placed on touch pattern. If not, C_B has to be connected. The R_B pattern should be routed as short as possible.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TSM12.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TSM12 is reset if RST Pin is high. (See 6.5 Reset implementation chapter)
- The TSM12 is working with single output mode if the SYNC/OPT pin is high and it will be in multi output mode when it's low. The resistor which is connected with GND should be connected with SYNC pin when the application is required over two TSM12 devices (Multi output mode).

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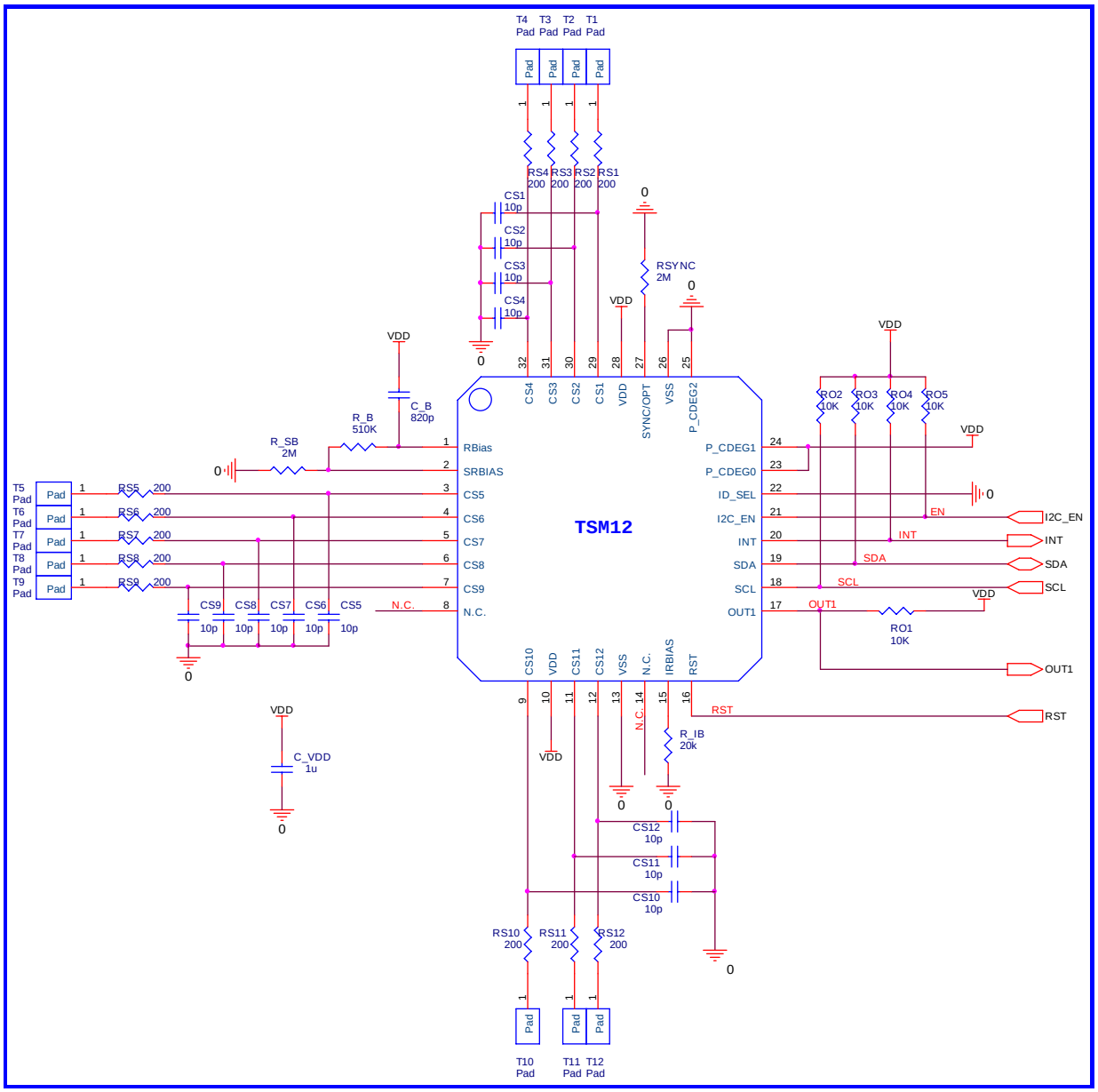
10.2 Application Example in noisy environment

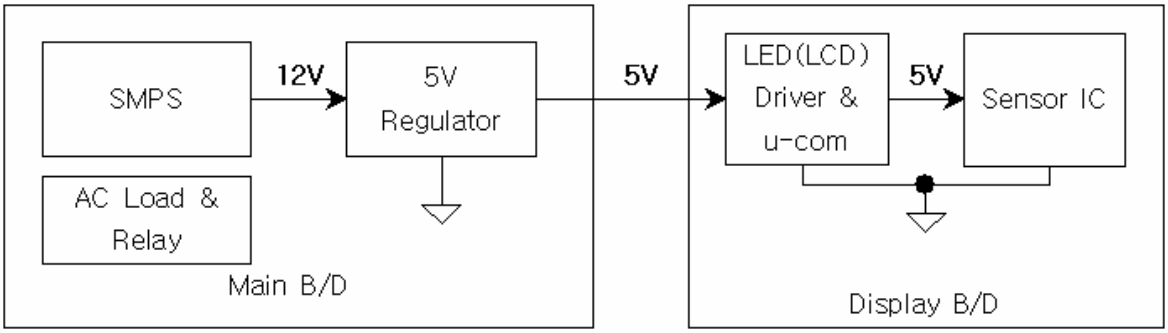


TSM12 Application Example Circuit (Noisy environment)

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The smaller R_B is recommended in noisy environments.

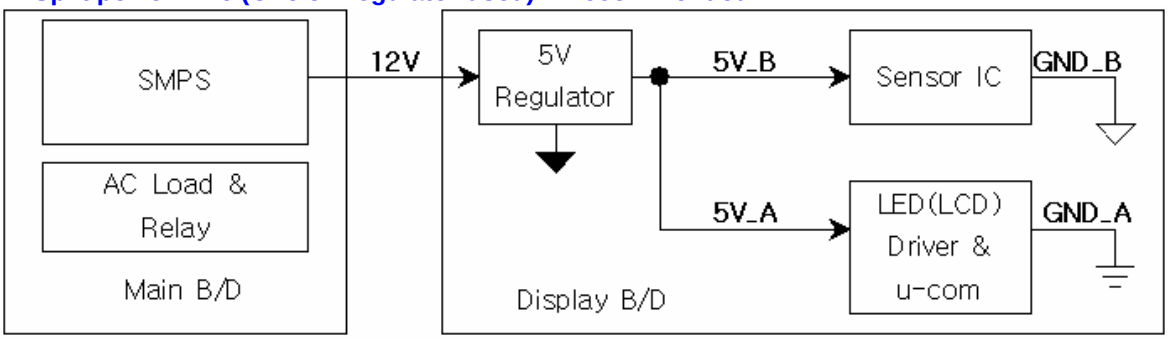
10.3 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

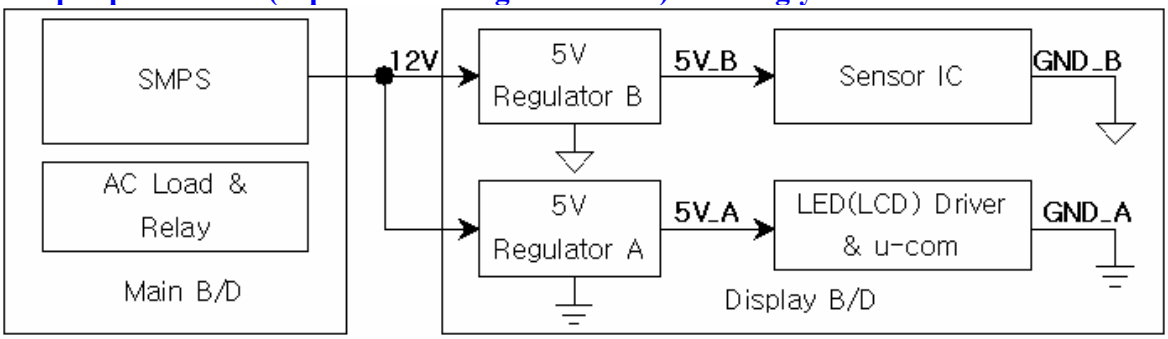


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

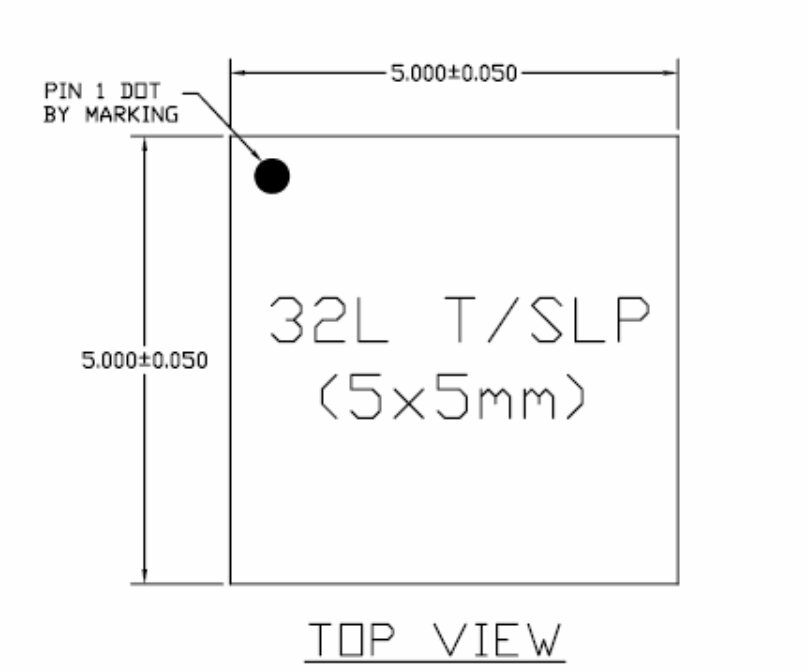
B. Split power Line (One 5V regulator used) – Recommended

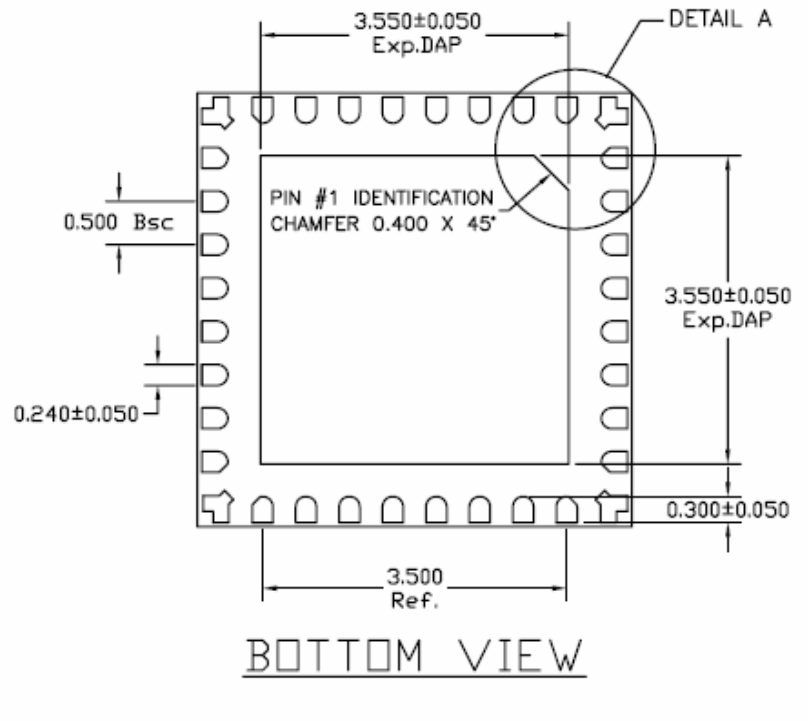


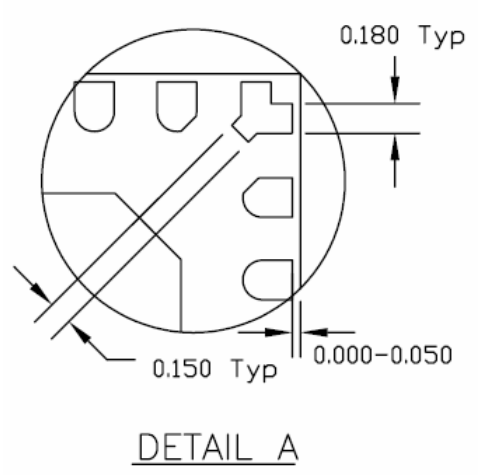
C. Split power Line (Separated 5V regulator used) – Strongly recommended

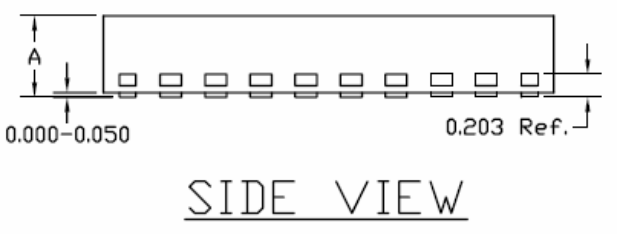


11 MECHANICAL DRAWING









		QFN
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

NOTE: Dimensions are in millimeters

12 MARKING DESCRIPTION

Device Code : **T S M 1 2**

Channel Number
Application
Touch Switch Group

Weekly Code : **YY ZZ**

Manufacturing Year
Manufacturing Week

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