Below is the diagram describing the design flow. It is a state machine with the following 8 states.

S0: SDA = '1', SCLK = '1'

S1: START CONDITION

S2: SWITCH TO HS-MODE – 0000 1XXXX

S3: SLAVE ADDRESSS AND WRITE BIT

1001 1100, expects an ACK in 9th clock cycle

S4: POINTER REGISTER BYTE, expects an ACK in 9th clock cycle

S5: WRITE THE CONFIGURATION REGISTER

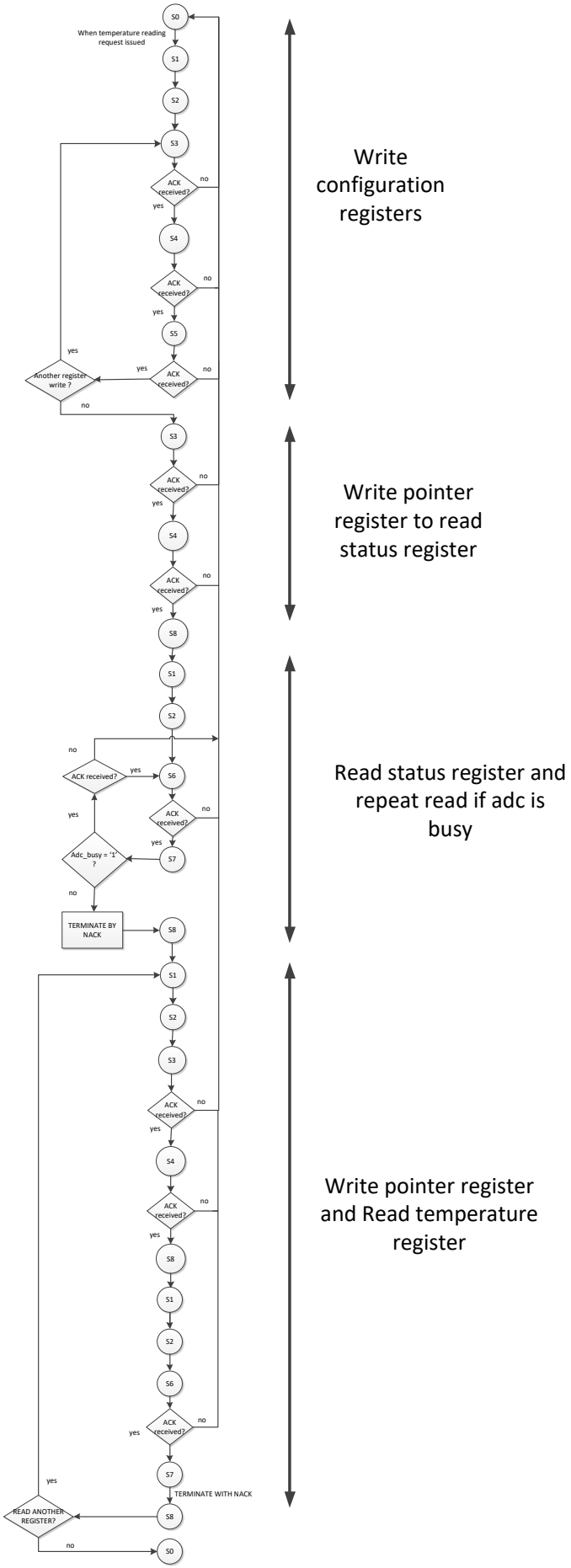
S6: SLAVE ADDRESSS AND READ BIT

1001 1101, expects an ACK in 9th clock cycle

S7: READ THE REGISTER VALUE, in the 9th clock cycle, issues nack to terminate read otherwise expects ack to continue reading the same register

S8: STOP CONDITION

The Configuration registers are written initially and then the status register is checked to see the status of adc. If adc is busy then repeat the read of the status register else, read the temperature registers.


S0
When temperature reading request issued
S1
S2
S3
ACK received?
no
yes
S4
ACK received?
no
yes
S5
yes
Another register write ?
yes
ACK received?
no
no
S3
ACK received?
no
yes
S4
ACK received?
no
yes
S8
S1
S2
no
ACK received?
yes
S6
ACK received?
no
yes
Adc_busy = '1' ?
yes
S7
no
TERMINATE BY NACK
S8
S1
S2
S3
ACK received?
no
yes
S4
ACK received?
no
yes
S8
S1
S2
S6
ACK received?
no
yes
S7
TERMINATE WITH NACK
yes
READ ANOTHER REGISTER?
S8
no
S0
Write configuration registers
Write pointer register to read status register
Read status register and repeat read if adc is busy
Write pointer register and Read temperature register