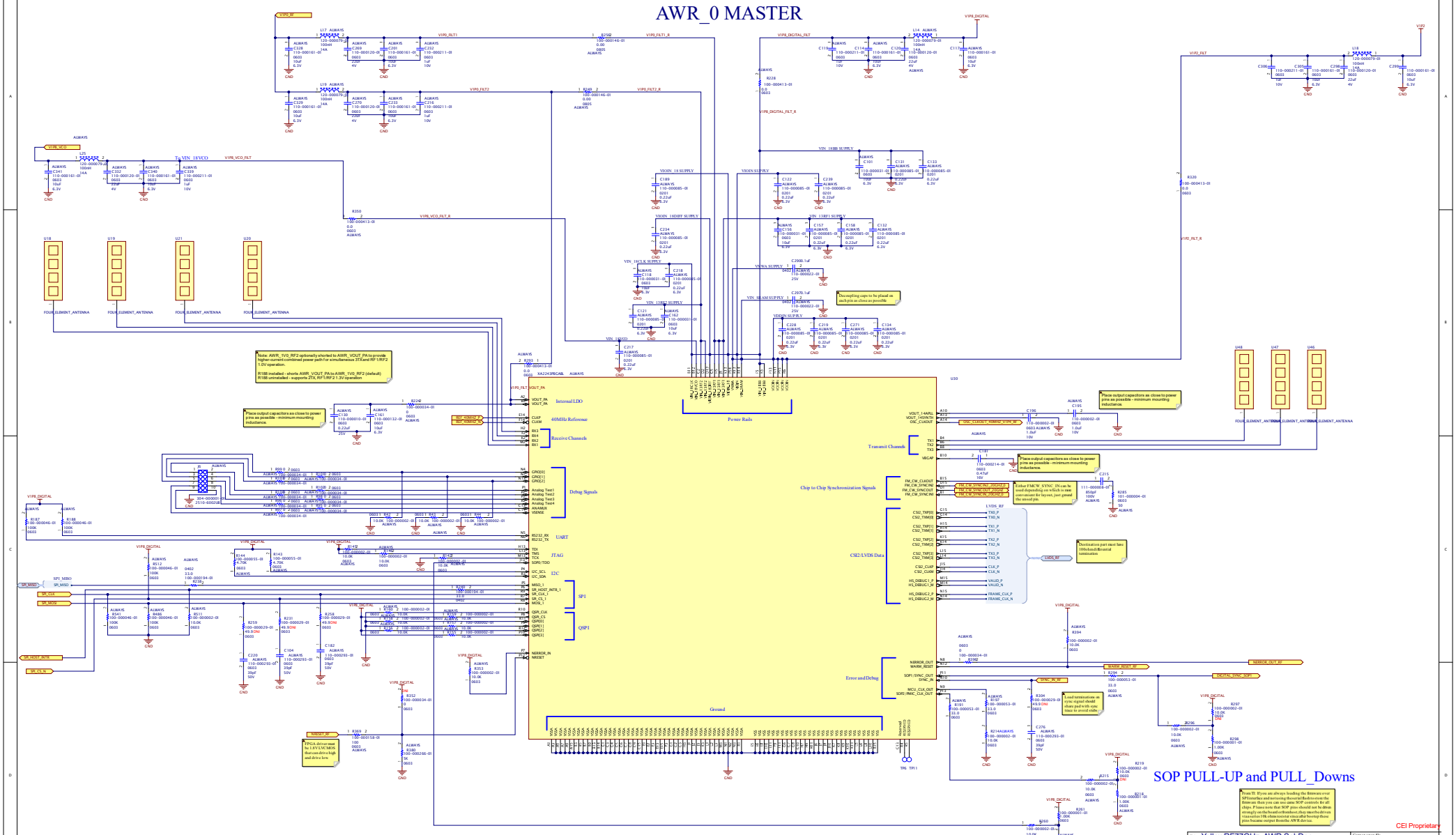
AWR_0 MASTER


SOP PULL-UP and PULL_Downs
Note: AWR_1V0_RF2 optionally shorted to AWR_VOUT_PA to provide higher-current combined power path for simultaneous 3TX and RF1/RF2 1.0V operation.
R188 installed - shorts AWR_VOUT_PA to AWR_1V0_RF2 (default)
R188 uninstalled - supports 2TX, RF1/RF2 1.3V operation
Place output capacitors as close to power pins as possible - minimum mounting inductance.
Decoupling caps to be placed on each pin as close as possible
Power Rails
Internal LDO
40MHz Reference
Receive Channels
Transmit Channels
Debug Signals
Chip to Chip Synchronization Signals
CSI2/LVDS Data
UART
JTAG
I2C
SPI
QSPI
Error and Debug
Ground
Either FMCW_SYNC IN can be used depending on which is more convenient for layout, just ground the unused pin.
Destination port must have 100ohm differential termination
Load terminations on sync signal should share pad with sync trace to avoid stubs
FPGA driver must be 1.8V LVCMOS that can drive high and drive low
From TI: If you are always loading the firmware over SPI interface and not using the serial flash to store the firmware then you can use same SOP controls for all chips. Please note that SOP pins should not be driven strongly on the board or floatiest, they must be driven via a series 10k ohms resistor since after bootup these pins become output from the AWR device.
CEI Proprietary
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