DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4223511

DRAFTER:	K. SINCERBOX	DATE:	08/01/2017
DESIGNER:		DATE:	
CHECKER:	K. SINCERBOX	DATE:	04/02/2018
ENGINEER:	F. MORTAN	DATE:	04/02/2018
APPROVED:	D. CHIN & D. BABARAN	DATE:	04/02/2018
RELEASED:	WDM	DATE:	04/02/2018
TEMPLATE INFO:	EDGE# 4218519	DATE:	04/07/2016

DIMENSIONS IN MILLIMETERS

TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER 01295

ePOD, RNV0018C / VQFN-HR,
18 PIN, 0.5 MM PITCH

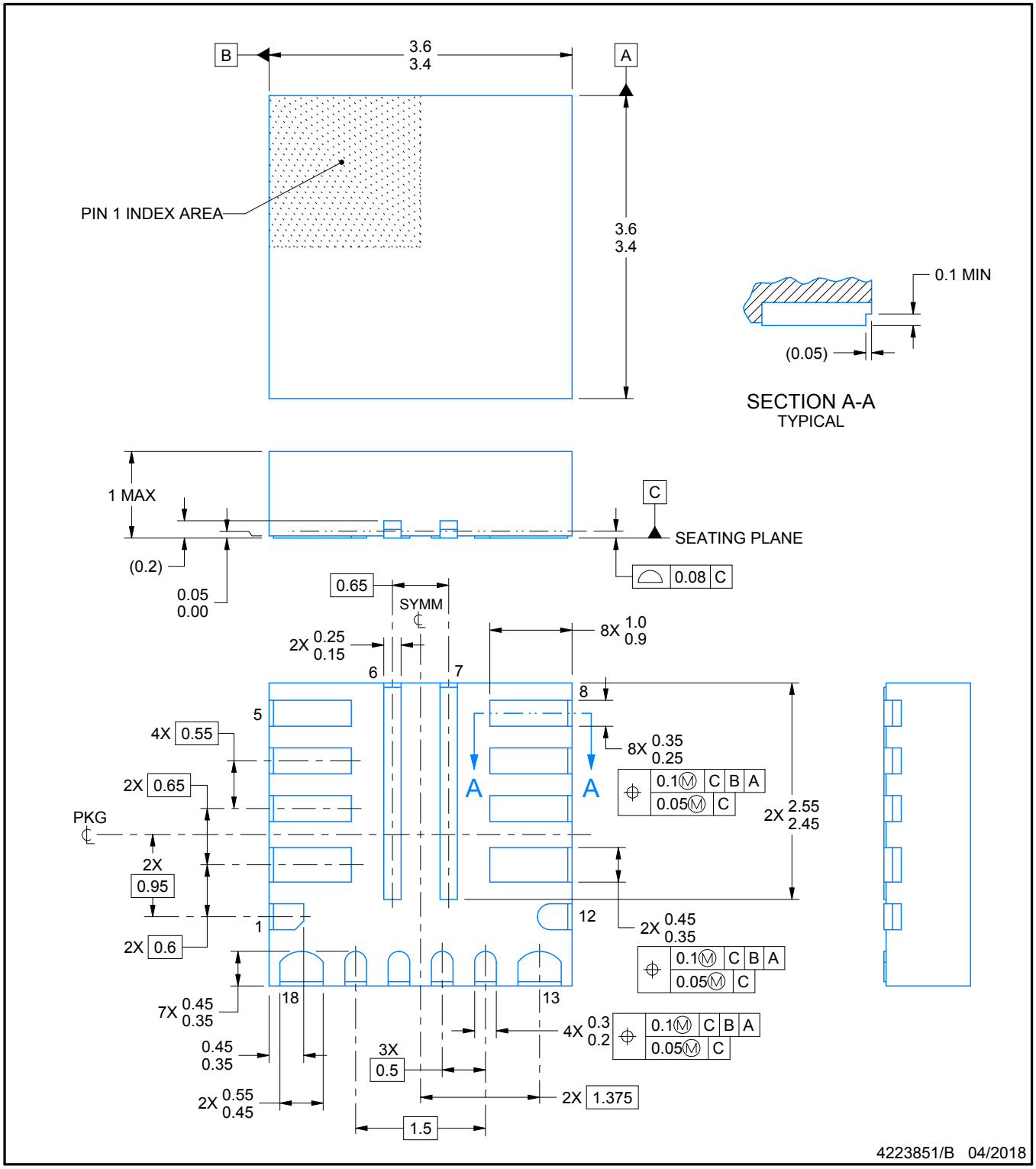
SCALE	SIZE		REV	PAGE
NTS	A	4223851	B	1 OF 5

RNV0018C

PACKAGE OUTLINE

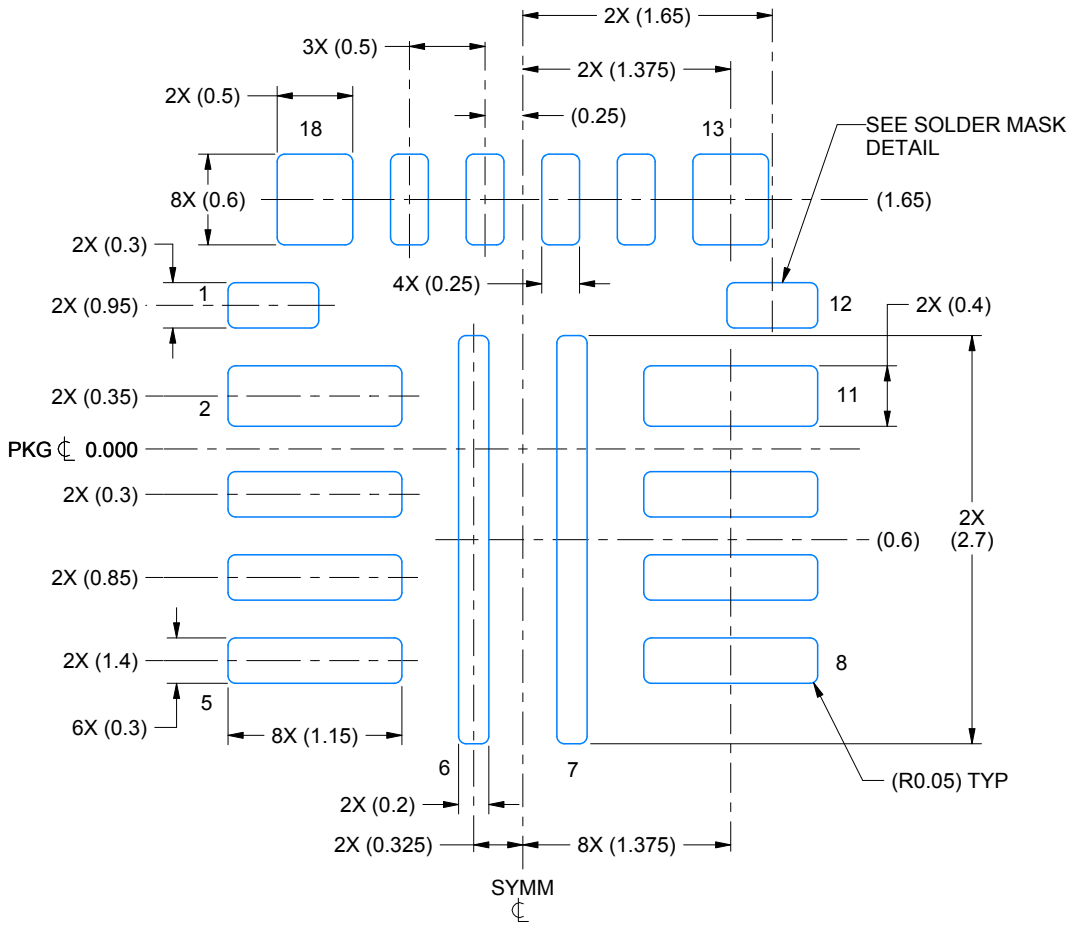
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

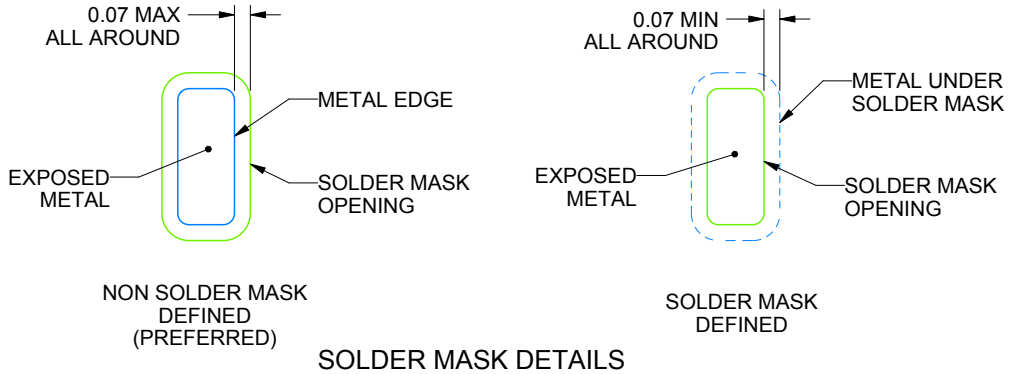


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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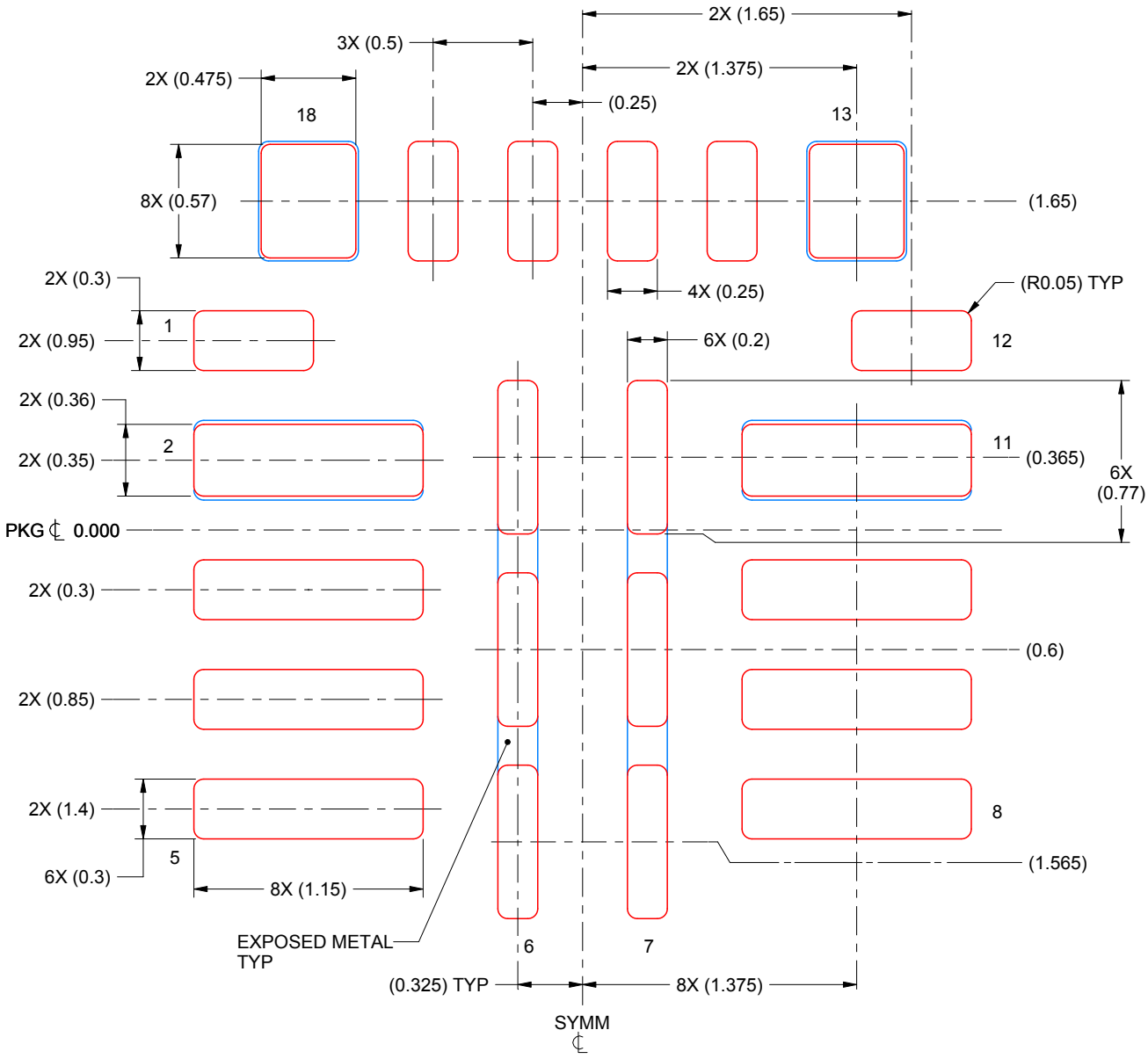
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. If any vias are implemented, it is recommended that vias under paste to be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 85.6% - PADS 2, 11, 13 & 18: 90%
SCALE:30X

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NOTES: (continued)

6. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2167471	08/01/2017	K. PHAM / K. SINCERBOX
B	CHANGE LAND PATTERN TO NSMD PREFERRED	2172698	04/02/2018	F. MORTAN / K. SINCERBOX