

CMRR Quiz Problems

1

Quiz: CMRR

1. In reviewing the CMRR specifications for an amplifier, the specification is listed for multiple different common mode ranges. For the full common mode range the CMRR is degraded. Why?
 - a) All bipolar devices have this relationship for CMRR. It is due to the *Beta* change for larger input voltages.
 - b) ESD diode leakage will impact CMRR for larger input signals.
 - c) This is due to drain-to-source capacitance on CMOS devices.
 - d) This is due to a transition between the P-channel and N-channel input pairs on rail-to-rail devices.

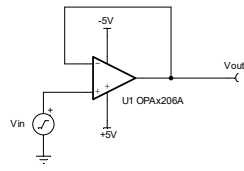
Parameter		Test Conditions	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	$V_S = 5.5 \text{ V}, (V-) - 0.2 \text{ V} < V_{CM} < (V+) - 1.4 \text{ V},$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$	76	90		dB
		$V_S = 5.5 \text{ V}, V_{CM} = -0.2 \text{ V to } 5.7 \text{ V},$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$	65	80		dB

TI Information – Selective Disclosure

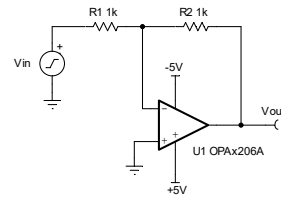


Quiz: CMRR

2. Which circuit below will not be impacted by CMRR issues?
- a) Circuit A.
 - b) Circuit B.
 - c) Both circuits will have CMRR effects.



Circuit A



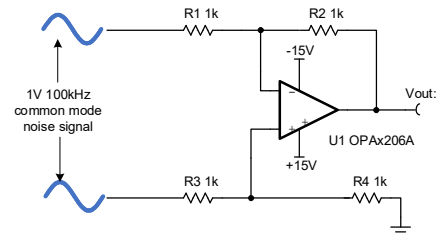
Circuit B

T1 Information – Selective Disclosure

 TEXAS INSTRUMENTS

Quiz: CMRR

3. The circuit below has matched resistors ($R1 = R2 = R3 = R4$). A 1V 10kHz common mode noise signal is picked up on the input leads. Some of the common mode signal appears at the amplifier output. Would the output due to common mode be better or worse at higher frequencies?
- a) Better
 - b) Worse



CMRR Quiz Solutions

Hello, and welcome to the lecture for the TI Precision Lab discussing input offset voltage, or V_{OS} . In this lecture we'll discuss op amp V_{OS} specifications, V_{OS} drift over temperature, input bias current (or I_B), and input bias current drift over temperature. We'll also show the range of V_{OS} and I_B across many different Texas Instruments op amps.

TI Information – Selective Disclosure

 TEXAS INSTRUMENTS

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TI Information – Selective Disclosure

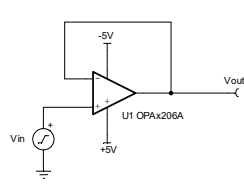


The N and P type input pairs often do not have well matched offset voltage. So, when the common mode transitions through the crossover-region, the offset will make a large transition. Since CMRR is $20\log(\Delta V_{os}/\Delta V_{cm})$, the large change in offset causes CMRR to degrade.

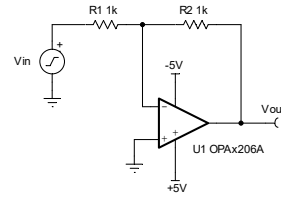
Quiz: CMRR

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Circuit A



Circuit B

T1 Information – Selective Disclosure

TEXAS INSTRUMENTS

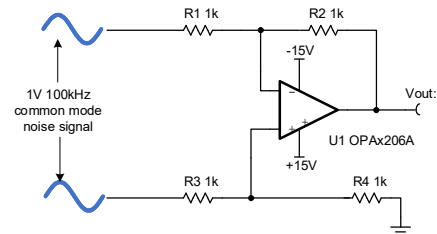
The common mode is held constant in the inverting configuration ($V_{cm} = 0V$ for circuit B). If V_{cm} is constant CMRR is not an issue.

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a) Better

b) Worse



T1 Information - Selective Disclosure

TEXAS INSTRUMENTS

CMRR degrades at high frequency. Look at the CMRR curve.