



Infinite possibilities...

Professional Audio Development Kit

User's Guide

September, 2007

Revision history

Revision	Date	Comments
1.0	July, 2005	First version.
1.1	September, 2005	Added <i>Downloading an application without a JTAG emulator</i> section.
2.0	February, 2006	Updated for release 2.0 and folder structure.
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Introduction

Congratulations on the purchase of your professional audio development kit (or PADK). The PADK is completely compatible and integrated with Code Composer Studio and eXpressDSP from Texas Instruments. The PADK also comes equipped with drivers for all the peripheral elements of the board, as well as application examples and an Audio Streaming and Wavetable Solution demonstration that truly showcases the potential of the PADK and its TMS320C6727 digital signal processor.

Organization

This document presents the PADK and explains how to install and use it.

[Product overview](#) presents a general overview of the PADK.

[Using the PADK](#) introduces application examples and demonstrations designed to help you use the PADK.

[Specifications](#) presents the main specifications of the PADK.

Conventions

In a procedure containing several steps, the operations that the user has to execute are numbered (1, 2, 3...). The diamond (♦) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (a, b, c...) can also be used to indicate secondary steps in a complex procedure.

The abbreviation *NC* is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in **bold** font style.

The abbreviation *N/A* is used to indicate something that is not applicable or not available at the time of press.

Note

The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

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Telephone: (1) (418) 877-4644
(1) (888) 922-4644
Hours: Monday to Friday, 9:00 AM to 5:00 PM (EST)
Fax: (1) (418) 877-7710
E-mail: support@lyrtech.com

Before reading this user's guide and sending your registration card, note the serial number of your PADK, its software version number (on the supplied CD-ROM), and its date of purchase. This information is necessary when you call for service.

Serial number	_____
Software version	_____
Date of purchase	_____

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Product overview

This chapter gives an overview of the PADK, presenting its features, components and their functions, as well as minimum hardware and software requirements necessary to use the PADK.

Outstanding features

The PADK boasts of the following outstanding features:

High-quality BURR-BROWN 24-bit resolution analog-to-digital and digital-to-analog converters

The PADK comprises two ADC and two DAC, each with four channels. The converters are capable of sampling rates of up to 192 kHz and they are used in multichannel coding, processing, and sound generation.

S/PDIF coaxial and optical digital audio input and output connectors

Also capable of sampling rates of up to 192 kHz, they are ideal for direct digital professional audio application development. The digital audio input incorporates a high-resolution sampling rate converter that allows you to simultaneously operate at different input and output sampling rates, as well as to lock onto various audio and word clock input sources.

Hi-speed USB port

Perfect for high-speed communications to host computers, it allows you to stream audio in real time, to download large sound banks, and to handle any other high-bandwidth applications.

MIDI connector

This type of connector is used to directly interface with external musical instruments and controllers.

Analog input connectors

These connectors are used to connect external control inputs, such as pedals and switches..

Supported file types

The PADK supports the following types of files.

Mp3Reverb

MP3, 44.1-kHz stereo

Audio Streaming and Wavetable Solution

- WAV up to 44.1 kHz (monophonic, stereo)
- MP3 up to 44.1 kHz (monophonic, stereo)
- MIDI (.mid)
- Soundfont (.sf2)

Hardware overview

This section presents an overview of the PADK at a hardware level. The PADK incorporates the following components. They are followed by a brief explanation of their functions.

Front view

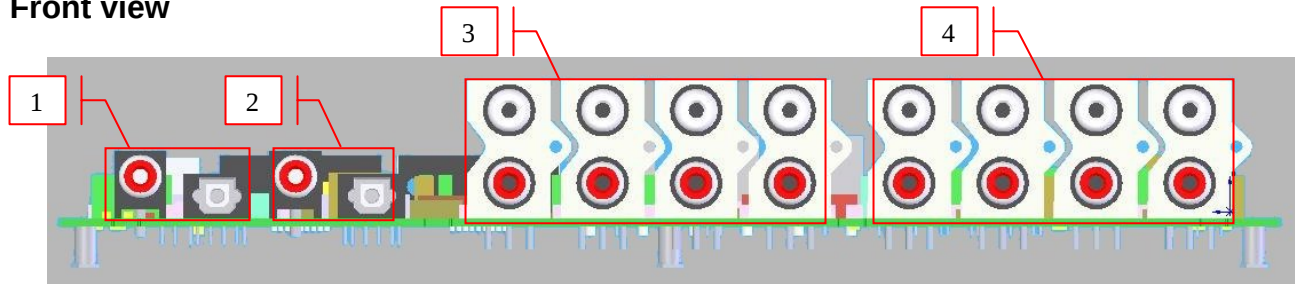


Figure 1 PADK front view

1. Digital stereo input connectors (S/PDIF)

Used to input digital stereo signals to the PADK through its coaxial or optical connector.

2. Digital stereo output connectors (S/PDIF)

Used to output digital stereo signals from the PADK through its coaxial or optical connector.

3. Analog input connectors

The PADK is equipped with eight analog input RCA connectors, through which you can input unbalanced line-level analog audio signals. The signals input to these connectors are converted through the two onboard analog-to-digital converters.

4. Analog output connectors

The PADK is also equipped with eight analog output RCA connectors, through which you can output unbalanced line-level analog audio signals. The signals output from these connectors are converted through the two onboard digital-to-analog converters.

Top view

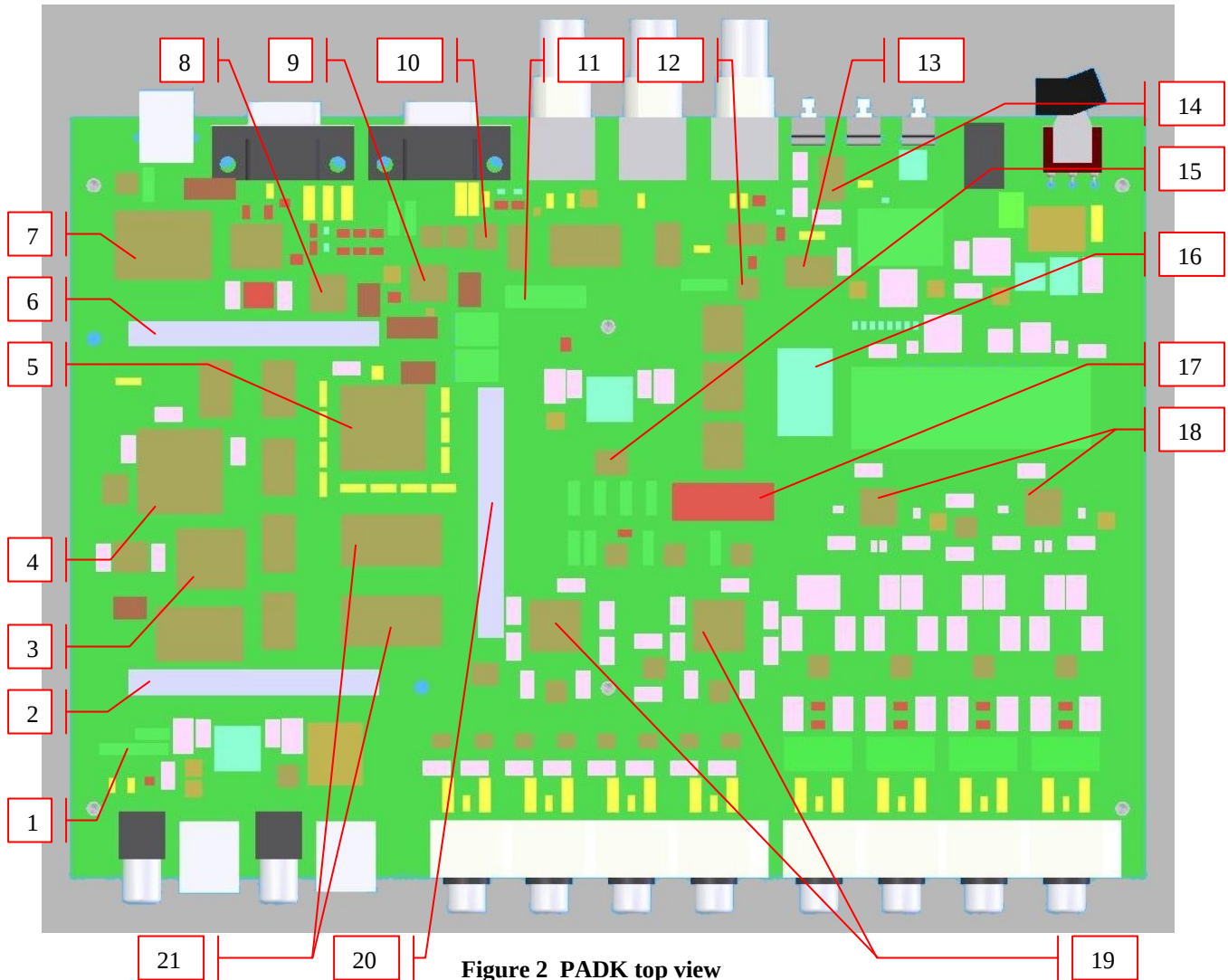


Figure 2 PADK top view

1. FPGA Joint test action group (JTAG) interface

This 6-pin header is used as an interface for FPGA development.

2. DSK connector

Used to connect user-supplied expansion modules based on the Texas Instruments DSK standard.

3. Flash memory

The PADK has a flash memory capacity of 8 MB.

4. Field-programmable gate array (FPGA)

The PADK uses a Xilinx Spartan-IIE as its FPGA to prototype professional audio applications.

5. Digital signal processor (DSP)

The PADK is equipped with one Texas Instruments TMS320C6727 high-performance, 32-bit floating-point DSP. The processor uses a 300-MHz or 350-MHz internal clock, yielding a performance that can reach up to 2100 MFLOPS or 2800 MIPS.

6. DSK connector

Used to connect user-supplied expansion modules based on the Texas Instruments DSK standard.

7. Universal serial bus (USB) microcontroller

Cypress Semiconductor EZ-USB FX2 microcontroller (CY7C68013) that supports USB and Hi-speed USB connections.

8. Musical instrument digital interface (MIDI) UART

TL16C550 that handles the asynchronous signals from musical instruments, for example. It is also capable of an alternate FIFO mode, relieving the DSP of excessive software overhead.

9. Universal asynchronous receiver/transmitter (UART)

TL16C550 that handles the asynchronous signals of non-MIDI devices.

10. 8-bit analog-to-digital converter (ADC)

The ADS7830 is a single-supply, low-power, 8-bit ADC equipped with a serial I²C interface used for external control input, such as pedals and switches.

11. DSP Joint test action group (JTAG) interface

This 14-pin header is used as a debugging interface with Code Composer Studio from Texas Instruments.

12. I²C serial EEPROM

Electrically erasable programmable read-only memory.

13. Stereo asynchronous sample rate converter (SRC)

The SRC4192 combines a wide input-to-output sampling ratio (from 16:1 to 1:16) with an outstanding dynamic range (144 dB). It can automatically detect the input-to-output sampling ratio and it is capable of time division multiplexed mode.

14. Digital interface receiver (DIR)

Cirrus Logic CS8416 capable of sampling digital audio signals at rates of up to 192 kHz, which is ideal for next-generation audio formats such as DVD-Audio. It is also capable of coaxial and optical connections.

15. SPI serial EEPROM

Electrically erasable programmable read-only memory.

16. Seven-segment display

The seven-segment display can be programmed to display error codes, messages, *et cetera*.

17. DIP switches

The DIP switches can be used as general-purpose selection switches. A PADK function is supplied that allows you to determine the status of the DIP switches.

18. Audio digital-to-analog converter (DAC)

The PADK is equipped with two, four-channel, 24-bit BURR-BROWN PCM4104 capable of sampling rates of up to 192 kHz.

19. Audio analog-to-digital converter (ADC)

The PADK is equipped with two, four-channel, 24-bit BURR-BROWN PCM4204 capable of sampling rates of up to 192 kHz.

20. DSK connector

Used to connect user-supplied expansion modules based on the Texas Instruments DSK standard.

21. Synchronous dynamic random access memory (SDRAM)

The PADK is equipped with a 128-MB SDRAM.

Rear view

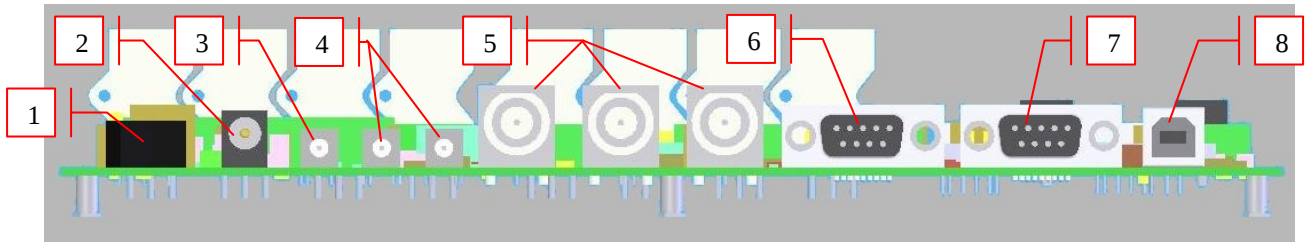


Figure 3 PADK rear view

1. Power switch

Used to turn the PADK on and off.

2. Power connector

Used to connect the +5 V DC universal power supply included with the PADK.

3. Reset switch

This switch is used to reset the PADK. In other words, pressing this switch reinitializes all DSP and FPGA registers, returning them to their default values.

Note

Pressing this switch does not delete the programming on the FPGA.

4. User switches

General-purpose push-button switches that can be used to configure various options.

5. Word clock connectors

Because the precise and accurate timing of digital audio samples is critical to the correct operation of interconnected digital audio equipment, the PADK is equipped with word clock connectors, respectively (from left to right) **IN**, **THRU**, and **OUT**.

6. Serial interface (RS-232) connector

The serial interface allows the PADK to communicate with the COM port of your computer.

7. MIDI/analog connector

The PADK is equipped with a MIDI connector controlled through a TL16C550 UART. It is comprised of MIDI in and out ports, as well as with an analog port.

8. USB port

The PADK is equipped with a Hi-speed USB port (USB 2.0) controlled through a Cypress Semiconductor EZ-USB FX2 microcontroller (CY7C68013).

For technical information about PADK-specific components, refer to the PADK technical reference guide.

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Using the PADK

This chapter presents PADK application examples, when used in conjunction with the Texas Instruments Code Composer Studio and eXpressDSP tools. The PADK comes with eight application examples that need to be compiled with the appropriate tool, and then accomplish a certain task.

The PADK also comes with two demonstrations, presented at the end of the chapter.

Basic application examples

Initial PADK example

Running *HelloWorld.pjt* simply displays *Hello world* in the Code Composer Studio window.

Using the DIP switches, push buttons, and user-defined LED

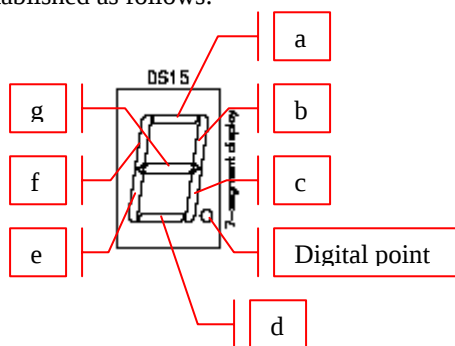
SwitchesAndLeds.pjt demonstrates how to use the DIP switches, push buttons, and user-defined LED of the PADK. The demonstration is divided into three stages.

The first stage of the demonstration sets LED DS7 to DS14 according to the state (on/off) of the corresponding DIP switches of the S5 array. Correspondence is established as follows:

- DS7 switch 1
- DS8 switch 2
- DS9 switch 3
- DS10 switch 4
- DS11 switch 5
- DS12 switch 6
- DS13 switch 7
- DS14 switch 8

The second stage lights the seven-segment display DS15 segments according to the state of the corresponding DIP switches of the S5 array. Correspondence is established as follows:

- DS15 segment a switch 1
- DS15 segment b switch 2
- DS15 segment c switch 3
- DS15 segment d switch 4
- DS15 segment e switch 5
- DS15 segment f switch 6
- DS15 segment g switch 7
- DS15 digital point switch 8



The third stage sets the LED assigned to the UART and MIDI microprocessors according to the state of push buttons S1 and S2. Correspondence is established as follows:

- S1 DS1 and DS3
- S2 DS2 and DS4

Refer to the demonstration comments for details.

Performing a loopback through the UART interface

UartLoopback.pjt demonstrates how to perform a simple loopback through the UART interface. To execute this demonstration correctly, you must connect the PADK to your computer with a standard serial DB9 cable. The UART connector of the PADK is J3. Refer to *Connecting the PADK through the JTAG interface* in the quick start guide for details.

When the PADK is connected, set up the serial connection of your computer with software such as HyperTerminal, for example. To match the default initialization values of the PADK UART module, the serial connection must be configured as follows:

- Serial port: COMx (depending on the configuration of your computer)
- Baud: 115200
- Data bits: 8
- Parity: None
- Stop bit: 1
- Flow control: None

When the serial connection of your computer is configured and the DSP code is running on the PADK, any character that you type in HyperTerminal should appear in the HyperTerminal window when the host receives it from the PADK.

Refer to the demonstration comments for details.

Performing a USB transfer

UsbGpio.pjt demonstrates how to transfer data between the host computer and the PADK through their USB interfaces. To execute this demonstration correctly, you must connect the PADK to your computer with the Hi-speed USB cable supplied with the PADK and that the USB drivers are correctly installed. Refer to *Installing USB device drivers* in the quick start guide for details.

When the PADK is connected, compile the host application you find under the *Windows* folder.

When the host application and the DSP code is running on PADK, you should see the communication there are between the host application and the PADK by pressing on the switch 1 - 2 on the PADK and changing the number on the host application.

Digital audio examples

Performing a digital audio loopback in polling mode

DigitalLoopbackPolling.pjt demonstrates how to perform digital audio loopback in polling mode with the PADK. The sampling rate is set at 48 kHz. The sampling frequency source is configured with the CLKGEN module of the PADK library.

The data received on the RCA input channel is sent to the optical and the RCA output channels:

RCA IN to RCA OUT
 to OPTICAL OUT

The DIR is initialized with the PADK library functions. The device is connected to the DSP through McASP 1 serializer 0. Both input signals, optical and S/PDIF, are connected to the DIR and can be selected as the source of the digital signal with a PADK library function. In this demonstration, the input is the RCA input. The DSP McASP 2 is used to perform to transmit the digital signal. This module of the C672x DSP is used in DIT mode to transmit digitized S/PDIF data through its 0 and 1 serializers. Serializer 0 is used to transmit to the RCA output, while serializer 1 is connected to the optical output.

Performing a digital audio loopback

DigitalLoopback.pjt demonstrates how to perform digital audio loopback with the PADK. The sampling rate is set at 48 kHz. The sampling frequency source is configured with the CLKGEN module of the PADK library.

The data received on the RCA input channel is sent to the optical and the RCA output channels:

```
RCA IN      to RCA OUT
            to OPTICAL OUT
```

The DIR is initialized with the PADK library functions. The device is connected to the DSP through McASP 1 serializer 0. Both input signals, optical and S/PDIF, are connected to the DIR and can be selected as the source of the digital signal with a PADK library function. In this demonstration, the input is the S/PDIF input. The DSP McASP 2 is used to perform to transmit the digital signal. This module of the C672x DSP is used in DIT mode to transmit digitized S/PDIF data through its 0 and 1 serializers. Serializer 0 is used to transmit to the RCA output, while serializer 1 is connected to the optical output.

The McASP and the dMAX are initialized with the Texas Instruments CSL library. The dMAX is used to sort the input data from the DIR into a separate buffer for each stereo channel (left and right buffers). The same organization is used for the DIT output data.

```
DIR left sample 0
DIR left sample 1
...
DIR left sample n-1
DIR left sample n
...
DIR right sample 0
DIR right sample 1
...
DIR right sample n-1
DIR right sample n
```

Refer to the demonstration comments for details.

Analog audio examples

Performing an analog audio loopback in polling mode

AnalogLoopbackPolling.pjt demonstrates how to perform analog audio loopback in polling mode with the PADK. The sampling rate is set at 96 kHz. The sampling frequency source is configured with the CLKGEN module of the PADK library.

Each ADC channel is then sent to its corresponding DAC channel:

- ADC 1 to DAC 1
- ADC 2 to DAC 2
- ADC 3 to DAC 3
- ADC 4 to DAC 4

The ADC and the DAC are initialized with the PADK library functions. The devices are connected to the DSP through the McASP 0 serializers.

- ADC 1 to McASP 0 serializer 0 (AXR0_0)
- ADC 2 to McASP 0 serializer 1 (AXR0_1)
- ADC 3 to McASP 0 serializer 2 (AXR0_2)
- ADC 4 to McASP 0 serializer 3 (AXR0_3)
- DAC 1 to McASP 0 serializer 4 (AXR0_4)
- DAC 2 to McASP 0 serializer 5 (AXR0_5)
- DAC 3 to McASP 0 serializer 6 (AXR0_6)
- DAC 4 to McASP 0 serializer 7 (AXR0_7)

Refer to the demonstration comments for details.

Performing an analog audio loopback

AnalogLoopback.pjt demonstrates how to perform analog audio loopback with the PADK. The sampling rate is set at 96 kHz. The sampling frequency source is configured with the CLKGEN module of the PADK library.

Each ADC channel is then sent to its corresponding DAC channel:

- ADC 1 to DAC 1
- ADC 2 to DAC 2
- ADC 3 to DAC 3
- ADC 4 to DAC 4

The ADC and the DAC are initialized with the PADK library functions. The devices are connected to the DSP through the McASP 0 serializers.

- ADC 1 to McASP 0 serializer 0 (AXR0_0)
- ADC 2 to McASP 0 serializer 1 (AXR0_1)
- ADC 3 to McASP 0 serializer 2 (AXR0_2)
- ADC 4 to McASP 0 serializer 3 (AXR0_3)
- DAC 1 to McASP 0 serializer 4 (AXR0_4)
- DAC 2 to McASP 0 serializer 5 (AXR0_5)
- DAC 3 to McASP 0 serializer 6 (AXR0_6)
- DAC 4 to McASP 0 serializer 7 (AXR0_7)

The McASP and the dMAX are initialized with the Texas Instruments CSL library. The dMAX is used to sort the input data from the ADC into a separate buffer for each stereo channel (left and right buffers). The same organization is used for the DAC output data.

ADC 0 left sample 0

ADC 0 left sample 1

...

ADC 0 left sample n-1

ADC 0 left sample n

ADC 1 left sample 0

ADC 1 left sample 1

...

ADC 1 left sample n-1

ADC 1 left sample n

ADC 2 left sample 0

ADC 2 left sample 1

...

ADC 2 left sample n-1

ADC 2 left sample n

ADC 3 left sample 0

ADC 3 left sample 1

...

ADC 3 left sample n-1

ADC 3 left sample n

Refer to the demonstration comments for details.

Processing simple audio effects

SimpleAudioEffect.pjt demonstrates how to process a simple audio effect on an acquired analog signal with the PADK. A panning effect is added to the standard analog loopback demonstration. The sampling rate is set at 96 kHz. The sampling frequency source is configured with the CLKGEN module of the PADK library.

Each ADC channel is then sent to its corresponding DAC channel:

- ADC 1 to DAC 1
- ADC 2 to DAC 2
- ADC 3 to DAC 3
- ADC 4 to DAC 4

The ADC and the DAC are initialized with the PADK library functions. The devices are connected to the DSP through the McASP 0 serializers.

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- ADC 1 to McASP 0 serializer 0 (AXR0_0)
- ADC 2 to McASP 0 serializer 1 (AXR0_1)
- ADC 3 to McASP 0 serializer 2 (AXR0_2)
- ADC 4 to McASP 0 serializer 3 (AXR0_3)
- DAC 1 to McASP 0 serializer 4 (AXR0_4)
- DAC 2 to McASP 0 serializer 5 (AXR0_5)
- DAC 3 to McASP 0 serializer 6 (AXR0_6)
- DAC 4 to McASP 0 serializer 7 (AXR0_7)

The McASP and the dMAX are initialized with the Texas Instruments CSL library. The dMAX is used to sort the input data from the ADC into a separate buffer for each stereo channel (left and right buffers). The same organization is used for the DAC output data.

ADC 0 left sample 0

ADC 0 left sample 1

...

ADC 0 left sample n-1

ADC 0 left sample n

ADC 1 left sample 0

ADC 1 left sample 1

...

ADC 1 left sample n-1

ADC 1 left sample n

ADC 2 left sample 0

ADC 2 left sample 1

...

ADC 2 left sample n-1

ADC 2 left sample n

ADC 3 left sample 0

ADC 3 left sample 1

...

ADC 3 left sample n-1

ADC 3 left sample n

Refer to the demonstration comments for details.

Using dMAX

DmaxDelayLinesEffect.pjt demonstrates how to use the outstanding capabilities of dMAX, such as delay lines, not normally used in other applications. They can be used to apply audio effects on analog signals acquired by the PADK, for example. This example adds a panning effect to the standard analog loopback example. See section [Performing an analog audio loopback](#) for details.

The sampling rate of the example is set to 96 kHz. It is generated by the onboard oscillator. The sampling frequency source is configured with the CLKGEN module of the PADK library.

Each ADC channel is then sent to its corresponding DAC channel:

- ADC 1 to DAC 1
- ADC 2 to DAC 2
- ADC 3 to DAC 3
- ADC 4 to DAC 4

The ADC and the DAC are initialized with the PADK library functions. The devices are connected to the DSP through the McASP 0 serializers.

- ADC 1 to McASP0 serializer 0 (AXR0_0)
- ADC 2 to McASP0 serializer 1 (AXR0_1)
- ADC 3 to McASP0 serializer 2 (AXR0_2)
- ADC 4 to McASP0 serializer 3 (AXR0_3)
- DAC 1 to McASP0 serializer 4 (AXR0_4)
- DAC 2 to McASP0 serializer 5 (AXR0_5)
- DAC 3 to McASP0 serializer 6 (AXR0_6)
- DAC 4 to McASP0 serializer 10 (AXR0_10)

The McASP and the dMAX are initialized with the Texas Instruments CSL library. The dMAX is used to sort the input data from the ADC into a separate buffer for each stereo channel (left and right buffers). The same organization is used for the DAC output data.

ADC 0 left sample 0

ADC 0 left sample 1

...

ADC 0 left sample n-1

ADC 0 left sample n

ADC 1 left sample 0

ADC 1 left sample 1

...

ADC 1 left sample n-1

ADC 2 left sample n

ADC 2 left sample 0

ADC 2 left sample 1

...

ADC 2 left sample n-1

ADC 2 left sample n

ADC 3 left sample 0

ADC 3 left sample 1

...

ADC 3 left sample n-1

ADC 3 left sample n

Refer to the demonstration comments for details.

Embedding a DSP application in the flash memory

...*PADK\Flash\Makerom* contains all the application and the tools necessary to write an application in the flash memory of the PADK. No restrictions apply to applications that you may write to the flash memory, except that the size of all the initialized sections must be less than that of the flash memory — that is, 16 MB. Proceed as follows.

1. Copy the *.out* file of a working application to the **Makerom** folder.
2. Run *MakeRom.exe Updater.out* <application_name> in a command shell.
This creates a file named *FLASH_<application_name>.out*.
3. Use Code Composer Studio to upload and run this file on the PADK.
4. Make sure that the PADK is set to boot from the flash memory.
5. Reset the PADK to run the programmed application.

Files in the Makerom folder

Loader.out

This file is the first-stage loader. When the board is reset, the EDMA copies this file to internal memory and runs it. *Loader.out* initializes the EMIF and the PLL, and then copies all the initialized memory sections of the application programmed in the flash memory to their appropriate locations. The loader then jumps to the application entry point. The source files to build this executable file are not supplied with the PADK.

Updater.out

This file reads a data vector from the SDRAM and writes it to the flash memory of the PADK. The length of the data to be programmed must be written in the SDRAM at address 0x80000000. The data to be programmed must follow at address 0x80000004. The source files to build this executable file are not supplied with the PADK.

MakeRom.exe

This Win32 application combines *Loader.out*, *Updater.out*, and the application to be programmed to create a DSP executable (*.out*) that can run in a CCS environment and can be used to write a user application in the flash memory of the PADK. This file is named *FLASH_<application name>.out*. The source files to build this executable file are not supplied with the PADK.

Downloading an application without a JTAG emulator

USB loader

...\PADK\Host\PADK_UsbLoader contains a program used to download applications through the USB port. The interface is very simple and self explanatory.

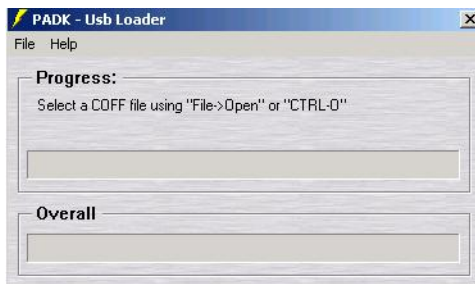


Figure 4 USB loader interface

1. On the **File** menu, click **Open** to open a COFF file.
Alternately, you can press CTRL + O on your keyboard.
2. On the **File** menu, click **Download** to download the opened COFF file.
Alternately, you can press CTRL + D on your keyboard.

Note

The DSP USB loader must be in the PADK flash memory before you can proceed. See [Embedding a DSP application in the flash memory](#) for details.

Demonstrations

Audio Streaming and Wavetable Solution demonstration

Audio Streaming and Wavetable Solution is installed on your computer when you copy the PADK software, as described in the quick start guide. To run the demonstration:

- ◆ On the Windows **Start** menu, point to **Programs, Lyrtech, PADK, Demos, Wavetable**, and then click **WavetableCS**.

The Audio Streaming and Wavetable Solution demonstration starts.

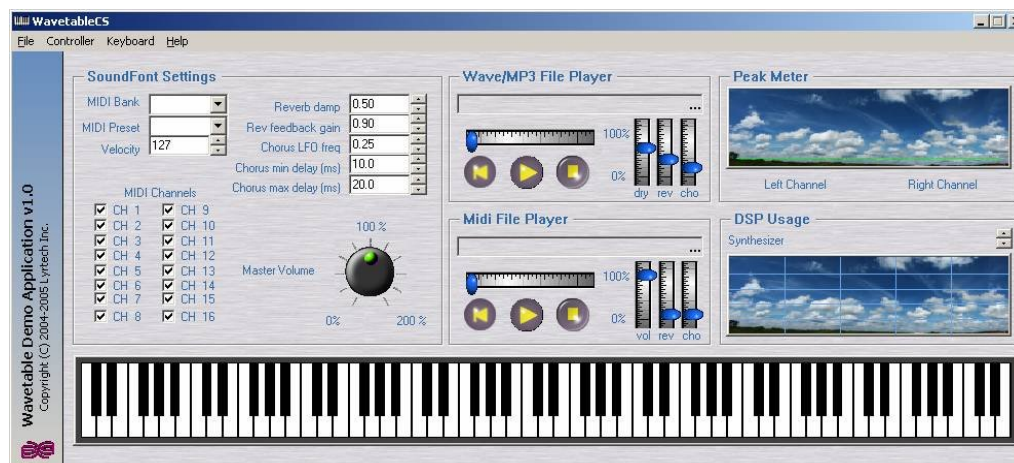


Figure 5 Audio Streaming and Wavetable Solution interface

This demonstration explores the various features of the PADK involving MIDI and MP3 technology. The demonstration allows you to play back MIDI files and 44.1-kHz MP3 files, and add special effects to them, such as chorus and reverberation. You may also use the piano keyboard with your mouse or connect a MIDI-compatible keyboard to the PADK MIDI connector.

Note

Lyrtech does not supply any audio files for the demonstration. It is the responsibility of the customer to purchase sounds libraries, such as those developed by Sonic Implants, or any other type of supported file. See [Supported file types](#) for details about file supported by the PADK. Also note that if the USB loader is not resident in the flash memory of the PADK, the demonstration does not work. See [Embedding a DSP application in the flash memory](#) for details.

Running the MP3/Reverb demonstration

MP3/Reverb is installed on your computer when you copy the PADK software, as described in the quick start guide. To run the demonstration:

- ◆ On the Windows **Start** menu, point to **Programs, Lyrtech, PADK, Demos, Mp3Reverb**, and then click **PADK_Mp3Reverb**.

The MP3/Reverb demonstration starts.

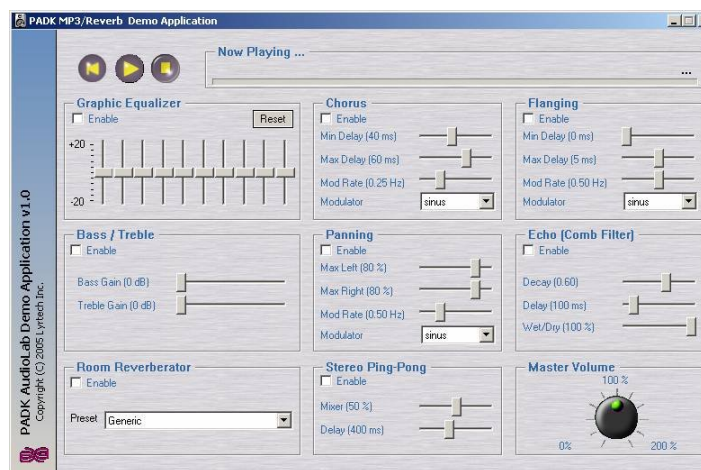


Figure 6 MP3/Reverb interface

This demonstration explores the various features of the PADK involving MP3 technology. The demonstration allows you to play back 44.1-kHz MP3 files and adjust audio preferences with a graphic equalizer, as well as mix special effects such as chorus, flanging, bass and treble, panning, echo, room reverberation, and Stereo ping-pong.

Note

If the USB loader is not resident in the flash memory of the PADK, the demonstration does not work. See [Embedding a DSP application in the flash memory](#) for details.

Specifications

This chapter presents the main specifications of the PADK.

Dimensions

245.0 mm × 50.0 mm × 192.0 mm (width × height × depth)

(9.65 in. × 1.97 in. × 7.56 in.)

Mass

761.82 g (26.87 oz.)

Operational temperature range

10°C to 40°C (50°F to 104°F)

Storage temperature range

−10°C to 50°C (14°F to 122°F)

Power consumption

Minimum: 1.0 A (5 W)

Typical: 2.4 A (12 W)

Analog input specifications

Audio Precision

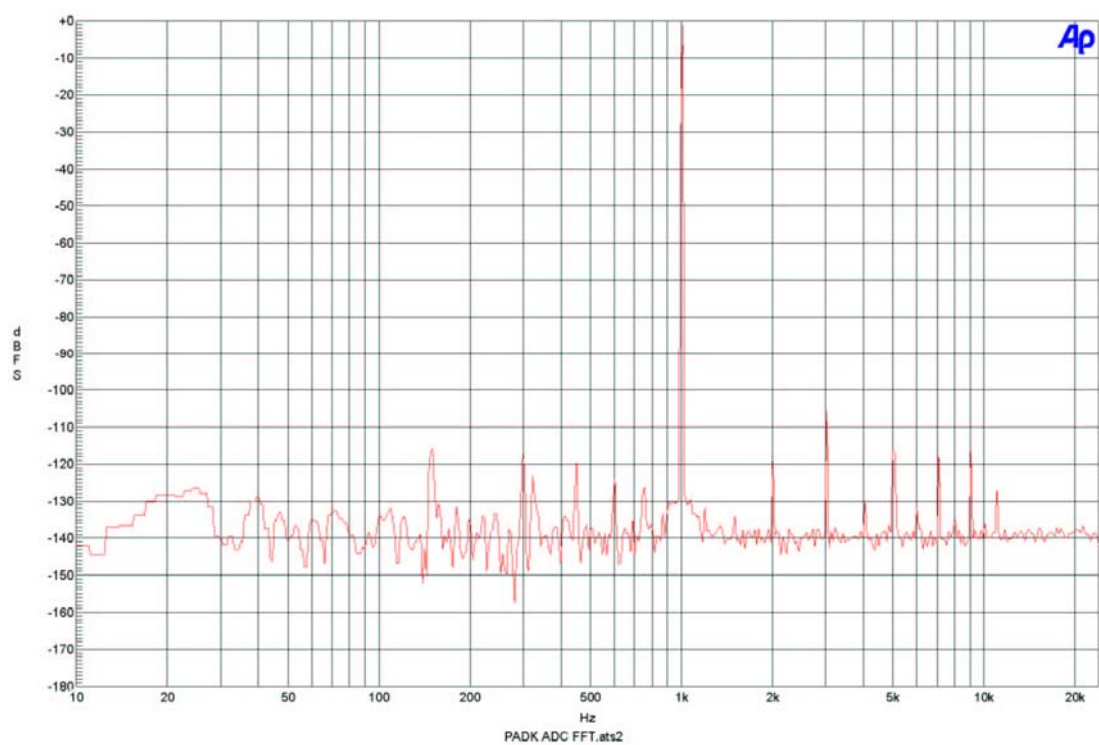


Figure 7 Analog input FFT plot

Audio Precision

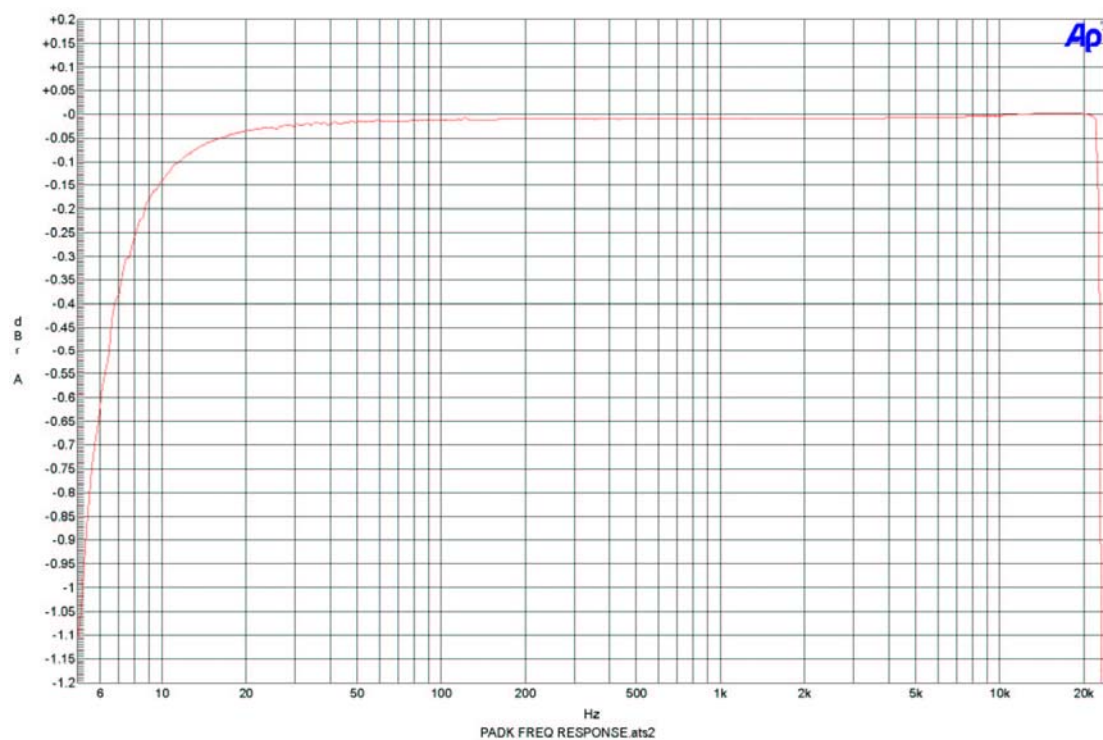


Figure 8 Analog input passband $F_s=48$ kHz

Audio Precision

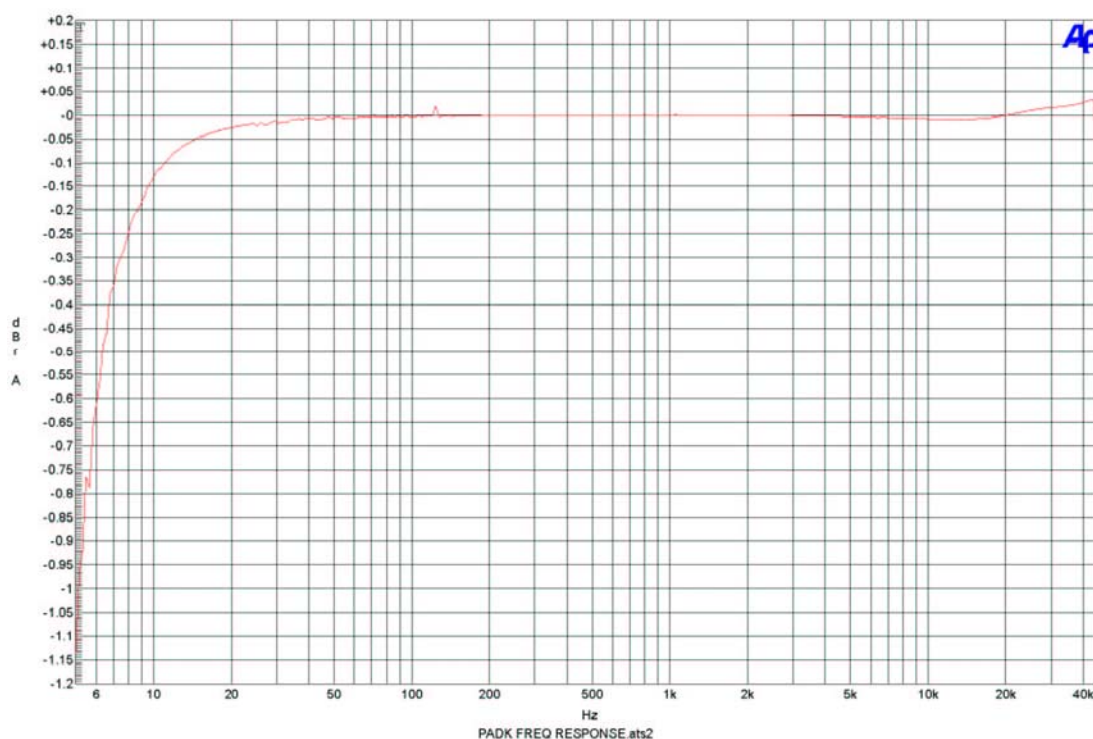
Figure 9 Analog input passband $F_s=96$ kHz

Table 1 Analog input specification summary

Parameter	Test condition	Analog input			Units
		Min	Typical	Max	
Passband ± 0.1 dB	48 kHz	13		22300	Hz
Passband ± 0.1 dB	96 kHz	13		44800	Hz
THD+N	$V = -0.5$ dBFS, $f = 1$ kHz, $F_s = 48$ kHz		-101	-96	dB
THD+N	$V = -6$ dBFS, $f = 1$ kHz, $F_s = 48$ kHz		-99	-94	dB
SNR		-106	-104	-100	dB
Channel separation			80		dB
Full-scale input			7		V _{pp}
Full-scale input			9.8		dBm

Notes

- The performance is measured using an Audio Precision ATS-2 audio test system. The bandwidth is limited with a 20 kHz low-pass filter. The measurements are made with the RMS detector selected.
- Typical values are obtained by averaging the results from eight channels.

Analog output specifications

Audio Precision

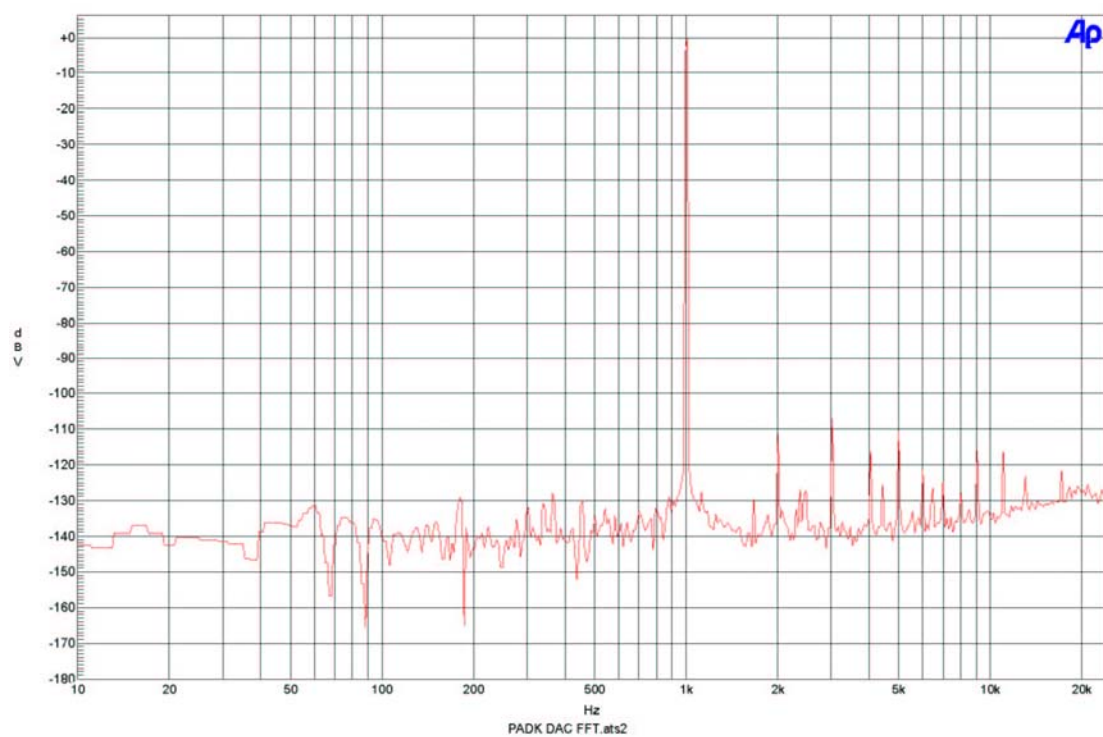


Figure 10 Analog output FFT plot

Audio Precision

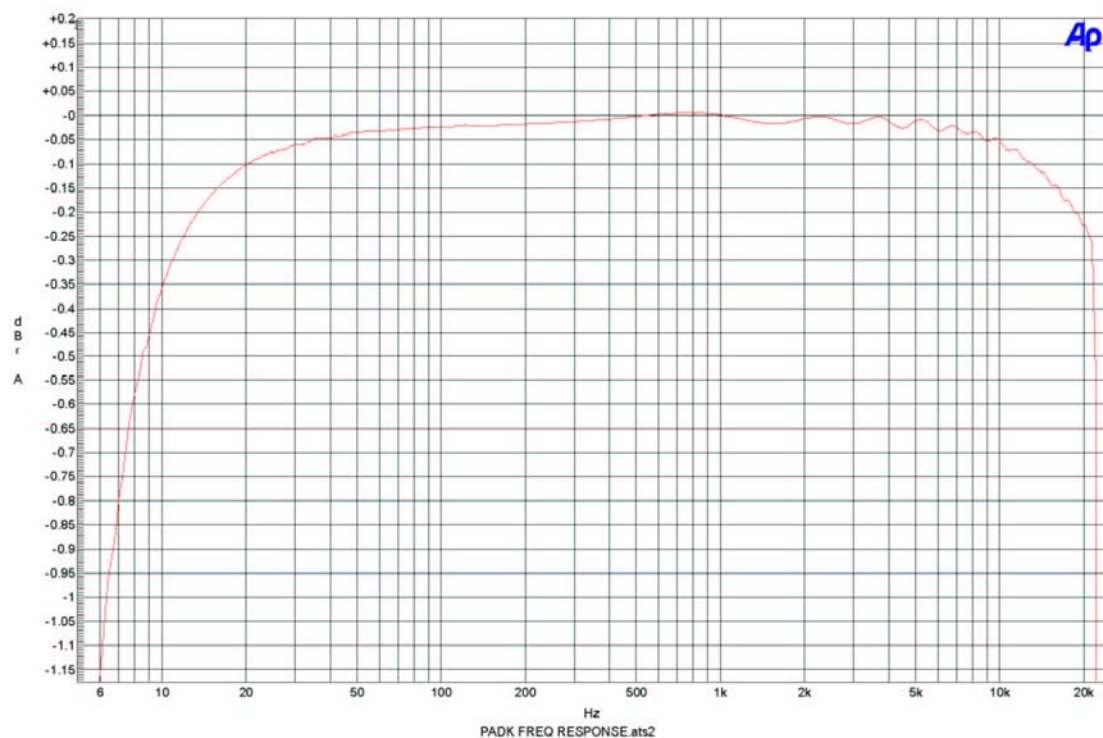


Figure 11 Analog output passband $F_s=48$ kHz

Audio Precision

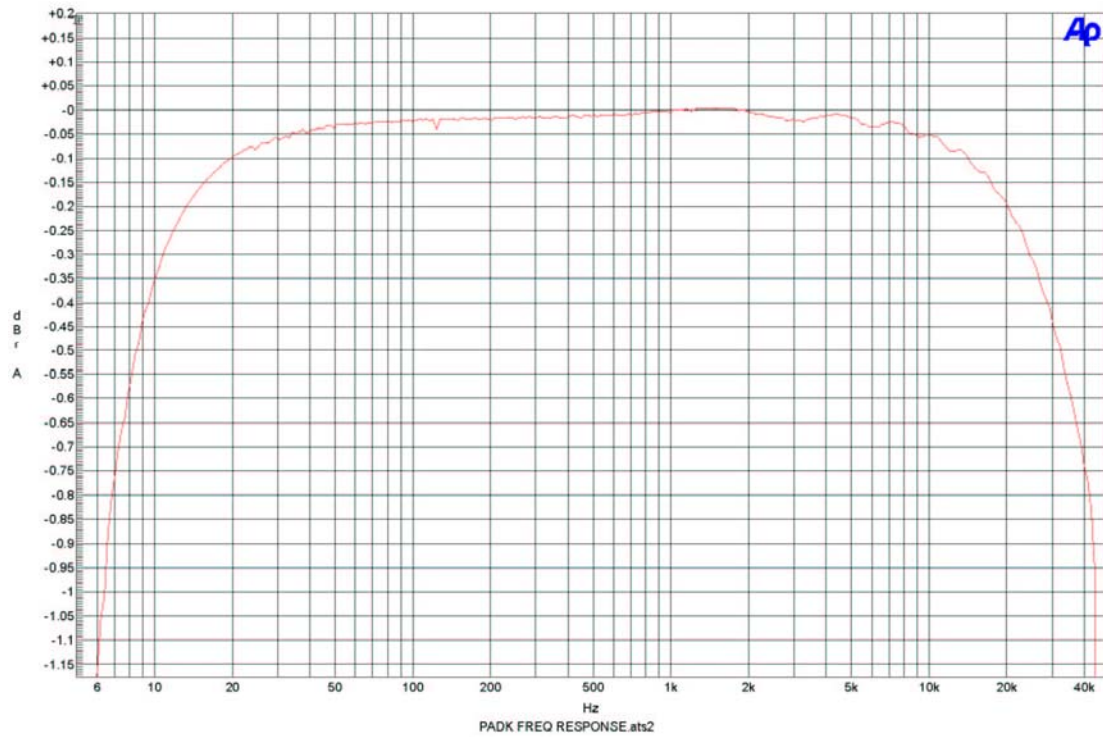
Figure 12 Analog output passband $F_s=96$ kHz

Table 2 Analog output specification summary

Parameter	Test condition	Analog input			Units
		Min	Typical	Max	
Passband ± 0.8 dB	48 kHz	7		22100	Hz
Passband ± 0.8 dB	96 kHz	7		41800	Hz
THD+N	$V = -0.5$ dBFS, $f = 1$ kHz, $F_s = 48$ kHz		-100	-96	dB
THD+N	$V = -6$ dBFS, $f = 1$ kHz, $F_s = 48$ kHz		-100	-98	dB
SNR		-102	-105		dB
Channel separation			-101	-98	dB
Full-scale output			3.1		V _{pp}
Full-scale output			3.0		dBm

Hardware specifications

Table 3 Hardware specifications

Item	Description
SDRAM	128 MB
Flash memory	8 MB
I ² C EEPROM	64 kilobits
SPI EEPROM	64 kilobits

For more hardware specifications, refer to the PADK technical reference guide.

Connector summary

Table 4 Connector summary

Connector	Description
J1	USB type B connector to connect to PC USB port.
J2	Female DB9 connector to connect to MIDI interface.
J3	Female DB9 connector to connect to PC serial RS-232 port.
J4	BNC connector to output sampling rate clock from SRC.
J5	BNC connector to pass through input from J6.
J6	BNC connector to input the word clock.
J7	DC +5 V input power jack.
J8	DSK memory 80-pin connector header.
J9	DSK HPI 80-pin connector header.
J10	DSK peripheral 80-pin connector header.
J11	S/PDIF digital input RCA jack.
J12	S/PDIF digital output RCA jack.
J13	ADC input 1 and 2 stereo RCA jack.
J14	ADC input 3 and 4 stereo RCA jack.
J15	ADC input 5 and 6 stereo RCA jack.
J16	ADC input 7 and 8 stereo RCA jack.
J17	DAC output 1 and 2 stereo RCA jack.
J18	DAC output 3 and 4 stereo RCA jack.
J19	DAC output 5 and 6 stereo RCA jack.
J20	DAC output 7 and 8 stereo RCA jack.
JP1	USB I ² C 3-pin header (to program USB identification EEPROM).
P1	DSP JTAG 14-pin header.
P2	DSP I ² C 4-pin header (to test all I ² C devices connected to DSP).
P3	FPGA JTAG 6-pin header (to program FPGA configuration EEPROM).

Jumper summary

Table 5 Jumper summary

Jumper	Description
JP2	Analog 1 input range selector.
JP3	Analog 2 input range selector.
JP6 JP7 JP8 JP10	DSP boot mode.
JP9	SPI EEPROM write-protect.
JP11	Source selector for DSP McASP signals AHCLKR0, AHCLKX0, AHCLKR2, and AHCLKX1.
JP12	Source selector for DSP McASP signals DSP_AXR0[7:9] DSP_AXR1[0].
JP13	Source selector for DSP McASP signals DSP_AXR0[0:3].

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