

# Hardware Issue

## Ethernet PHYs

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## Index

1	Introduction.....	3
1.1	Scope .....	3
1.2	Referenced documents.....	3
2	Test Setup .....	4
3	Test results.....	5
3.1	Correct Ping Request.....	5
3.2	Corrupted Ping Request Echo .....	5
3.3	Correct Ping Reply.....	6
3.4	Corrupted Ping Reply Echo.....	6
4	Schematics .....	9
4.1	Link 1.....	9
4.2	Link 2.....	10
5	Conclusions .....	10

## Index of figures

Figure 1:	Ping reply – D0 path.....	7
Figure 2:	Ping reply – D1 path.....	7
Figure 3:	Ping reply – data setup .....	8
Figure 4:	Ping reply – data hold .....	8

## Index of tables

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## Revision table

Revision	Date	Author	Changes
00	04/08/2017	Eletech	First Release

# 1 Introduction

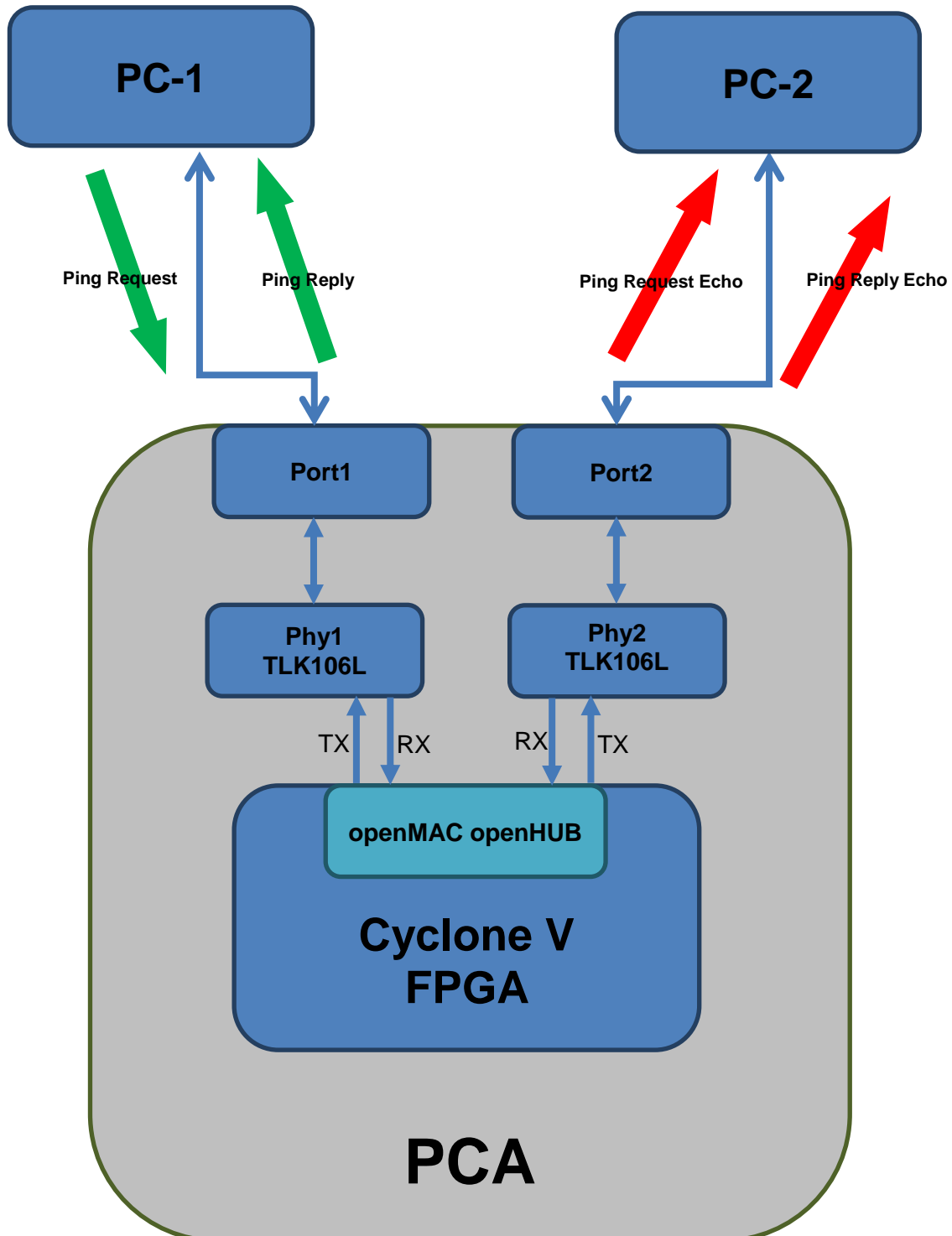
## 1.1 Scope

Scope of this document is the analysis of the communication problems on the ethernet interfaces equipped with the TLK106L (TLK106LRHBT) phy transceivers from Texas Instruments.

## 1.2 Referenced documents

Name	Description	Version	Author
[1]			
[2]			

## 2 Test Setup



Ping request from PC-1(using Linux terminal) connected to Port1.  
 PC-1 send the ping request and receive the corresponding reply from the openMAC/openHUB core implemented in FPGA.  
 PC-2 receive the echoes of every ping requests and replies.

Traffic passing through the ethernet network is sniffed by both PC-1 and PC-2 using Wireshark. Signals of the TX and RX interfaces between FPGA and phys are monitored with a Lecroy Wave-runner 6200A oscilloscope.

### 3 Test results

Every ping request has a corresponding correct ping reply from Port1, no packets are lost during the test.

Some messages (ping requests or replies) from Port2 are not correctly received and recognized by PC-2.

Ethernet data packets seems malformed or corrupted as shown in the following wireshark traces.

#### 3.1 Correct Ping Request

```
No.    Time    Source          Destination      Protocol Length Info
 2985 2284.016001 192.168.100.40 192.168.100.1   ICMP      98    Echo (ping) request id=0x0a4c, seq=1318/9733, ttl=64
```

```
Frame 2985: 98 bytes on wire (784 bits), 98 bytes captured (784 bits)
Ethernet II, Src: Giga-Byt_13:f2:12 (00:1f:d0:13:f2:12), Dst: MS-NLB-PhysServer-18_34:ca:fe:01 (02:12:34:ca:fe:01)
Internet Protocol Version 4, Src: 192.168.100.40 (192.168.100.40), Dst: 192.168.100.1 (192.168.100.1)
Internet Control Message Protocol
```

```
0000 02 12 34 ca fe 01 00 1f d0 13 f2 12 08 00 45 00  ..4.....E.
0010 00 54 00 00 40 00 40 01 f1 2e c0 a8 64 28 c0 a8  .T.@.@....d(.
0020 64 01 08 00 76 8f 0a 4c 05 26 a5 30 84 59 00 00  d...v..L.&.0.Y..
0030 00 00 7e a1 0b 00 00 00 00 10 11 12 13 14 15  ..~:.....
0040 16 17 18 19 1a 1b 1c 1d 1e 1f 20 21 22 23 24 25  .....!""#$%
0050 26 27 28 29 2a 2b 2c 2d 2e 2f 30 31 32 33 34 35  &'()*+,-./012345
0060 36 37                                     67
```

#### 3.2 Corrupted Ping Request Echo

```
No.    Time    Source          Destination      Protocol Length Info
 2985 2288.007626 ChengduL_a3:fe:11 Optex_33:21:2f 0x8000 98  Ethernet II
```

```
Frame 2985: 98 bytes on wire (784 bits), 98 bytes captured (784 bits) on interface 0
Ethernet II, Src: ChengduL_a3:fe:11 (01:22:44:a3:fe:11), Dst: Optex_33:21:2f (00:1f:d1:33:21:2f)
Data (84 bytes)
  Data: 40000054050040044001102e028c6a11c0886a280000b08e...
  [Length: 84]
```

```
0000 00 1f d1 33 21 2f 01 22 44 a3 fe 11 80 00 40 00  ...3!/"D.....@.
0010 00 54 05 00 40 04 40 01 10 2e 02 8c 6a 11 c0 88  .T.@.@....j...
0020 6a 28 00 00 b0 8e aa 40 55 27 a9 00 84 98 05 00  j(.....@U'.....
0030 00 00 70 a7 ba 00 00 00 00 10 11 12 31 41 51  ..p.....1AQ
0040 61 77 81 91 11 bb c1 dd ee 1f 21 11 22 33 22 55  aw.....!"3"U
0050 22 72 82 22 2a bb 22 d2 2e 2f 30 11 32 33 43 53  "r."*".../0.23CS
0060 66 77                                     fw
```

### 3.3 Correct Ping Reply

```
No.   Time      Source          Destination      Protocol Length Info
 2662 2004.015607 192.168.100.1   192.168.100.40  ICMP      98    Echo (ping) reply  id=0x0a4c, seq=1248/57348, ttl=64
```

Frame 2662: 98 bytes on wire (784 bits), 98 bytes captured (784 bits)  
 Ethernet II, Src: MS-NLB-PhysServer-18\_34:ca:fe:01 (02:12:34:ca:fe:01), Dst: Giga-Byt\_13:f2:12 (00:1f:d0:13:f2:12)  
 Internet Protocol Version 4, Src: 192.168.100.1 (192.168.100.1), Dst: 192.168.100.40 (192.168.100.40)  
 Internet Control Message Protocol

```
0000 00 1f d0 13 f2 12 02 12 34 ca fe 01 08 00 45 00  .....4....E.
0010 00 54 00 00 40 00 40 01 f1 2e c0 a8 64 01 c0 a8  .T..@.@.....d...
0020 64 28 00 00 80 da 0a 4c 04 e0 8d 2f 84 59 00 00  d(.....L.../..Y..
0030 00 00 94 9d 0b 00 00 00 00 10 11 12 13 14 15  .....
0040 16 17 18 19 1a 1b 1c 1d 1e 1f 20 21 22 23 24 25  ..... !"#$$%
0050 26 27 28 29 2a 2b 2c 2d 2e 2f 30 31 32 33 34 35  &'()*+,-./012345
0060 36 37                                     67
```

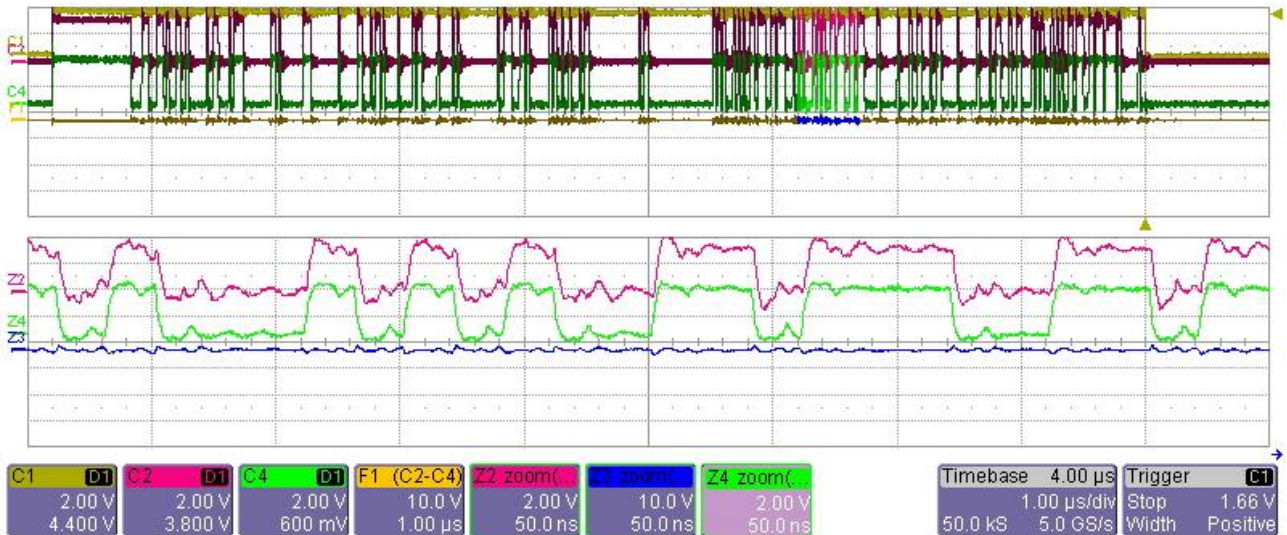
### 3.4 Corrupted Ping Reply Echo

```
No.   Time      Source          Destination      Protocol Length Info
  215 164.002291  MS-NLB-PhysServer-18_34:ec:1f:80 Giga-Byt_13:22:22 0x0850 98 Ethernet II
```

Frame 215: 98 bytes on wire (784 bits), 98 bytes captured (784 bits) on interface 0  
 Ethernet II, Src: MS-NLB-PhysServer-18\_34:ec:1f:80 (02:12:34:ec:1f:80), Dst: Giga-Byt\_13:22:22 (00:1f:d0:13:22:22)  
 Destination: Giga-Byt\_13:22:22 (00:1f:d0:13:22:22)  
 Source: MS-NLB-PhysServer-18\_34:ec:1f:80 (02:12:34:ec:1f:80)  
 Type: Unknown (0x0850)  
 Data (84 bytes)

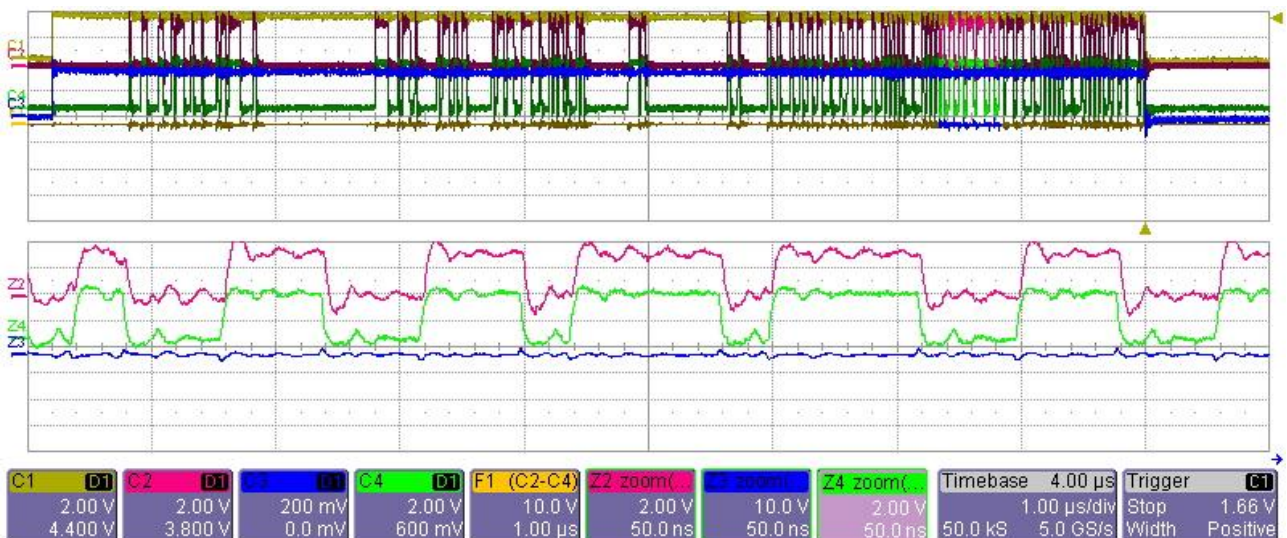
```
0000 00 1f d0 13 22 22 02 12 34 ec 1f 80 08 50 45 00  ....""..4...PE.
0010 40 05 00 00 40 00 10 00 ef 22 c0 aa 14 00 c0 aa  @...@...".
0020 64 28 00 20 62 30 09 0f 00 2c d3 1a 91 59 00 00  d( b0.....Y..
0030 00 00 b7 0f 00 00 00 00 00 11 21 32 11 11 61  .....!2..a
0040 71 11 18 19 1a 1b 1c 11 f1 0f 20 21 32 42 52 25  q..... !2BR%
0050 26 22 22 29 ba c2 d2 e2 f2 22 30 23 33 43 53 33  &(")....."0#3CS3
0060 36 37                                     67
```

Waveforms in Figure 1 and Figure 2 show the TX interface signals between the FPGA and the phys during a corrupted ping reply. Measured data setup and hold times are shown in Figure 3 and Figure 4. Signals on the TX interfaces are the same on both the phys but the Ethernet packet sent from Port2 is corrupted while the Ethernet packet sent from Port1 is correct.



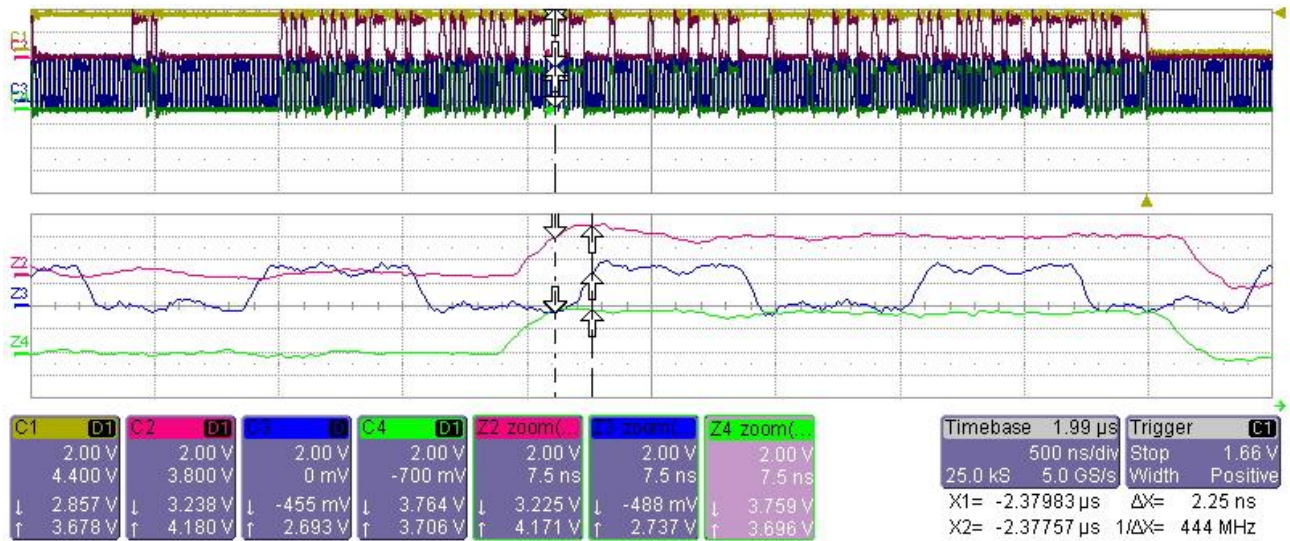
**Figure 1: Ping reply – D0 path**

[Channel1 = TXEN\_1 / Channel2 = TXD0\_1 / Channel3 = TXEN\_2 / Channel4 = TXD0\_2]



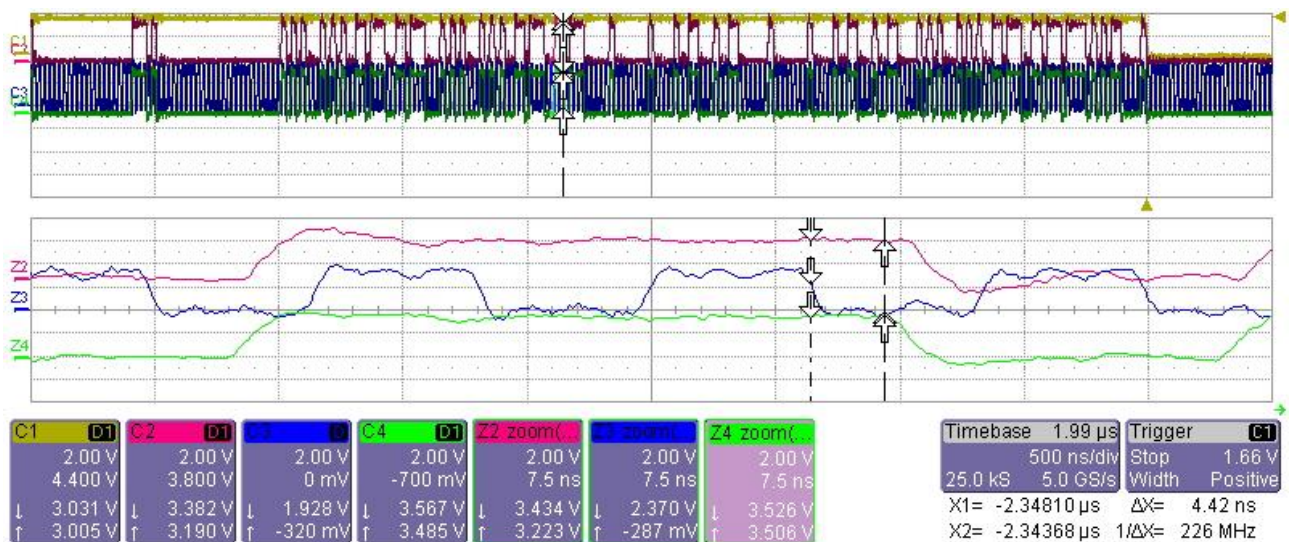
**Figure 2: Ping reply – D1 path**

[Channel1 = TXEN\_1 / Channel2 = TXD1\_1 / Channel3 = TXEN\_2 / Channel4 = TXD1\_2]



**Figure 3: Ping reply – data setup**

[Channel1 = TXEN\_1 / Channel2 = TXD0\_1 / Channel3 = RMIICLK / Channel4 = TXD0\_2]



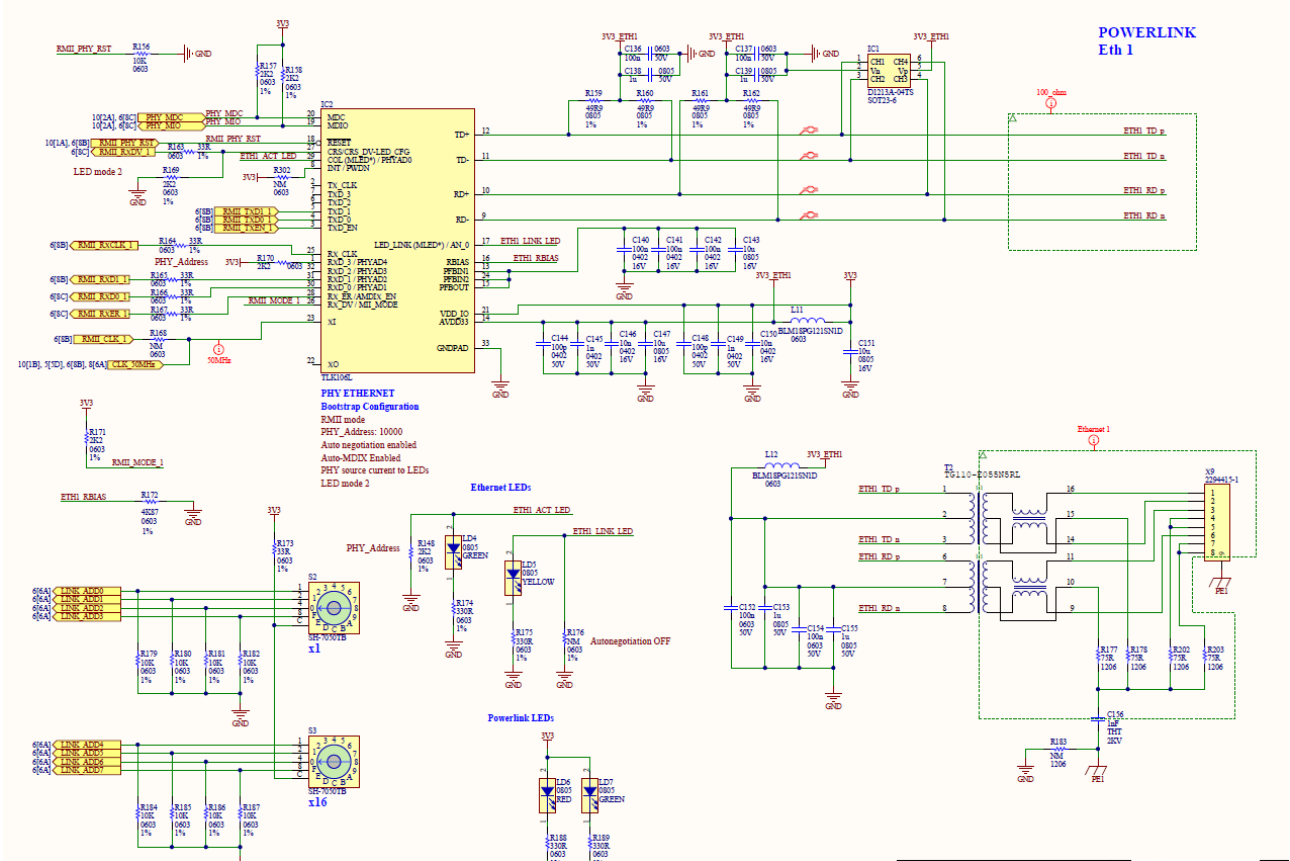
**Figure 4: Ping reply – data hold**

[Channel1 = TXEN\_1 / Channel2 = TXD0\_1 / Channel3 = RMIICLK / Channel4 = TXD0\_2]

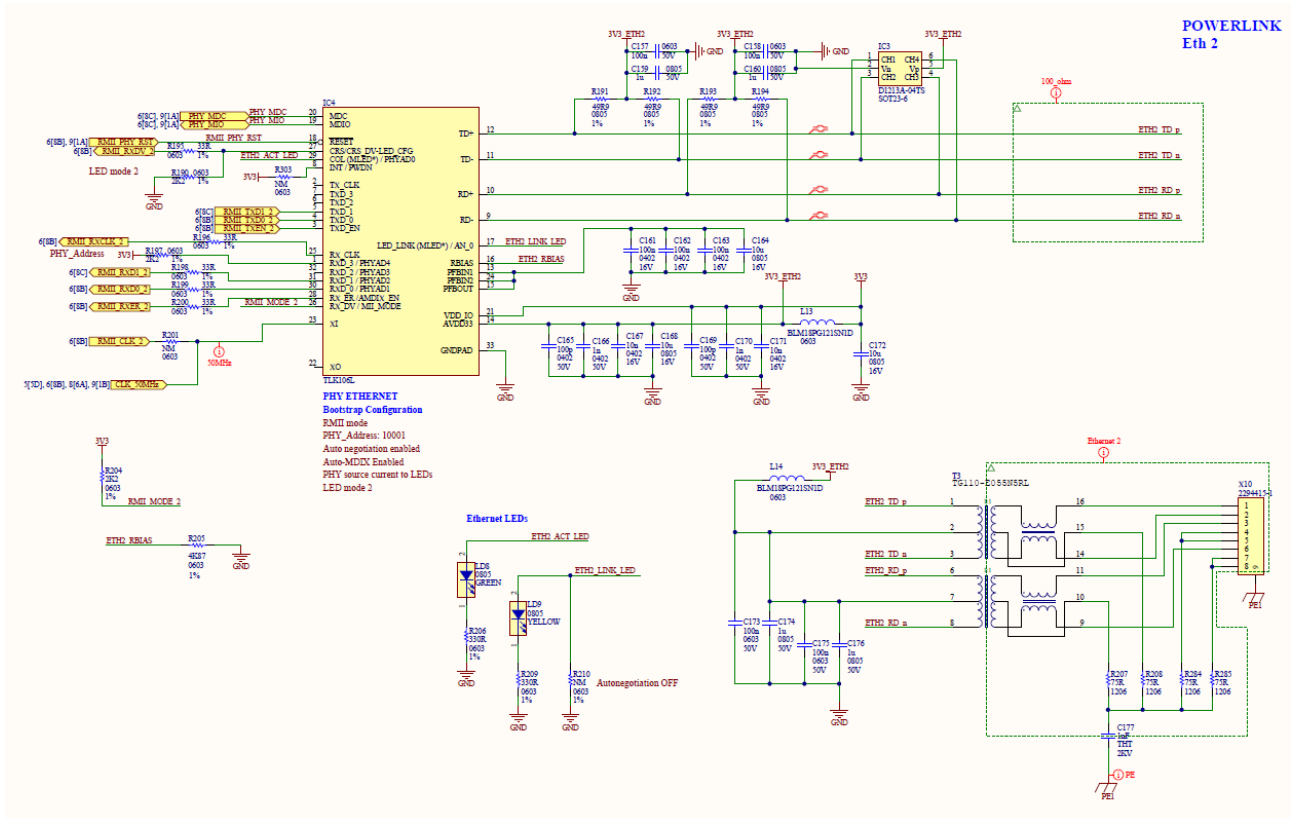


# 4 Schematics

## 4.1 Link 1



## 4.2 Link 2



## 5 Conclusions

A lot of other tests have been done on these interfaces without positive results:

1. Changed Ethernet transformers
2. Changed the driving logic (and the interface timing constraints) inside the FPGA
3. Changed the source of the RMII 50MHz clock (external oscillator source common to FPGA & Phys; clock directly generated from FPGA)
4. Changed the oscillator (from  $\pm 50\text{ppm}$  to  $\pm 20\text{ppm}$ )
5. Exchanged the Phy between the two links

Exchanging the Phys between the two links, the problem “follows” the Phy and seems that it is not related to the surrounding hardware circuits connected to them.

Exchanging the devices between them on a board with Link1 working properly and Link2 failing, results in a board with Link1 failing and Link2 working properly.

**As a consequence, it seems that the Phy does not work properly.**