**Implementation note**

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# *Steps to configure the test mode on the SN65LVDS324*

## 1. Procedure

First of all you must configure the desired output format:

a. Set the active Width by means of the registers:
**FRAME_WIDTH_MSB** (0x0B, bits 4:0) & **FRAME_WIDTH_LSB** (0x0C)

b. Set the active Height by means of the registers:
**FRAME_ HEIGHT_MSB** (0x0D, bits 4:0) & **FRAME_ HEIGHT_LSB** (0x0E)

c. Set the total frame Width by means of the registers:
**TESTMODE_WIDTH_MSB** (0x1F, bits 4:0) & **FRAME TESTMODE_WIDTH_LSB** (0x20)

d. Set the total frame Height by means of the registers:
**TESTMODE_HEIGHT_MSB** (0x21, bits 4:0) & **TESTMODE_ HEIGHT_LSB** (0x22)

Now is precisely to know which output frequency will generate the desired output frame rate.

e. Obtain the output clock frequency you need to generate the desired frame rate:

$$F_{CLKOUT} = TestMode_{Width} * TestMode_{Height} * FrameRate$$

f. Configure **PLL_CFG** (0x0A, bits 1:0) in order to have a valid CLKOUT frequency range, according to the configured mode on **SENSOR_CFG** (0x09, bits 2:0).

> **NOTE:** The output frequency is generated by the input clock (SCLK), multiplied by the PLL block of the device. This PLL multiplier factor (see the PLL_CFG section of the table 3, datasheet page 6) depends on the configured values on **SENSOR_CFG** (0x09, bits 2:0).

g. The input frequency on SCLK you need to generate the desired output video format is given by:

$$F_{SCLK} = \frac{F_{CLKOUT}}{PLL_{multiplier}}$$

h. Enable the test mode by setting **TESTMODE_VIDEO** (0x09, bit 6) to 1.

## 2. Example

Starting by **SENSOR_CFG** (0x09, bits 2:0) is configured as LVDS Parallel 10bpp and the desired output video format is:

- Active area= 1920x1080
- Total frame size= 2250x1100
- Frame Rate = 60 fps

**Procedure:**

a. The active frame width is 1920 (0x0780), therefore

**FRAME_WIDTH_MSB** (0x0B, bits 4:0) = 0x07
**FRAME_WIDTH_LSB** (0x0C) = 0x80

b. The active frame height is 1080 (0x0438), therefore

**FRAME_HEIGHT_MSB** (0x0D, bits 4:0) = 0x04
**FRAME_HEIGHT_LSB** (0x0E) = 0x38

c. The total frame width is 2250 (0x08CA), therefore

**TESTMODE_WIDTH _MSB** (0x1F, bits 4:0) = 0x04
**TESTMODE_WIDTH _LSB** (0x20) = 0x38

d. The total frame height is 1100 (0x044C), therefore

**TESTMODE_ HEIGHT _MSB** (0x21, bits 4:0) = 0x04
**TESTMODE_ HEIGHT _LSB** (0x22) = 0x4C

e. $F_{CLKOUT} = TestMode_{Width} * TestMode_{Height} * FrameRate = 2250 * 1100 * 60 = \mathbf{148.5}\boldsymbol{MHz}$

f. **PLL_CFG** (0x0A, bits 1:0) = 10 (SCLK = 58 to 81MHz, CLKOUT = **116 to 162MHz**).

g. $F_{SCLK} = \frac{F_{CLKOUT}}{PLL_{multiplier}} = \frac{148.5MHz}{2} = \mathbf{74.25}\boldsymbol{MHz}$

h. **TESTMODE_VIDEO** (0x09, bit 6)= 1