PARADE TECHNOLOGIES INC.

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PS8811

USB 3.1 Gen 2 10Gbps Retimer with DCI Support

V1.0

Aug. 14, 2018

KEY FEATURES

- Supports USB 3.1 Gen 2 10Gbps retiming
- Supports USB 3.1 full power management with automatic power saving
- CrystalFree – no external crystal or clock needed
- High input jitter tolerance and low output jitter
- UniEye™ Adaptive Equalizer to compensate channel loss
- Very low latency
- DCI support
- Low power consumption
- Ultra low standby power
- 4.2x4.2 mm 36-pin QFN Halogen free RoHS Package
- 3.3V and 1.2V power supply
- ESD: 7kV Human Body Mode

APPLICATIONS

- Notebook/PCs
- Tablets and mobile devices
- Docking stations and active cables

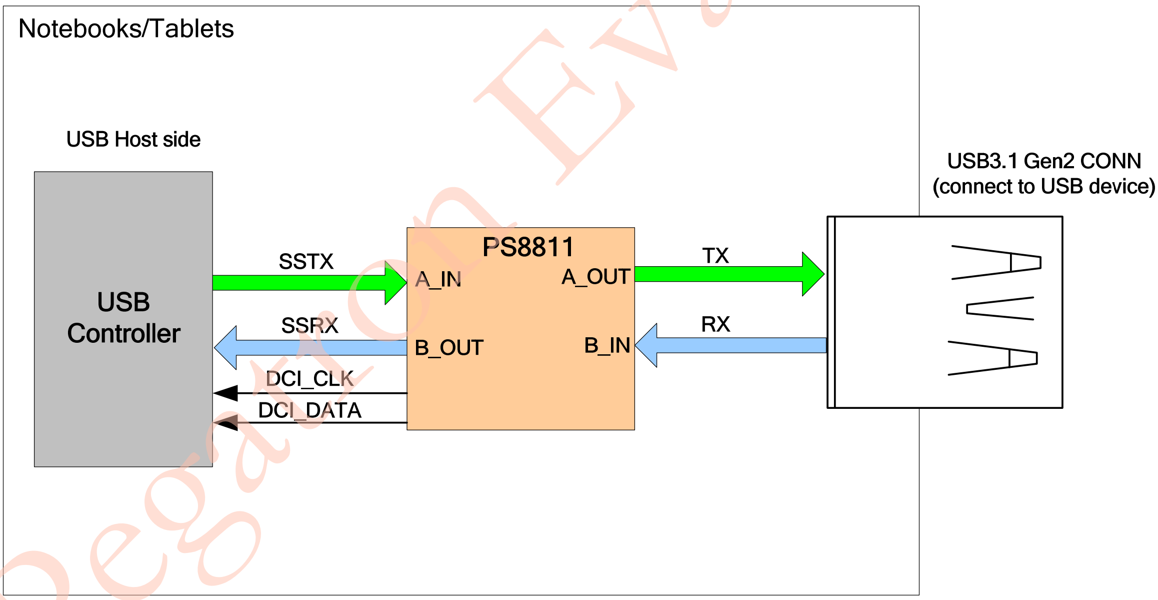

Figure 1. Typical Application

DESCRIPTION

PS8811 is a one-port bidirectional USB 3.1 Gen 2 retimer that integrates the UniEye equalizer and retimer to re-condition USB 3.1 signals for long media link application. It supports USB 3.1 Gen 2 with operation speed up to 10Gbps as well as Gen 1 operation at 5Gbps.

PS8811 supports Intel DCI (Direct Connect Interface) for closed chassis debugging over USB port.

Retiming/Redriving mode for USB3.1

PS8811 supports retiming operation mode for USB3.1. It includes clock and data recovery (CDR) circuit and automatically locks its internal clock to the incoming data by detecting its data stream bit transactions. By removing jitter frequency out of the PLL bandwidth, the CDR circuit reduces the output jitter and allows PS8811 to achieve the excellent jitter performance in retiming mode.

For USB 3.1 Gen 1 and Gen 2 data rates, PS8811 is configured to support retiming for Gen 2 speed and redriving for Gen 1 speed. Gen 1 and Gen 2 speeds are automatically detected.

Receiver Equalization

PS8811 implements equalizers for all USB 3.1 receiving channels, offering outstanding performance for different PCB trace or cable lengths. PS8811 is capable of working for a variety of systems with different input PCB trace and cable conditions, providing signal compensation and regenerating high quality signals with minimal timing jitter.

Programmable Transmitter Equalization

PS8811 supports programmable transmitter equalization for all USB 3.1 output channels. A two-tap Tx equalization (De-emphasis) is used for Gen 1 speed, and a three-tap Tx equalizer including De-emphasis and Pre-shoot is applied for Gen 2 speed.

Automatic Squelch

PS8811 implements automatic squelch circuitry internally, which will drive the output to the common mode voltage when input signals fall below the threshold level at the input of each channel. PS8811 also implements the USB power saving features.

DCI Support

PS8811 has built-in level shifters and supporting circuitry for DCI debugging. Integrator can control DCI_EN pin to enable or disable auto DCI feature for implementation.

Power Management

PS8811 has very low standby power, which is essential to battery-operated devices such as notebooks and tablets.

Power states that PS8811 supports are described below:

- Standby mode

PS8811 enters into standby mode to consume the least power whenever the EN pin is de-asserted.

- Idle mode

Upon assertion of EN signal, PS8811 will exit from standby mode and enter idle mode.

In the idle mode, the USB channels of PS8811 are at Rx.Detect state to check for the existence of a USB 3.1 device, and will exit from idle mode upon successful detection of far-end termination from a USB device.

- USB Sleep mode

At USB link idle(U3 state), when the input signal amplitude on USB channel falls below the squelch threshold level for longer than a pre-defined period, the USB channel will be powered down; thereafter the channel will enter sleep mode. Upon valid signal detection, PS8811's USB channel will go back to the normal operation mode immediately.

- Normal Operation (Active) Mode

In this mode, PS8811 is fully operational.

FUNCTIONAL BLOCK DIAGRAM

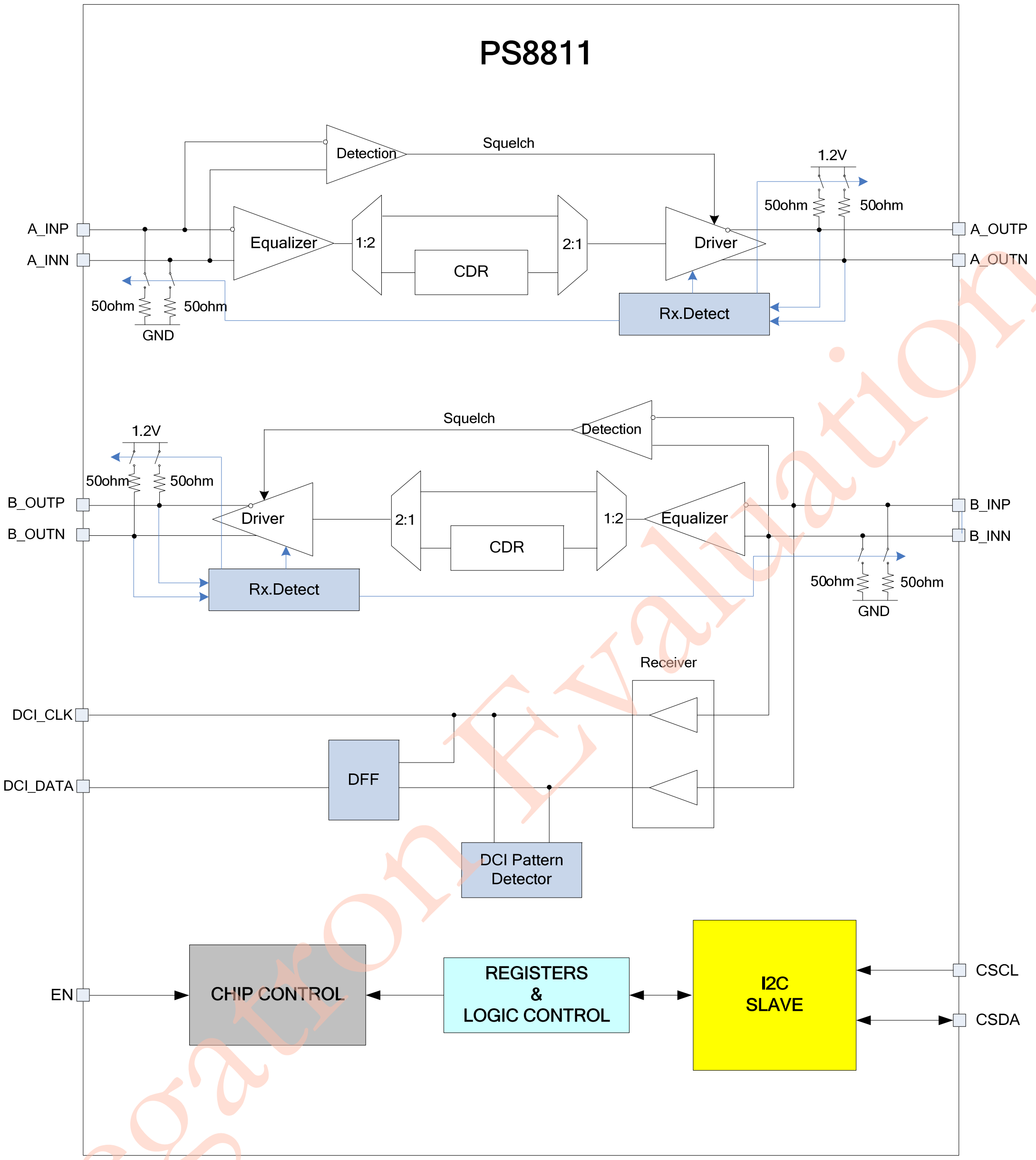

Figure 2. PS8811 Functional Block Diagram

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PIN ASSIGNMENT & DESCRIPTION: PS8811

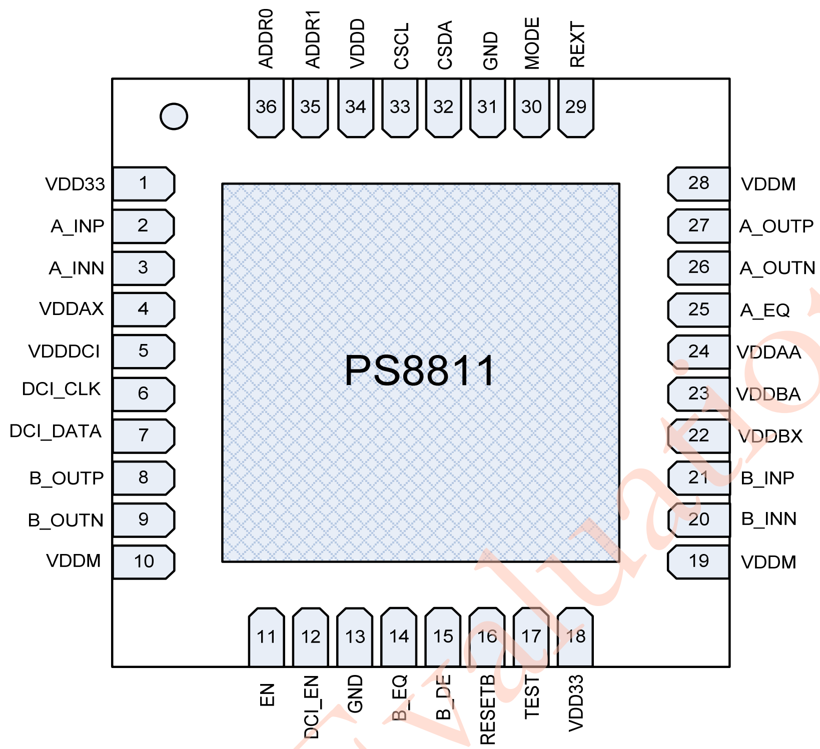


Figure 3. PS8811 Pin Assignment (Top View)

Table 1. PS8811 Pin Descriptions

Pin	Name	I/O	Description
2,3	A_INP A_INN	I	HOST facing port USB SuperSpeed/SuperSpeedPlus differential input
8,9	B_OUTP B_OUTN	O	HOST facing port USB SuperSpeed/SuperSpeedPlus differential output
27,26	A_OUTP A_OUTN	O	Connector facing port USB SuperSpeed/SuperSpeedPlus differential output
21,20	B_INP B_INN	I	Connector facing port USB SuperSpeed/SuperSpeedPlus differential input
11	EN	I	Chip enable, active high, 3.3V input. Internal pull-down at 150kΩ.
29	REXT	I/O	External resistor for output swing adjustment. Connected to a 4.99kΩ resistor for normal output swing.
33,32	CSCL CSDA	I/O	CSCL /CSDA are local I^{2}C control bus: Clock and Data. Open drain structure. 3.3V tolerant. *PS8811 supports I^{2}C operation speed up to 1MHz.*
16	RESET#	I	Reset. Active low, 3.3V input. Internal pull-up at ~100kΩ.
6	DCI_CLK	O	CLK signal output of DCI interface. Tolerant to VDDIO.
7	DCI_DATA	O	DATA signal output of DCI interface. Tolerant to VDDIO.
36,35	ADDR0 ADDR1	I	I^{2}C address setting. Internal pull down at 150kΩ, 3.3V I/O. [ADDR1,ADDR0]= LL: 0x50~0x53 (default) LH: 0x54~0x57 HL: 0xE0~0xE3 HH: 0xE4~0xE7
12	DCI_EN	I	Auto DCI enable or disable control. Internally tied to VDD33/2, 3.3V I/O. L: Disable M: Disable(Default) H: Enable
15	BDE	I	In pin control mode, this pin is used as USB HOST facing Tx channel De-emphasis setting; 3-state input. Internally tied to VDD33/2, 3.3V I/O. L: 0dB M: -3.5dB (default) H: -6.0dB In I2C mode, this pin has higher priority; it should be disabled before register setting.
25	AEQ	I	In Pin Control mode, this pin is used for USB HOST facing Rx channel receiver equalization setting; 3-state input. Internally tied to VDD33/2, 3.3V

			I/O. L: Compensation for channel loss up to 10.5dB M: Compensation for channel loss up to 13dB (default) H: Compensation for channel loss up to 19dB In I2C mode, this pin has higher priority; it should be disabled before register setting.
14	BEQ	I	In Pin Control mode, this pin is used as USB connector facing Rx channel receiver equalization setting; 3-state input. Internally tied to VDD33/2, 3.3V I/O. L: Compensation for channel loss up to 10.5dB M: Compensation for channel loss up to 12dB (default) H: Compensation for channel loss up to 18dB In I2C mode, this pin has higher priority; it should be disabled before register setting.
17	TEST	I	Test Mode control; NC for normal operation
30	MODE	I	Operation mode: L: 5G redriver mode, 10G retimer mode, adaptive EQ. M: 5G redriver mode, 10G retimer mode, fixed EQ (default). H: Reserve
5	VDDDCI	P	Power supply for DCI Interface in a range of 1.8V ~ 3.3V. Connect to VDD33 if DCI is not used.
34	VDDD	P	Connect to external 1.2V power supply
10,19, 28	VDDM	P	Connect to external 1.2V power supply
4	VDDAX	P	Connect to external 1.2V power supply
24	VDDAA	P	Connect to external 1.2V power supply
22	VDDBX	P	Connect to external 1.2V power supply
23	VDDBA	P	Connect to external 1.2V power supply
1,18	VDD33	P	Connect to external 3.3V power supply I/O supply
13,31	GND		Ground
	ePAD		Ground

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Unit
Supply Voltage Range, VDD33		-0.5 V to 3.6 V
Supply Voltage Range, VDD_xx (VDDD, VDDM, VDDAX, VDDAA, VDDBX, VDDBA)		-0.5 V to 1.32 V
Normal I/O Voltage Range		-0.5 V to 3.6 V
ESD	Human Body Mode: Machine Mode: Charged Device Mode:	+/- 7000V +/- 400V +/- 2000V

ESD Standard:

Human Body Model: JS-001-2012

Machine Model: JESD22-A115-C

Charged Device Model: JESD22-C101-E

Latch-up Standard: JESD78D; I-Test: +/- 200mA; V-Test: 1.5X of Vcc

NORMAL OPERATING CONDITIONS AND POWER CONSUMPTION

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage, VDD33		3.0	3.3	3.6	V
Supply Voltage, VDD_xx (VDDD, VDDM, VDDAX, VDDAA, VDDBX, VDDBA)		1.14	1.2	1.26	V
Ambient Temperature, Ta		0		85	°C
Junction Temperature, Tj		0		125	°C
USB Active Mode Normal Supply Current, IDD @ 10Gbps	VDD_xx=1.2V VDD33=3.3V REXT = 4.99KΩ @VDD_xx @VDD33		 306 23	 367 28	 mA mA
USB Sleep Mode Sleep mode Current, I_{sleep} (U3 state)	 @VDD_xx @VDD33		 430 83	 650 125	 uA uA
USB Idle Mode Idle mode Current, I_{idle} (Far end termination removed)	 @VDD_xx @VDD33		 1.0 0.2	 2.0 0.5	 mA mA
Standby Mode Standby Current, I_{stdby} (EN=L)	 @VDD_xx @VDD33		 0.1 3.2	 1.0 5.0	 uA uA
Power Consumption USB Active Mode			 443	 533	 mW
Power Consumption USB Sleep Mode USB Idle Mode			 0.8 1.9	 1.2 4.1	 mW mW
Power Consumption Standby Mode				 18	 uW

PACKAGE DISSIPATION RATING

36-pin QFN	Still air, 4-layer PCB
θ_{JA} – Junction to Ambient Thermal Resistance	45°C/W
θ_{JC} – Junction to Case Thermal Resistance	25°C/W
Maximum Power Dissipation Rating, Ta = 85 °C	889mW

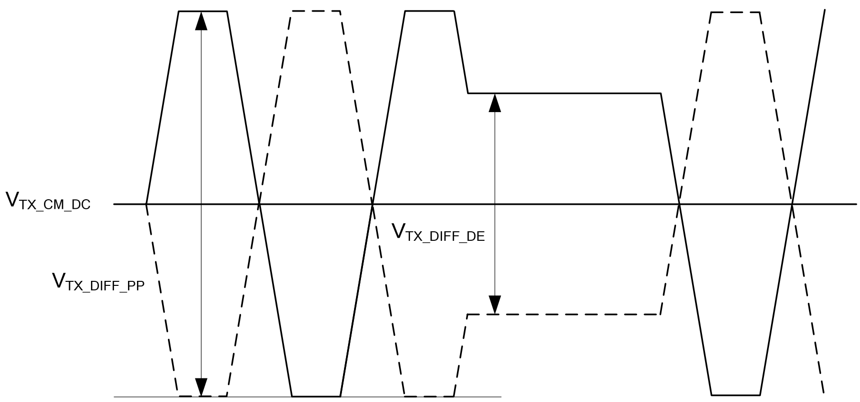
DC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ[d]	Max	Unit
Control pins (3.3V I/O):ADDR0,ADDR1						
V_{IH}	LVTTL input High-level voltage		2		VDD33	V
V_{IL}	LVTTL input Low-level voltage		GND		0.8	V
$\|I_{IH}\|$	Input High-level current	V_{IH} = 2V to VDD33			40	µA
$\|I_{IL}\|$	Input Low-level current	V_{IL} = GND to 0.8V			10	µA
Control pins (3.3V I/O): EN						
V_{IH}	LVTTL input High-level voltage		2		3.6	V
V_{IL}	LVTTL input Low-level voltage		GND		0.8	V
$\|I_{IH}\|$	Input High-level current	V_{IH} = 2V to 3.6V			50	µA
$\|I_{IL}\|$	Input Low-level current	V_{IL} = GND to 0.8V			30	µA
Control I^{2}C Pins: CSDA, CSCL(3.3V I/O)						
V_{IH}	High-level input voltage		1.6		3.6	V
V_{IL}	Low-level input voltage		GND		1	V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	GND		0.4	V
Resistors						
REXT	External reference resistor			4.99		kΩ
$R_{RX-TERM}$	Differential input termination resistor			100		Ω
$R_{TX-TERM}$	Differential output termination resistor			100		Ω

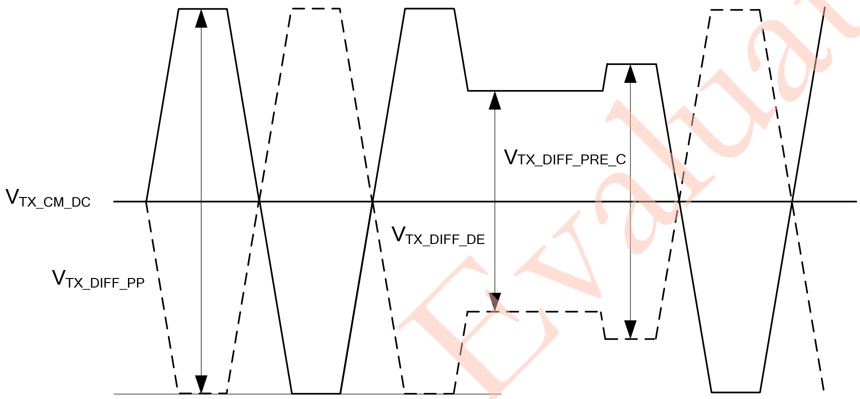
[d] All typical values are measured at 25 °C and 3.3V / 1.2V power supply.

AC CHARACTERISTICS

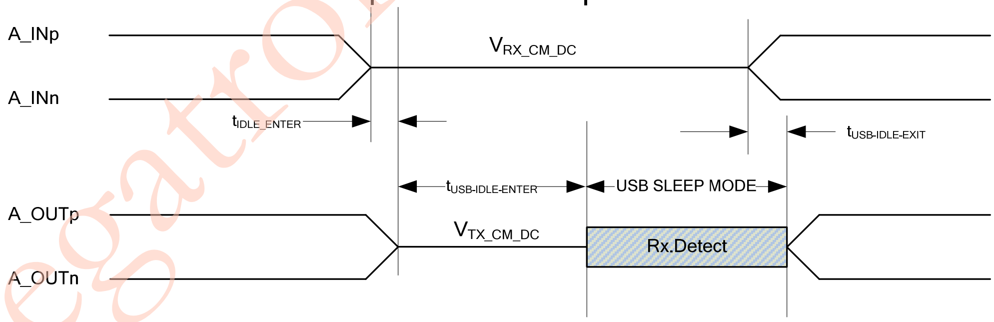
Parameter	Test Conditions	Min	Typ	Max	Unit
USB Receiver					
$V_{RX\_EYE\_HEIGHT}$ Rx input signal eye height	After Ref. Rx EQ @10Gbps	70			mV
Tj_{Rx} Rx input total jitter	After Ref. Rx EQ @10Gbps			0.671	UI
R_{RX_HIZ} Rx high impedance		10			kΩ
$R_{RX\_DC\_CM}$ Rx DC common mode impedance		18		30	Ω
$R_{RX\_DIFF\_DC}$ Rx DC differential impedance			100		Ω
$V_{RX\_CM\_DC}$ Rx common mode voltage			0		V
$V_{RX\_LFPS\_DET\ LFPS}$ signal detection threshold		100		300	mV
$t_{USB-IDLE-ENTER}$ Bus idle time before entering USB Idle mode				450	ms
$t_{USB-IDLE-EXIT}$ USB Idle mode to normal operation exit time				150	ns
USB Transmitter					
$V_{TX\_DIFF\_PP}$ Differential peak to peak output voltage	RLOAD=100Ω REXT = 4.99KΩ	800		1200	mV
$R_{TX\_DIFF\_DC}$ DC differential impedance	Normal operation		100		Ω
$V_{TX\_CM\_DC}$ Tx common mode voltage				1.2	V
$V_{TX\_CM\_AC}$ Tx AC common mode voltage				100	mVpp
t_{RISE} / t_{FALL} Tx output 20% to 80% rise time / fall time			50		ps
T_{SKEW_INTRA} Tx output intra-pair skew				10	ps
$t_{PROPAGATION}$ Differential propagation delay			2.1		ns



TX Differential Output with De-emphasis



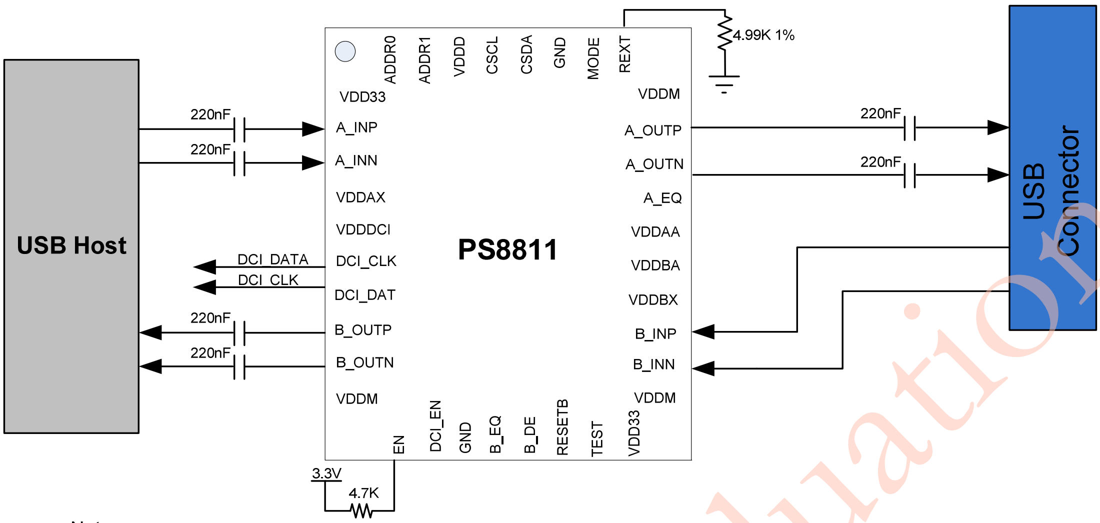
TX Differential Output with De-emphasis and Pre-shoot



Automatic Power Saving

Figure 4. Definition of Key Parameters for USB

TYPICAL APPLICATION DIAGRAM



Note:

1. Connect VDDD/VDDM/VDDAX/VDDAA/VDDBX/VDDBA to 1.2V Power supply. Connect VDD33 to 3.3V power supply. Connect VDDDCI to 3.3V if DCI is not used. Connect EPAD to GND.
2. For High speed signals connection, A_INP/A_INN & B_OUTP/B_OUTN should have to connect to Host side and A_OUTP/A_OUTN & B_INP/B_INN should have to connect to Connector side.

Figure 5. Typical Application Diagram

LAYOUT GUIDELINES

High Speed Interfaces

- Select proper PCB stack up and trace width at 85 Ω differential transmission line impedance for the high speed USB signals
- Avoid tight bends for the high speed USB signals
- Match intra-pair traces length within each differential pair
- Keep uninterrupted ground plane beneath USB signals
- Keep wide and shortest traces for both power and ground path to PS8811

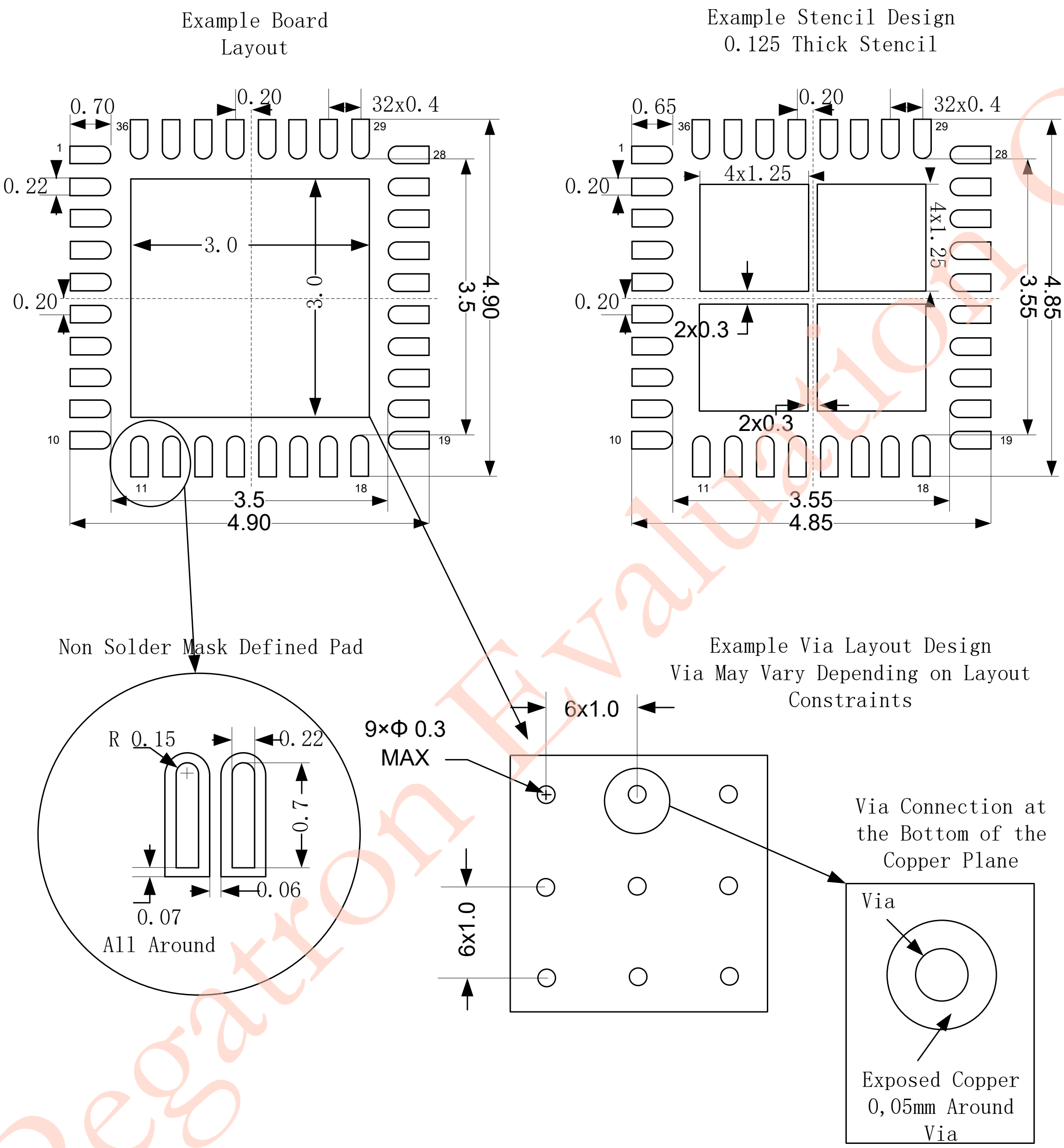
Filtering Capacitors

- Place 0.1 uF, 0.01 uF decoupling capacitors close to each power pin

Analog Current Bias Resistor

- Place a 4.99k Ω 1% precision resistor close to REXT pin and connect to GND solidly

PAD LAYOUT PATTERN GUIDELINES: 36-PIN 4.2x4.2mm QFN



NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

Figure 6. Exposed Thermal Pad Layout Guidelines for PS8811

ORDER & PACKAGING INFORMATION

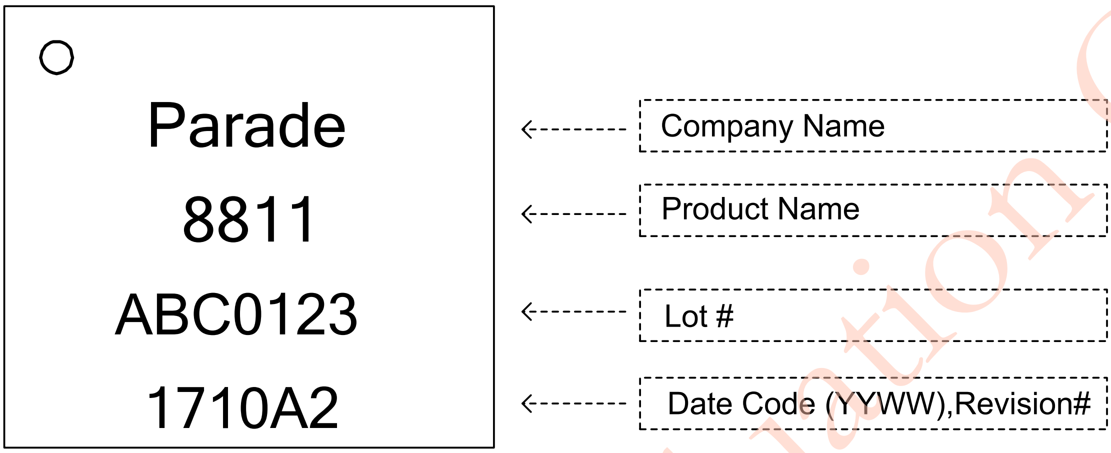
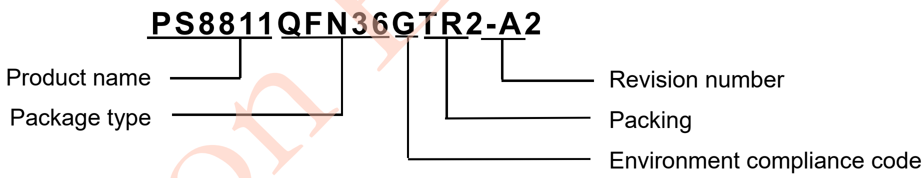


Figure 7. Top Side Marking

Order Information

PS8811 part number:

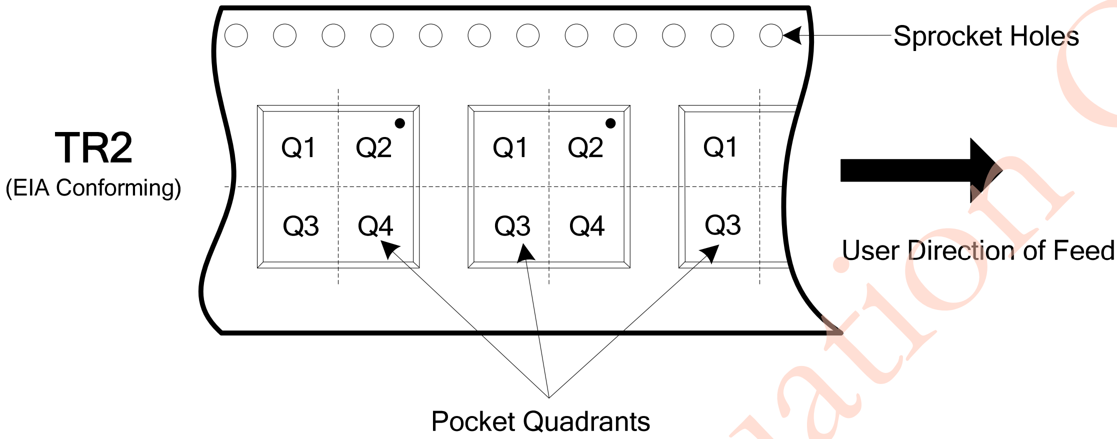


Part Number	Packing
PS8811QFN36GTR2-A2	Tape and Reel

Lead Finish: 100% Sn

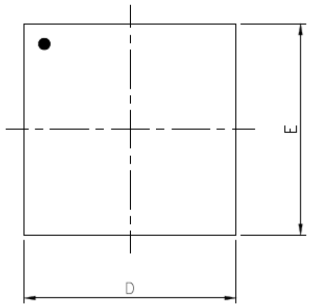
TAPE AND REEL PACKING PIN1 ORIENTATION

QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE

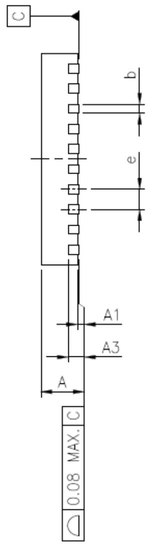


PHYSICAL DIMENSION

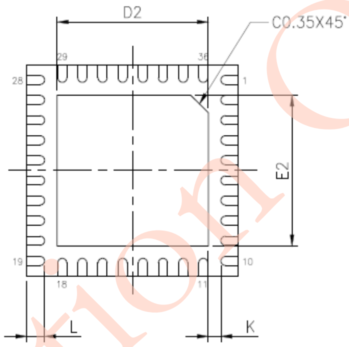
36-pin QFN 4.2x4.2 mm^2



Top View



Side View



Bottom View

Parameter	MIN	NOM	MAX	Unit
A	0.700	0.750	0.800	mm
A1	0.000	0.02	0.050	mm
A3		0.203 REF		mm
b	0.150	0.200	0.250	mm
D	4.10	4.20	4.30	mm
D2	2.95	3.00	3.05	mm
E	4.10	4.20	4.30	mm
E2	2.95	3.00	3.05	mm
e		0.400 BSC		mm
K	0.20	--	--	mm
L	0.30	0.35	0.40	mm

REVISION HISTORY

Version	Date	Items
Preliminary	2017/07/25	Initial release
V0.7	2017/09/25	Update PACKAGE DISSIPATION RATING Update AC/DC characteristic Update power consumption
V0.9	2018/05/14	Update Power consumption Update DCI description Update PAD layout guidelines Update order & packaging information
V1.0	2018/08/14	Update order & packaging information Update Pin description and change ADE to DCI_EN Updated Power consumption