ASMEDIA TECHNOLOGY INC

ASM1074 Data Sheet

USB3.0 HUB Controller

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	Nov. 15, 2011	Initial Release
0.2	March 26, 2012	Update the name of the pinout Update the electrical spec of clock Add power consumption table
0.3	May, 23, 2012	Correct the title of the figure 6 as package QFN88 Remove core power 1.2V support Rename the pin VCC12 and VCC12U as VCC10 and VCC10U Update the power consumption Add the power on sequence for crystal mode Upadte the strapping table Upadte the electrical spec
0.4	June 28, 2012	Update the pin description and strapping table
0.5	July 30, 2012	Correct the pin arrangement of Pin 72, 73, 75 and 76 Change the naming of power pins Update the pin description for strapping function Add the notice on strapping setting Update the power on sequence
0.6	Jan 23,2012	DSP port 1/2 USB3.0 pins polarity inversion change for better compatibility to some device controllers(pin26<->pin 27/pin29<- >pin30/pin32<- >pin33/ pin35<- pin36) Correct the description of Superspeed USB DSP naming rule.
0.7	Mar 26,2013	Add power consumption report notice.
1.0	Apr 30,2013	Formal Release
1.1	May 17,2013	5V regulator input range 4.0V~5.5V.
1.2	July 25,2013	Add Top Marking information & Total Power Consumption
1.3	April 22, 2016	Update thermal design spec
1.4	Mar 14,2017	Add HBM/MM ESD
1.5	Jan 17,2019	Correct the typo of disabling power saving mode
1.6	Dec 23,2019	Add Strapping pin timing diagram & requirement

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1. General Description

Engaged in Gigabit Data transfer Speed I/O solution development, Asmedia Technology is committed to enlarging product portfolio with introducing USB3.0 HUB controller Products. The ASM1074, the four downstream ports USB3.0 HUB Controller, highly integrated with ASMedia SuperSpeed USB3.0 and USB2.0 self-design PHYs, enables high speed PHY interface up to 5Gbps, following Universal Series Bus 3.0 Revision 1.0 Specification, supporting battery charge for portable device, following battery charge Revision 1.2.

2. Features

USB3.0 HUB Features

- Universal series Bus 3.0 Revision 1.0 Compliance
- Upstream Port support SuperSpeed, High-Speed and Full-Speed Connections
- Four Downstream Ports support SuperSpeed, High-Speed, Full-Speed and Low-Speed Connections
- Implement USB3.0 power management function
    - SuperSpeed Link Power Management support
    - USB2.0 Link Power Management support
- USB Attached SCSI Protocol Revision 1.0 Compliance
- Multiple Transaction Translator support
- Port Power Switching and Over-Current Protection per port control
- Individual and Gang mode selectable via strapping
- Remarkable with Removable or permanently attached

Battery Charge Features

- Support Battery Charge function for portable device, like Cellphone and Pad
- Dedicated Charge Port (DCP) support
- Battery Charge Rev1.2 specification Compliance
- Automatic Battery Charge function detection
- Support the charge function while the system enters active or suspend state

General Feature

- Integrated 8-bit RISC microprocessor
- SPI flash support for customized firmware
- I2C EEPROM support for customized configuration
- Uploadable Firmware & configuration via upstream port
- Integrated 5V to 3.3V linear regulator
- Self-power and bus-power support
- Automatic power type detection and dynamic power type switch
- Flexible and selectable clock source
    - Could select crystal mode or external clock mode
    - Support 20MHz or 25MHz or 30MHz crystal
    - Support 48MHz clock input from external clock generator
- Multiple GPIOs for LED application
- Two Power Supply domain
    - IO power supply with 3.3V+/-0.3V
    - Core power supply 1.05V+/-0.05V
- 10x10 mm^2 88-pin QFN package
- Green Package with RoHs Compliance

Package Type

◇ QFN 88L

3. Functional Diagram

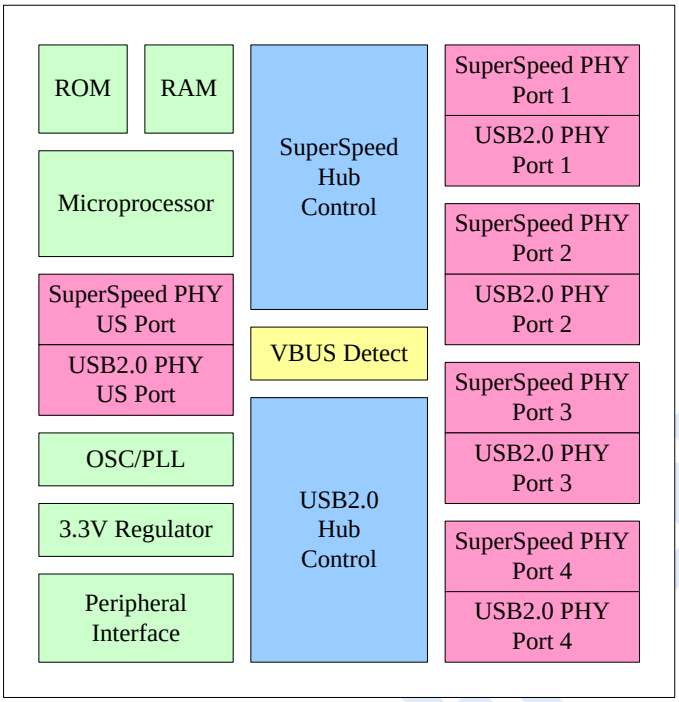


Figure 1: Functional Diagram

4. Pinout Diagrams

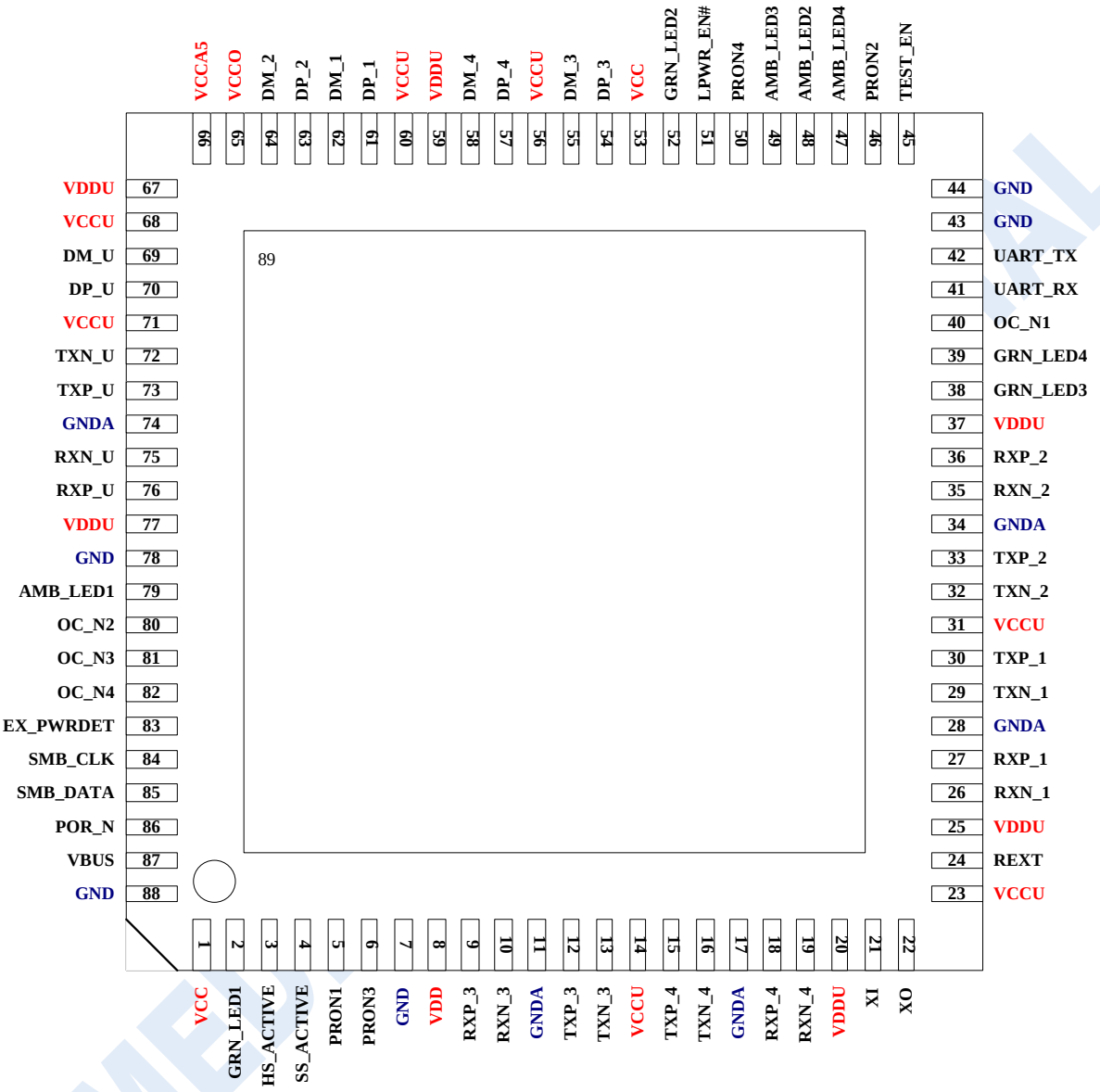


Figure 2: ASM1074 pinout

5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

SuperSpeed USB Interface

Pin No.	Name	TYPE	Descriptions
26	RXN_1	DiI	SuperSpeed USB Downstream Port 1 Differential Receive Data -
27	RXP_1	DiI	SuperSpeed USB Downstream Port 1 Differential Receive Data +
29	TXN_1	DiO	SuperSpeed USB Downstream Port 1 Differential Transmit Data -
30	TXP_1	DiO	SuperSpeed USB Downstream Port 1 Differential Transmit Data +
35	RXN_2	DiI	SuperSpeed USB Downstream Port 2 Differential Receive Data -
36	RXP_2	DiI	SuperSpeed USB Downstream Port 2 Differential Receive Data +
32	TXN_2	DiO	SuperSpeed USB Downstream Port 2 Differential Transmit Data -
33	TXP_2	DiO	SuperSpeed USB Downstream Port 2 Differential Transmit Data +
9	RXP_3	DiI	SuperSpeed USB Downstream Port 3 Differential Receive Data +
10	RXN_3	DiI	SuperSpeed USB Downstream Port 3 Differential Receive Data -
12	TXP_3	DiO	SuperSpeed USB Downstream Port 3 Differential Transmit Data +
13	TXN_3	DiO	SuperSpeed USB Downstream Port 3 Differential Transmit Data -
18	RXP_4	DiI	SuperSpeed USB Downstream Port 4 Differential Receive Data +
19	RXN_4	DiI	SuperSpeed USB Downstream Port 4 Differential Receive Data -
15	TXP_4	DiO	SuperSpeed USB Downstream Port 4 Differential Transmit Data +
16	TXN_4	DiO	SuperSpeed USB Downstream Port 4Differential Transmit Data -
75	RXN_U	DiI	SuperSpeed USB Upstream Port Differential Receive Data -
76	RXP_U	DiI	SuperSpeed USB Upstream Port Differential Receive Data +
72	TXN_U	DiO	SuperSpeed USB Upstream Port Differential Transmit Data -
73	TXP_U	DiO	SuperSpeed USB Upstream Port Differential Transmit Data +

USB2.0 Interface

Pin No.	Name	TYPE	Descriptions
61	DP_1	DiB	USB2.0 Downstream Port C Bus Data +
62	DM_1	DiB	USB2.0 Downstream Port C Bus Data -
63	DP_2	DiB	USB2.0 Downstream Port D Bus Data +
64	DM_2	DiB	USB2.0 Downstream Port D Bus Data -
54	DP_3	DiB	USB2.0 Downstream Port A Bus Data +
55	DM_3	DiB	USB2.0 Downstream Port A Bus Data -
57	DP_4	DiB	USB2.0 Downstream Port B Bus Data +
58	DM_4	DiB	USB2.0 Downstream Port B Bus Data -
70	DP_U	DiB	USB2.0 Upstream Port Bus Data +
69	DM_U	DiB	USB2.0 Upstream Port Bus Data -

MISC Interface

Pin No.	Name	TYPE	Descriptions

Pin No.	Name	TYPE	Descriptions
45	TEST_EN	I	Test Enable Pin. 0: Normal mode, 1:ATE Test mode
87	VBUS	I	VBUS valid input
5	PRON1	O	Port 1 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
46	PRON2	O	Port 2 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
6	PRON3	O	Port 3 Power Switch Enable, Internal ~40Kohm resistance Pull Down during chip reset
50	PRON4	O	Port 4 Power Switch Enable Internal ~40Kohm resistance Pull Down during chip reset
40	OC_N1	I	Port 1 Over Current Indicator
80	OC_N2	I	Port 2 Over Current Indicator
81	OC_N3	I	Port 3 Over Current Indicator
82	OC_N4	I	Port 4 Over Current Indicator
86	POR_N	I	Power On Reset
24	REXT	I	External Reference Resistor 12.1Kohm +/-0.1%
83	EX_PWRDET	I	External Power Detect 1: Self-powered mode 0: Bus-powered mode
51	LPWR_EN#	O	Low power mode enable
21	XI	I	Crystal Input or Clock input
22	XO	O	Crystal Output
84	SMB_CLK	O	SMBus Clock Bus or I2C_CLK. Refer to the strapping table
85	SMB_DATA	O	SMBus Data Bus or I2C_DATA. Refer to the strapping table
42	UART_TX	O	UART DATA Transmit Internal ~40Kohm resistance Pull Down during chip reset
41	UART_RX	I	UART DATA Receive
3	HS_ACTIVE	O	Upstream Port High Speed Bus Active LED Indicator Configured as SPI_CLK while power on Internal ~40Kohm resistance Pull Down during chip reset
4	SS_ACTIVE	O	Upstream Port SuperSpeed Bus Active LED Indicator Configured as SPI_DI while power on
2	GRN_LED1	O	Port 1 Green LED Indicator Internal ~40Kohm resistance Pull Down during chip reset
52	GRN_LED2	O	Port 2 Green LED Indicator Internal ~40Kohm resistance Pull Down during chip reset
38	GRN_LED3	O	Port 3 Green LED Indicator
39	GRN_LED4	O	Port 4 Green LED Indicator Internal ~40Kohm resistance Pull Down during chip reset
79	AMB_LED1	O	Port 1 Amber LED Indicator
48	AMB_LED2	O	Port 2 Amber LED Indicator
49	AMB_LED3	O	Port 3 Amber LED Indicator
47	AMB_LED4	O	Port 4 Amber LED Indicator

Power and Ground

Pin No.	Name	TYPE	Descriptions
7, 88, 43, 44, 78, 89	GND	**G**	Common Ground
11, 17, 28, 34, 74	GNDA	**G**	Analog Ground
1, 53	VCC	**P**	3.3V IO Power
8	VDD	**P**	1.05V Core Power
14, 23, 31, 56, 60, 68, 71	VCCU	**P**	3.3V Analog Power for USB PHY
20, 25, 37, 59, 67, 77	VDDU	**P**	1.05V Analog Power for USB PHY
65	VCCO	**P**	Linear Regulator 3.3V Output
66	VCCA5	**P**	Linear Regulator 5V Input

Strapping Table

Pin	Function	Description

GRN_LED[2:1]	CLK_SEL[1:0]	00: 25MHz Crystal (Default) 01: 48MHz Clock input 10: 30MHz Crystal 11: 20MHz Crystal
GRN_LED4	Individual/gang mode select	0: Individual Mode (Default) 1: gang mode
UART_TX	SMB mode enable	0: Disable (Default), 1: Enable
HS_ACTIVE	SMB Address Select	0: 0x60 (Default), 1: 0x62
SMB_CLK	I2C I/F enable	0: Disable 1: Enable

Notice:

1.) GRN_LEDs and HS_ACTIVE are also used as strapping with internal pull down resistors during chip reset. Strongly recommend to have **ACTIVE HIGH** type for LED PCB design.
Please refer to the reference schematic and the below examples are for the strap low (internal pull down resistor) and strap high (external pull up resistor)

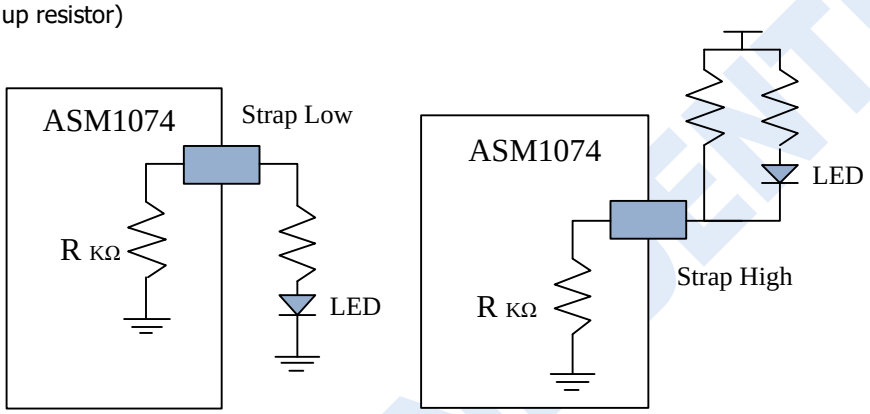
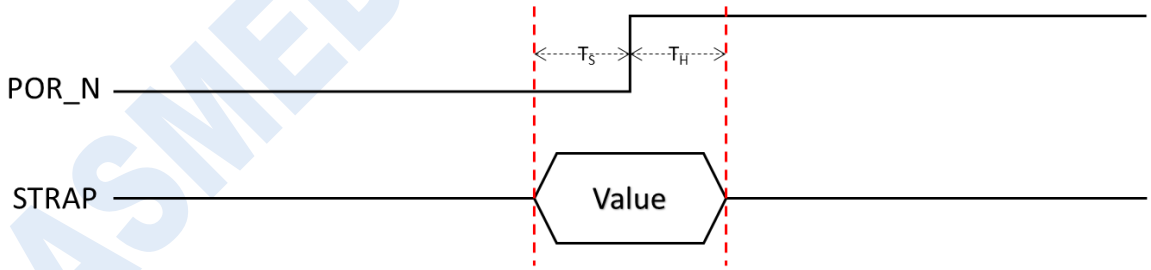


Figure 3: LED application on strapping pins

2.) While the strapping is setting up, only one interface between SPI, SMBus and I2C can be enabled after power on.

UART_TX	SMB_CLK	Mode
1	X	SMbus Interface Enable
0	1	Enable External I2C EEPROM
0	0	Enable External SPI flash

3.) Strapping timing diagram & timing requirement



Strapping timing requirement:

	Paramater	Min	Max	Unit
Ts	Setup time	100		us
TH	Hold time	100		us

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses the below parameter listed under absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply for VDD	-0.5 ~ +1.5	V
Power Supply for VCC	-0.5 ~ +4.0	V
Power Supply for VCCA5	-0.5 ~ 6.0	V
DC Input Voltage	-0.5 ~ +4.0	V
Output Voltage	-0.5 ~ +4.0	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VCC	3.3V Digital Power Supply	3.0	3.3	3.6	V	
VDD	1.05V Digital Power Supply	1.00	1.05	1.10	V	
VCCU	3.3V USB Analog Power Supply	3.0	3.3	3.6	V	
VDDU	1.05V USB Analog Power Supply	1.00	1.05	1.10	V	
VCCA5	5V Regulator Input	4.0	5.0	5.5	V	
VCCO	3.3V Regulator Output	3.0	3.3	3.6	V	
T_J	Operating Junction Temperature	0	25	125	ºC	
T_C	Operating Case Temperature			85	ºC	
T_A	Operating Ambient Temperature			55	ºC	
HBM ESD	Human Body Mode ESD Capability		3.5		KV	
MM ESD	Machine Mode ESD Capability		250		V	

Chip Temperature (T_J, T_C) Calculation

Symbols	Parameter	How to get?
T_A	Ambient temperature	Measure temperature around chip
T_J	Operating junction temperature	$T_J = \Theta_{JA}$ * Power + T_A
T_C	Operating case temperature	$T_C = T_J - \Psi_{JT}$ * Power
R_{JA}	Junction to Ambient thermal resistance	24.6 (data from package vender)
R_{JC}	Junction to case thermal resistance	5.1 (data from package vender)
Ψ_{JT}	Junction to top thermal characterization	0.08 (data from package vender)
Power	Chip power consumption	Measure chip power consumption

- Thermal test board condition, please refer to JEDEC JESD51-5
- Thermal test method environmental conditions refer to JESD51-2
- Example: If chip power consumption is 1.2W; T_A=55^{0}C
  TJ = 24.6*1.2 + 55 = 84.5^{0}C
  TC = 84.52 – 0.08*1.2 = 84.4^{0}C

6.3 AC/DC Characteristics

DC Electrical Characteristics for General Digital Pins

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
VIH	Input High Level	2.0			V	
VIL	Input Low Level			0.8	V	
Ileak	Input Leakage Level			10	uA	
VOH	Output High Level	2.4			V	
VOL	Output Low Level			0.5	V	

DC Electrical Characteristics for VBUS Pin

Symbols	Parameter	Min.	Typ.	Max.	Units
VIH	Input High Level	2			V
VIL	Input Low Level			0.8	V
VHYS	Input Hysteresis	0.57	0.6	0.65	V
VTH-L2H	VTH of Schmitt Trigger low to high	1.38		1.8	V
VTH-H2L	VTH of Schmitt Trigger high to low	0.82		1.15	V

Noted: This pin could only support 3.3+/-0.3V power, not 5V tolerance.

USB3.0 Electrical Specification

(Refer to Universal Serial Bus 3.0 Specification Rev. 1.0)

Transmitter Normative Electrical Parameters

Symbols	Parameter	Min	Max	Unit	Remark
UI	Unit Interval	199.94	200.06	ps	300 ppm without SSC
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	1.2	V	
$V_{TX-DIFF-PP-LOW}$	Low Power differential p-p Tx voltage swing	0.4	1.2	V	
$V_{TX-DE-RATIO}$	Tx de-emphasis level ratio	3.0	4.0	dB	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection		0.6	V	
$C_{AC-COUPLING}$	AC Coupling Capacitor	75	200	nF	
$R_{TX-DIFF-DC}$	DC Differential impedance	72	120	Ω	
$T_{CDR-SLEW-MAX}$	Maximum slew rate		10	ms/s	

Transmitter Informative Electrical Parameters

Symbols	Parameter	Min	Max	Unit	Remark
$V_{TX-DC-CM}$	Transmitter DC common mode voltage	0	2.2	V	
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC common mode voltage active		100	mVpp	
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC Common Mode Voltage between U0 and U1		200	mV	
$V_{TX-IDLE-DIFF-ACpp}$	Electrical Idle Differential Peak-Peak Output Voltage	0	10	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0	10	mV	
$C_{TX-PARASITIC}$	Tx input capacitance for return loss		1.25	pF	
$I_{TX-SHORT}$	Transmitter Short-Circuit Current Limit		60	mA	
R_{TX-DC}	Transmitter DC common mode impedance	18	30	Ω	
$T_{MIN-PULSE-DJ}$	Deterministic min pulse	0.96		UI	

Symbols	Parameter	Min	Max	Unit	Remark
$T_{MIN-PULSE-TJ}$	Tx min pulse	0.9		UI	
T_{TX-EYE}	Transmitter Eye	0.625		UI	
$T_{TX-DJ-DD}$	Tx deterministic jitter		0.205	UI	

Receiver Normative Electrical Parameters

Symbols	Parameter	Min	Max	Unit	Remark
UI	Unit Interval	199.94	200.06	ps	300 ppm without SSC
$V_{RX-LFPS-DET-DIFFpp}$	LFPS Detect Threshold	100	300	mV	
R_{RX-DC}	Receiver DC common mode impedance	18	30	Ω	
$R_{RX-DIFF-DC}$	DC Differential impedance	72	120	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during Reset or power down	25K		Ω	

Receiver Informative Electrical Parameters

Symbols	Parameter	Min	Max	Unit	Remark
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30		mV	
$V_{RX-CM-AC}$	Rx AC common mode voltage		150	mVp	
$V_{RX-CM-DC-ACTIVE-IDLE-DELTAp}$	Rx AC Common Mode Voltage during the U1 to U0 transition		200	mV	
$C_{RX-PARASITIC}$	Rx input capacitance for return loss		1.1	pF	
R_{TX-DC}	Transmitter DC common mode impedance	18	30	Ω	
T_{RX-TJ}	Maximum Rx inherent timing error		0.45	UI	
$T_{RX-DJ-DD}$	Maximum Rx inherent deterministic timing error		0.285	UI	

USB2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

External Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{XTAL}	Frequency		20/25/30		MHz
Δf_{XTAL}	Long Term Stability (at 25^0C)	-30		30	ppm
T_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

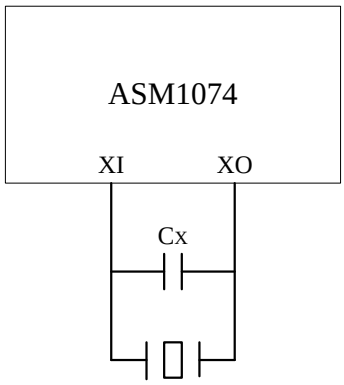


Figure 4: Differential Crystal Design

Differential Clock Oscillator Electrical Specification (Crystal mode)

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		20/25/30		MHz
Δf_{CLK}	Long Term Stability (all condition)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		C_{TOTAL}-C_O		pF
C_{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R_{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

48MHz Clock Input Electrical Specification (Clock mode)

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		48		MHz
T_{PERIOD}	CLK Period	20.83125		20.83542	ns
T_{ABS}	Absolute Min/Max CLK Period	20.48125		21.18542	ns
T_{HIGH}	CLK high time	8.216563		11.15198	ns
T_{LOW}	CLK low time	7.816563		10.95198	ns
Edge Rate	Rising/Falling edge rate	1.0		2.0	V/ns
$T_{CCJITTER}$	Cycle to Cycle Jitter			350	ps
	Duty Cycle	45		55	%
V_{IH}	Input High Level	2.0			V
V_{IL}	Input Low Level			0.8	V

Total Power Consumption

- **Enabling Power Saving mode:**

Mode	Ports	VCC			VDD			Units
		Idle	Suspend	Run Junior	Idle	Suspend	Run Junior	
USB 3.0	USP	1.66	1.66	NA	13.18	13.18	NA	
USB2.0	Port 1	29.8	1.66	32.5	37.6	13.18	37.7	mA
	Port 1+2	35.9	1.66	45.4	40.3	13.18	40.8	mA
	Port 1+2+3	42.1	1.66	57.8	41.9	13.18	42.6	mA
	Port 1+2+3+4	48.06	1.66	74.5	44.38	13.18	44.75	mA
USB3.0	Port 1	35.52	11.26	57.8	81.1	18.7	199.1	mA
	Port 1+2	33.2	11.26	76.52	76.4	18.7	200.5	mA
	Port 1+2+3	44.55	11.26	105.77	92.32	18.7	261.6	mA
	Port 1+2+3+4	64.19	11.26	120.4	96.34	18.7	307.8	mA

- **Disabling Power Saving Mode:**

Mode	Ports	VCC			VDD			Units
		Idle	Suspend	Run Junior	Idle	Suspend	Run Junior	
USB 3.0	USP	159	135.6	NA	215.7	183.3	NA	
USB2.0	Port 1	187.2	135.7	187.2	223.8	184.1	223.8	mA
	Port 1+2	210.8	135.7	210.7	227.4	185.4	229.1	mA
	Port 1+2+3	234.3	135.7	233.9	231.2	184.5	256.3	mA
	Port 1+2+3+4	257.7	135.7	257.2	235.1	186.3	261.1	mA
USB3.0	Port 1	151.7	128.1	151.6	290.3	186.4	292.4	mA
	Port 1+2	151.8	88.2	151.8	334.1	137.4	335.6	mA
	Port 1+2+3	147.8	84	147.8	388.2	139.4	388.1	mA
	Port 1+2+3+4	144.1	39.15	144.09	448.4	90.93	437	mA

7. Timing Diagram

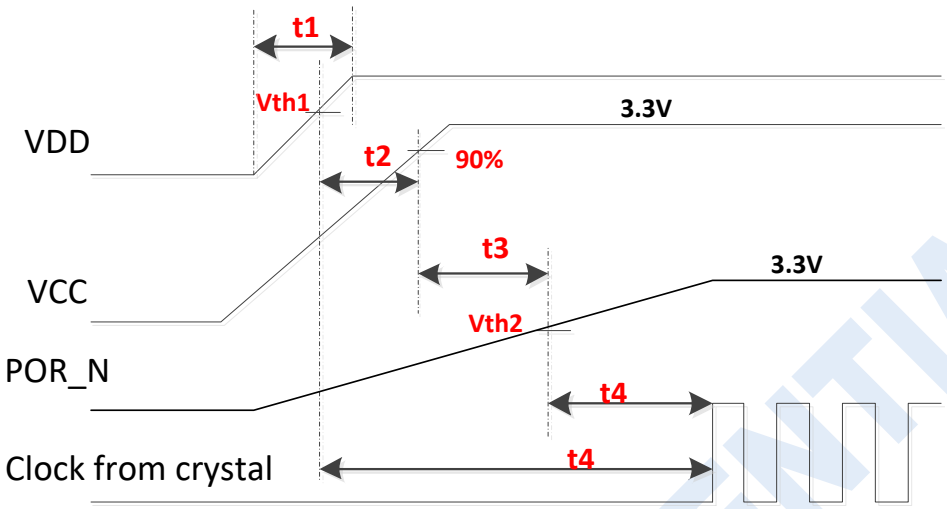


Figure 5: Power on Sequence for crystal mode

Power on Sequence Timing Specification for crystal mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
Vth1	The threshold of VDD internal power detect	0.49	0.7	0.92	V	
Vth2	The threshold of POR_N signal detect		0.5*VCC		V	
t1	Settling time of VDD stable power			6	ms	Measure from 10% to 90%
t2	The maximum delay timing of VCC power ready after the threshold of VDD	N/A		6	ms	Measure the timing between the point of Vth1 to 90% of VCC
t3	POR_N goes high after VCC power ready	0		N/A	ms	Measure the timing between the 90% of VCC to Vth2 of POR# (If without external POR_N circuit, this rule could be skipped)
t4	Maximum delay of stable clock available after the latest available point of Vth1 or Vth2			26	ms	Measure the timing between the point of Vth to stable clock available (self-powered mode)
				151	ms	Measure the timing between the point of Vth to stable clock available (bus-powered mode)

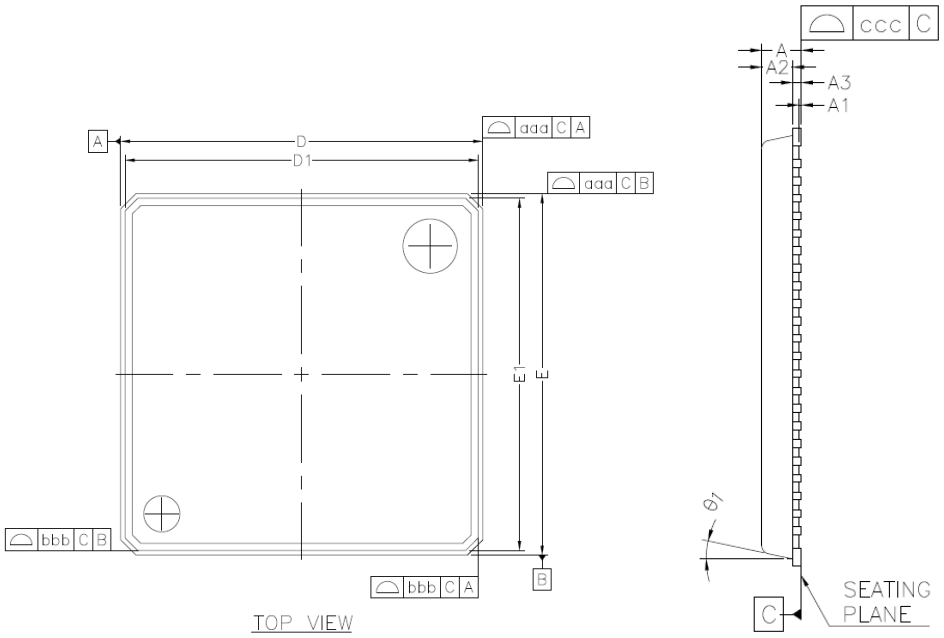
TBD

Figure 6: Power on Sequence for clock input mode

Power on Sequence Timing Specification for 48MHz clock mode

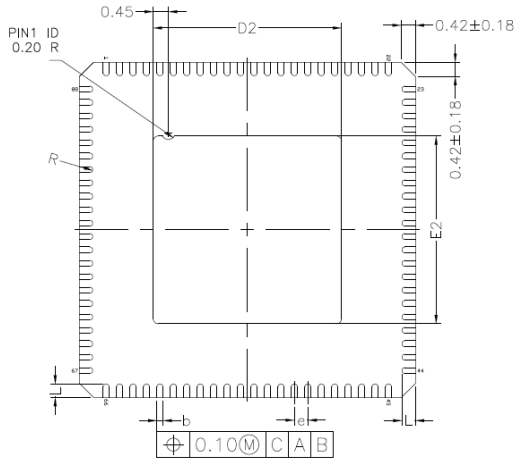
Symbols	Parameter	Min	Typ	Max	Unit	Remark
t5	VCC power ready after VDD power ready			2	ms	Measure the timing between the point of Vth to 90% of VCC33
t6	POR_N goes high after VDD power ready and 48MHz clock available		TBD		ms	
t7	stable 48MHz clock available after VDD power ready		TBD		ms	

8. Package Information



* CONTROLLING DIMENSION : MM

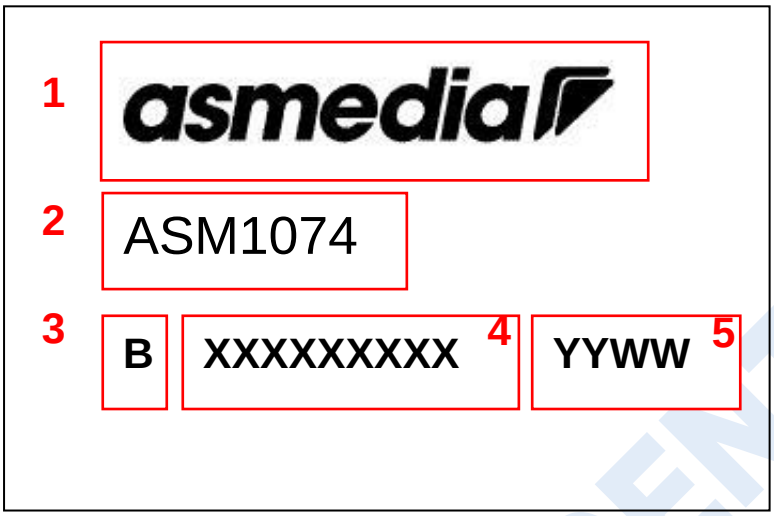
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.13	0.18	0.23	0.005	0.007	0.009
D	10.00 bsc			0.394 bsc		
D1	9.75 bsc			0.384 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	10.00 bsc			0.394 bsc		
E1	9.75 bsc			0.384 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.065	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		



NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.13 AND 0.23 mm FROM TERMINALTIP.(REFER TO SPEC "b")
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING. (TIN PLATING)
9.APPLIED ONLY TO TERMINALS.(TIN PLATING)
10.PACKAGE CORNERS UNLESS
OTHERWISE SPECIPIED
ARE R0.175±0.025 mm.

Figure 7: Mechanical Specification – QFN 88L

9. Top Marking Information



1. asmedia: ASMedia Logo
2. ASM1074: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code