Vendor p/n:TPS25810RVCR
Pin Define same as page.3
dimension same as "dimension. pdf"

TPS25810 USB Type-C DFP Controller and Power Switch with Load Detection

1 Features

- Complete USB Type-C DFP (Downstream Facing Port) Solution (w.o. USB PD)
  - Connector Attach/Detach Detection
  - STD/1.5A/3A Capability Advertisement on CC Line
  - Super Speed Lines Polarity Determination
  - V_{BUS} Application
  - V_{CONN} Application to Active Cable
  - Audio and Debug Accessory Identification
- Ultra-Low Iddq
  - 5 uA (typ) with no attachment
- Optional Three Supply Inputs for Maximum System Design Flexibility
  - IN1: USB Charging Supply
  - IN2: VCONN Supply
  - AUX: Device Power Supply
- Built-in Power Wake to Support Low Power in System Hibernate (S4) and OFF (S5) Power States
- Integrated 36 mΩ (typ) High-Side MOSFET
- Selectable 3.34 A/1.67 A OUT Current Limit with +/- 7.5% Accuracy
- Load Detection to Enable Port Power Management
- Built-in ESD Protection on CC1 and CC2
  - +/8 kV Contact and +/-15 kV Air Discharge ESD Rating (IEC 61000-4-2)
- Package: 20-pin QFN (3x4)

2 Applications

- Type C USB Host Port
- Notebook/Desktop/Tablets
- LCD Monitor/Docking Station and Charging Cradles
- USB Wall and Automotive Charger Adapters

4 Simplified Schematic

3 Description

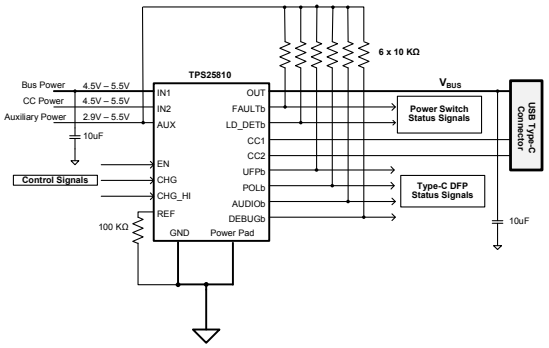
The TPS25810 is a USB Type-C Downstream Facing Port (DFP) controller with an integrated 3 A rated USB power switch. The TPS25810 monitors the Type-C Configuration Channel (CC) lines to determine when a USB device is attached. If an Upstream Facing Port (UFP) device is attached, the TPS25810 applies power to V_{BUS} and communicates the selectable V_{BUS} current sourcing capability to the UFP via the pass through CC line. If the UFP is attached using an active cable, the TPS25810 applies V_{CONN} power to the cable CC line. The TPS25810 also identifies when Type-C Audio or Debug Accessories are attached.

The TPS25810 draws less than 5 uA (TYP) when nothing is attached. Additional system power savings is achievable in S4/S5 system power states by using the UFPb output to disable the high power 5V supply when no UFP is attached. In this mode the device is capable of running from an auxiliary supply (AUX) which can be a lower voltage supply, typically powering the system uC in low power states (S4/S5).

The TPS25810's 36 mΩ power switch has two selectable fixed current limits that align with the Type-C current levels. The FAULTb output signals when the switch is in an over current or over temperature condition. The LD_DETb output controls power management to multiple high current Type-C ports in an environment where all ports cannot simultaneously provide high current (3A).

Device Information

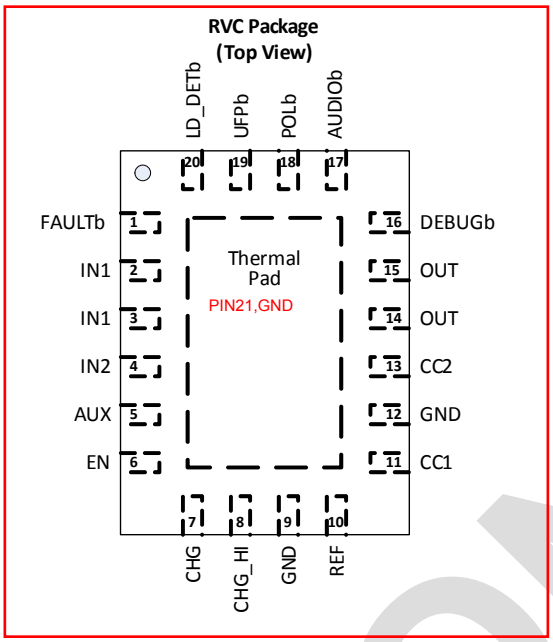
PART NUMBER	PACKAGE	*Packing*	*Number of Pieces*
TPS25810RVCR	QFN (20)	Large Reel	3000
TPS25810RVCT	QFN (20)	Small Reel	250



5 Revision History

Date	Revision	Notes
FEB 2015		Initial Draft
MARCH 2015		Added Packing information on page 1

6 Terminal Configuration and Functions



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	FAULTb	O	Open-drain logic output that asserts when the device is in current limit or over temperature.
2,3	IN1	I	V_{BUS} input supply. Internal power switch connects IN1 to OUT.
4	IN2	I	V_{CONN} input supply. Internal power switch connects IN2 to CC1 or CC2. Short to IN1 if only one 5V supply is used.
5	AUX	I	Auxiliary input supply. Connect to always alive system rail to use the Power Wake feature. Short to IN1 and IN2 if only one supply is used.
6	EN	I	Enable logic input to turn the device on and off.
7	CHG	I	Charge logic input to select between standard USB or Type-C current sourcing ability.
8	CHG_HI	I	High-charge logic input to select between 1.5 A and 3.0 A Type-C current sourcing ability. Valid when CHG is set to Type-C current.
9,12	GND	-	Ground.
10	REF	I	Analog input used to make a current reference. Connect a 1%, 100ppm, 100kΩ resistor between this terminal and GND.
11	CC1	I/O	Analog input/output that connects to the Type-C receptacle CC1 terminal.
13	CC2	I/O	Analog input/output that connects to the Type-C receptacle CC2 terminal.
14,15	OUT	O	Power switch output.
16	DEBUGb	O	Open-drain logic output that asserts when a Type-C Debug accessory is identified on the CC lines.
17	AUDIOb	O	Open-drain logic output that asserts when a Type-C Audio accessory is identified on the CC lines.
18	POLb	O	Polarity open-drain logic output that signals which Type-C CC terminal is connected to the CC line. This gives the information needed to mux the super speed lines. Asserted when the CC2 terminal is connected to the CC line in cable.
19	UFPb	O	Open-drain logic output that asserts when a Type-C UFP is identified on the CC lines.
20	LD_DETb	O	Load-detect open-drain logic output that signals when a device set to source Type-C 3 A current is sourcing at least 1.67 A
—	PowerPAD	—	Thermal pad on bottom of package.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Voltages are respect to GND unless otherwise noted

			MIN	MAX	UNIT
V	Terminal voltage	IN1, IN2, AUX, EN, CHG, CHG_HI, RREF, OUT, LD_DETb, FAULTb, CC1, CC2, UFPb, POLb, DEBUGb, AUDIOb	-0.3	7	V
I_{SRC}	Terminal positive source current	OUT, REF, CC1, CC2		Internally limited	A
I_{SNK}	Terminal positive sink current	OUT		5	A
		CC1, CC2 (While applying V_{CONN})		1	A
		LD_DETb, FAULTb, UFPb, POLb, DEBUGb, AUDIOb		Internally limited	mA
T_J	Operating junction temperature		-40	180	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage Temperature	-65	150	°C
V_{ESD}(1) Electrostatic Discharge	Human body model (HBM) ESD stress voltages, all pins(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltages, all pins(3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Voltages are respect to GND unless otherwise noted

			MIN	NOM	MAX	UNIT
V_I	Supply Voltage	IN1	4.5		6.5	V
		IN2	4.5		5.5	V
		AUX	2.9		5.5	V
V_I	Input Voltage	EN, CHG, CHG_HI	0		5.5	V
V_{IH}	High-level input voltage	EN, CHG, CHG_HI	1.17			V
V_{IL}	Low-level input voltage	EN, CHG, CHG_HI			0.63	V
V_{PU}	Pull-up Voltage	Used LD_DETb, FAULTb, UFPb, POLb, DEBUGb, AUDIOb	0		5.5	V
I_{SRC}	Positive source current	OUT			3	A
		CC1 or CC2 when supplying V_{CONN}			250	mA
I_{SNK}	Positive sink current (10 ms moving average)	LD_DETb, FAULTb, UFPb, POLb, DEBUGb, AUDIOb			10	mA
I_{SNK_PULSE}	Positive repetitive pulse sink current	LD_DETb, FAULTb, UFPb, POLb, DEBUGb, AUDIOb			Internally limited	mA
R_{REF}	Reference Resistor	Room temperature value	99	100	101	kΩ
T_J	Operating junction temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		RVC (20 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	
Ψ_{JT}	Junction-to-top characterization parameter	3.7	
Ψ_{JB}	Junction-to-board characterization parameter	20.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	

[1] For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUT - POWER SWITCH						
$R_{DS(on)}$	On resistance(1)	T_J = 25°C, I_{OUT} = 3 A		36	42	mΩ
		-40°C ≤ T_J ≤ 85°C, I_{OUT} = 3 A		36	53	
		-40°C ≤ T_J ≤ 125°C, I_{OUT} = 3 A		36	60	
t_r	Output voltage rise time	V_{IN1} = 5 V, C_L = 1 uF, R_L = 100 Ω (see Figure X&X)	1.5	2	2.5	ms
t_f	Output voltage fall time		.5	.8	1.1	
t_{on}	Output voltage turn-on time	V_{IN1} = 5 V, C_L = 1 uF, R_L = 100 Ω (see Figure X&X)	3	4	5	ms
t_{off}	Output voltage turn-off time		2.5	3	3.5	
I_{REV}	OUT to IN reverse leakage current	V_{OUT} = 6.5 V, V_{IN1} = V_{EN} = 0 V, -40°C ≤ T_J ≤ 85°C , I_{REV} is current out of IN1 terminal		0	3	uA
OUT - CURRENT LIMIT						
I_{OS}	Short circuit current limit(1)	V_{CHG} = 0V or, V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V	1.55	1.67	1.79	A
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX}	3.10	3.34	3.58	
		R_{REF} = 10 Ω			8.00	
t_{res}	Current limit response time to short circuit	V_{IN1} - V_{OUT} = 1 V, R_L = 10 mΩ (see Figure X&X)		1.5	4	us
OUT - DISCHARGE						
	Discharge resistance	V_{OUT} = 4V, UFP signature removed from CC lines, time < t_{w_DCHG}	400	500	630	Ω
	R_{DCHG} discharge time	V_{OUT} = 1V, time I_{SNK_OUT} > 1mA after UFP signature removed from CC lines	39	65.5	106	ms
	Bleed discharge resistance	V_{OUT} = 4V, No UFP signature on CC lines, time > t_{w_DCHG}	TBD	150	TBD	kΩ
REF						
V_O	Output voltage		0.78	0.8	0.82	V

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$\overline{\text{FAULT}}$						
V_{OL}	Output low voltage	$I_{/FAULT}$ = 1 mA			250	mV
I_{OFF}	Off-state leakage	$V_{/FAULT}$ = 5.5V			1	uA
t_{DEGR}	Fault rising deglitch due to over current		5.5	8.2	11.8	ms
t_{DEGR}	Fault rising deglitch due to over temperature in current limit			none		ms
t_{DEGF}	Fault falling deglitch		5.5	8.2	11.8	ms
$\overline{\text{LD\_DET}}$						
V_{OL}	Output low voltage	$I_{/LD\_DET}$ = 1 mA			250	mV
I_{OFF}	Off-state leakage	$V_{/LD\_DET}$ = 5.5V			1	uA
I_{TH}	OUT sourcing, rising threshold current for load detect		1.66	1.77	1.89	A
	Hysteresis(2)			100		mA
t_{DEGR}	Load detect rising deglitch		44.4	65.4	94	ms
t_{DEGF}	Load detect falling deglitch NT		1.4	2.1	3.2	s

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CC1/CC2 - V_{CONN} POWER SWITCH						
$R_{DS(on)}$	On resistance	T_J = 25°C, I_{OUT} = 250 mA		480	560	mΩ
		-40°C ≤ T_J ≤ 85°C, I_{OUT} = 250 mA		480	705	
		-40°C ≤ T_J ≤ 125°C, I_{OUT} = 250 mA		480	800	
V_{TH}	OUT rising threshold voltage for V_{CONN} enable		3.8	4.0	4.2	V
	Hysteresis[2]		180	200	220	mV
t_r	Output voltage rise time	V_{IN2} = 5 V, C_L = 1 uF, R_L = 100 Ω (see Figure X&X)	TBD	TBD	TBD	ms
t_f	Output voltage fall time		TBD	TBD	TBD	
t_{on}	Output voltage turn-on time	V_{IN2} = 5 V, C_L = 1 uF, R_L = 100 Ω (see Figure X&X)	TBD	TBD	TBD	ms
t_{off}	Output voltage turn-off time		TBD	TBD	TBD	
CC1/CC2 - V_{CONN} POWER SWITCH - CURRENT LIMIT						
I_{OS}	Short circuit current limit[1]		300	375	460	mA
		R_{REF} = 10 Ω			1000	
t_{res}	Current limit response time to short circuit	V_{IN2} – V_{CONN} = 1 V, R = 10 mΩ (see Figure X&X)		1.5	4	us

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CC1/CC2 – CONNECT MANAGEMENT – DANGLING ACTIVE CABLE MODE						
I_{SRC}	Sourcing current on the pass-through CC line	V_{CCx} = 0 V	64	80	96	uA
I_{SRC}	Sourcing current on the Ra CC line	0 V ≤ V_{CCx} ≤ 1 V	64	80	96	uA
CC1/CC2 – Connect Management – Accessory Mode						
I_{SRC}	CCx Sourcing current (CC2- Audio, CC1-Debug)	0 V ≤ V_{CCx} ≤ 1 V	64	80	96	uA
I_{SRC}	CCx Sourcing current (CC1- Audio, CC2-Debug)	0 V ≤ V_{CCx} ≤ 1 V		none		uA

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CC1/CC2 – Connect Management – UFP Mode						
I_{SRC}	Sourcing current	V_{CHG} = 0 V and V_{CHG_HI} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V	74	80	86	uA
		V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V	166	180	194	
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX}, 0 V ≤ V_{CCx} ≤ 2.45 V	304	330	356	

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$\overline{UFP}$, $\overline{POL}$, $\overline{AUDIO}$, $\overline{DEBUG}$						
V_{OL}	Output low voltage	I_{SNK} = 1 mA			250	mV
I_{OFF}	Off-state leakage	V_O = 5.5V			1	uA
t_{DEGR}	Rising deglitch	CC signature applied	100	148	212	ms
t_{DEGF}	Falling deglitch	CC signature removed	8.4	12.5	18	ms
EN, CHG, CHG_HI - LOGIC INPUTS						
V_{TH}	Rising threshold voltage for given output			0.925	1.15	V
V_{TH}	Falling threshold voltage for given output		0.65	0.875		V
	Hysteresis (2)			50		mV
I_{IN}	Input current	V_{EN} = 0 V or 6.5V	-0.5		0.5	uA
OVER TEMPERATURE SHUT DOWN						
T_{TH_OTSD2}	Rising threshold temperature for device shutdown		155		180	°C
	Hysteresis (2)			20		°C
T_{TH_OTSD1}	Rising threshold temperature for OUT / V_{CONN} switch shutdown in current limit		135			°C
	Hysteresis (2)			20		°C

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
IN1						
V_{TH}	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis (2)		90	100	110	mV
I_I	Disabled supply current	V_{EN} = 0 V			2	uA
I_I	Enabled supply current with accessory or dangling active cable signature on CC lines or with CC lines open				2	uA
I_I	Enabled supply current with UFP attached	UFP signature on CC lines	TBD	TBD	TBD	uA
IN2						
V_{TH}	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis (2)		90	100	110	mV
I_I	Disabled supply current	V_{EN} = 0 V			2	uA
I_I	Enabled supply current with accessory or dangling active cable signature on CC lines or with CC lines open				2	uA
I_I	Enabled internal supply current with UFP and non-active cable signature on CC lines – no V_{CONN} applied (Does not include IN current that provides CC output current to the UFP Rd resistor)	UFP signature on CC lines, I_{q_INT} = I_{IN2} – $I_{SRC\_CC\_Rd}$	TBD	TBD	TBD	uA
I_I	Enabled internal supply current with UFP and active cable signature on CC lines – V_{CONN} applied (Does not include IN current that provides CC output current to the UFP Rd resistor)	UFP signature on CC lines, I_{q_INT} = I_{IN2} – $I_{SRC\_CC\_Rd}$	TBD	TBD	TBD	uA

Electrical Characteristics (continued)

Unless otherwise noted: -40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
AUX						
V_{TH}	Rising threshold voltage for UVLO		2.65	2.75	2.85	V
	Hysteresis (2)		90	100	110	mV
I_I	Disabled supply current			TBD	2	uA
I_I	Enabled internal supply current with CC lines open			5	10	uA
I_I	Enabled supply current with accessory or dangling active cable signature on CC lines			TBD	TBD	uA
I_I	Enabled supply current with UFP signature on CC lines			TBD	TBD	uA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

(2) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

8 Detailed Description

8.1 Overview

TPS25810 is a highly integrated USB Type-C power switch developed for the new USB connector. The part provides complete functionality needed to support a USB Type C Downstream Facing Port in a Type C receptacle where USB power delivery (PD) source capabilities (i.e. VBUS > 5V) are not implemented. The device is designed to be compliant to latest released version of Type C specification.

8.2 USB Type C Basic

For a detailed description of Type-C spec please refer to USB-IF website to download the latest released version. Some of the basic concepts of Type-C spec that pertains to understanding the operation of TPS25810 (a DFP device) are described below.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacle since the Type-C cable is plug-able in *either* direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of below three data modes

- **Host** mode: the port can only be host (provider of power)
- **Device** mode: the port can only be device (consumer of power)
- **Dual-Role** mode: the port can be either host or device

Port types:

- DFP (Downstream Facing Port): Host
- UFP (Upstream Facing Port): Device
- DRP (Dual-Role Port): Host or Device

Valid DFP-to-UFP connections:

- The table below describes valid DFP-to-UFP connections
- Host to Host or Device to Device have no functions

	Host-mode port	Device-mode port	Dual-role port
Host-mode port	No Function	Works	Works
Device-mode port	Works	No Function	Works
Dual-role port	Works	Works	Works*

*This may be automatic or manually driven

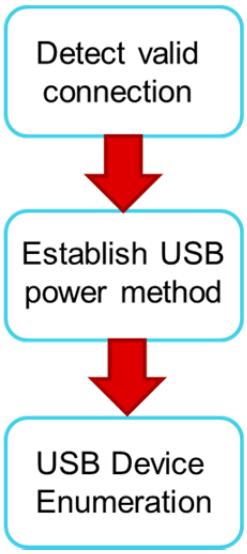
8.2.1 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB Power Delivery
- Discovery and configure optional Alternate and Accessory modes
- Enhances flexibility and ease of use

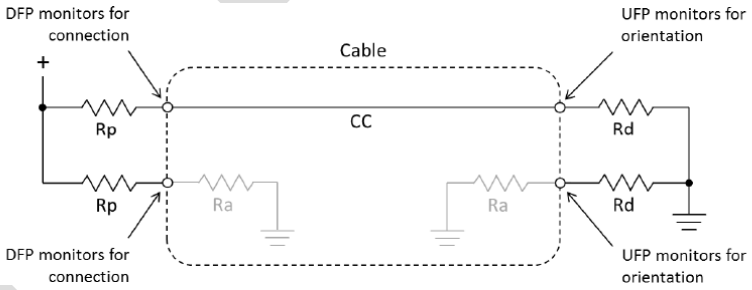
Typical flow of DFP to UFP configuration is shown below:



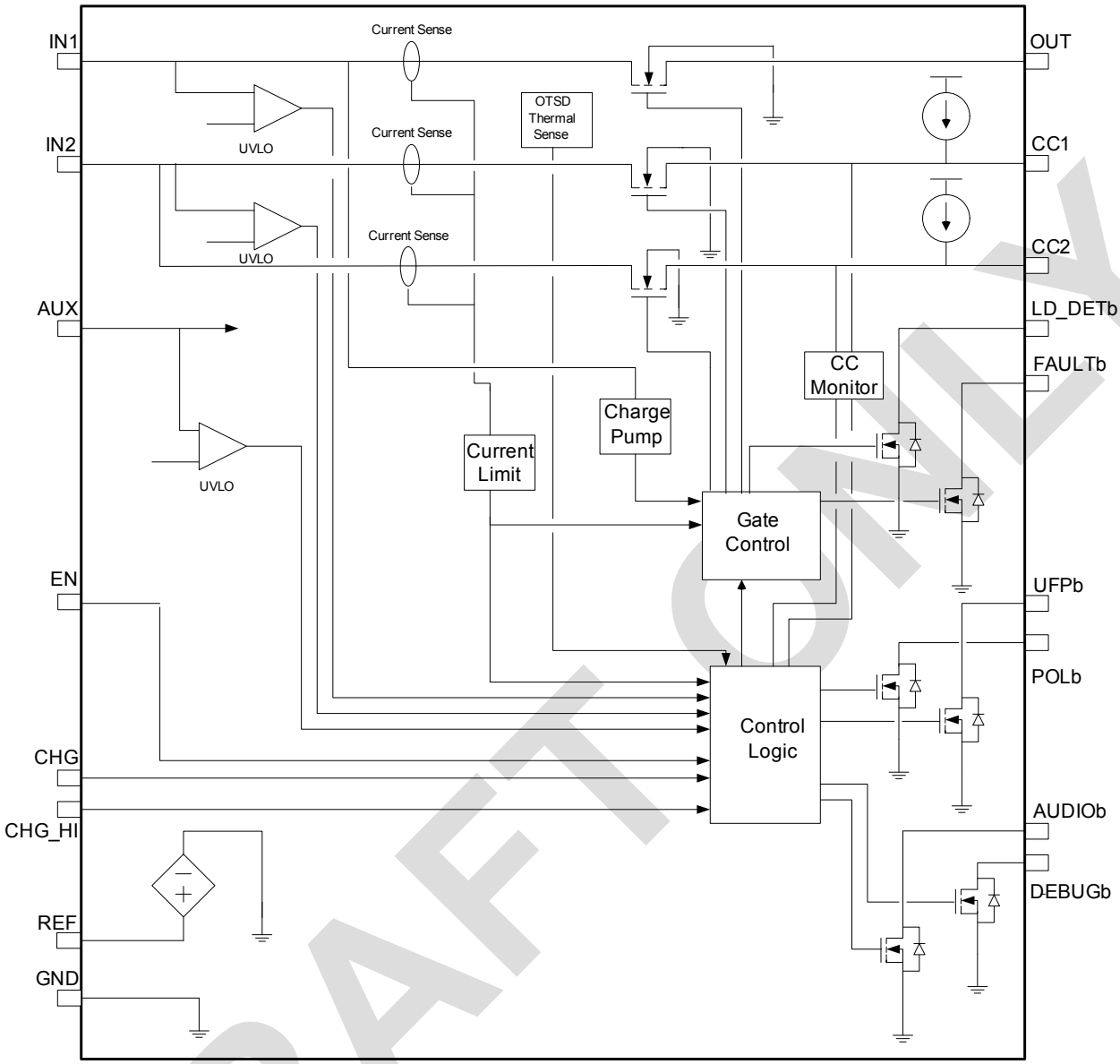
8.2.2 Detecting a Connection

DFPs and DRPs fulfil the role of detecting a valid connection over USB Type-C. Figure below shows a DFP to UFP connection made with Type C cable. DFPs and DRPs fulfil the role of detecting a valid connection over USB Type-C. As shown in the figure below, detection concept is based on being able to detect terminations in the product which has been attached. A pull-up and pull-down termination model is used. A Pull-up termination can be replaced by a current source.

- In the DFP-UFP connection the DFP monitors both CC pins for a voltage lower than its unterminated voltage
- An UFP advertises Rd on its CC pin
- A powered cable advertises Ra on it's Vconn pin
- An analog audio device advertises Ra on both Vconn and CC pins, which identifies it as an analog audio device, and initiates the transfer to the alternative audio mode



8.3 Functional Block Diagram



8.4 Feature Description

8.4.1 Detecting Connection

TPS25810 has two pins, CC1 and CC2 that serves to detect attachment to the port, establish current broadcast to a valid UFP, resolve cable orientation, configure VCONN and detect Debug or Audio Adapter Accessory attachment.

Below table lists TPS25810 response to various attachments to its port.

TPS25810 Port	CC1	CC2	OUT	TPS25810 Response				
				VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

8.4.2 Current Broadcast Capability and Overload Protection

TPS25810 supports all three Type-C current advertisements as defined by the base spec. Current broadcast to a connected UFP is controlled by the CHG and CHG_HI pins. For each broadcast level the device protects itself from a UFP that draws current in excess of the port's USB Type-C Current advertisement by setting current limit as shown in the table below.

Under overload conditions, the internal current-limit amplifier regulates the output current to selected I_{LIM} for OUT and VCONN pins (when connected). OUT/VCONN voltage will droop during current regulation resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold T_{TH_OTSD1} the internal FET associated with either VCONN or OUT will be turned off and FAULTb pin will be pulled low to signal fault condition. TPS25810 will commence to start-up when Tj cools down to < [T_{TH_OTSD1} – 20°C]. FAULTb pin will then pull high. Current limit response time to short circuit is 1.5 uS (TYP).

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

8.4.3 Device Power Pins (IN1, IN2, AUX, OUT and GND)

The device has multiple input power pins; IN1, IN2 and AUX. IN1 is connected to OUT by the internal power FET and serves the supply for the Type-C charging current. IN2 is the supply for VCONN and ties directly between VCONN power switch on its input and CC1 or CC2 on its output. AUX or auxiliary input supply provides power to the chip.

In the simplest implementation where multiple supplies are not available; IN1, IN2 and AUX can be tied together. However in mobile systems (battery powered) where system power savings is paramount, IN1 and IN2 can be powered by the high power DC-DC supply (>3A capability) while AUX can be connected to low power supply that typically powers the system uC when system is in hibernate or sleep power state. Unlike IN1 and IN2, AUX can operate directly from a 3.3V supply commonly used to power uC when system is put in low power mode.

A ceramic bypass capacitor close to the device from IN/AUX to GND is recommended to alleviate bus transients. The recommended operating voltage range for IN1/IN2 is 4.5V-5.5V while AUX can be operated from 2.9V to 5.5V.

8.4.4 FAULT Response

FAULTb pin is an open drain output that asserts (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is crossed. Refer to section 5.5 for over current and temperature values. The FAULTb signal remains asserted until fault condition is removed and the device resumes normal operation. The device is designed to eliminate false over current fault reporting by using internal deglitch circuit.

Connect FAULTb with a pull up resistor to AUX. FAULTb can be left open or tied to GND when not used.

8.4.5 Thermal Shutdown

Device has two internal over temperature shutdown thresholds, T_{TH_OTSD1} and T_{TH_OTSD2}, to protect the internal FET from damage and overall safety of the system. $T_{TH\_OTSD2} > T_{TH\_OTSD1}$. FAULTb is asserted low to signal a fault condition when device temperature exceeds T_{TH_OTSD1} however when T_{TH_OTSD2} is exceeded all open drain outputs are left open and device is disabled such that minimum power/heat is dissipated. The device will attempt to power-up when die temperature is < [T_{TH_OTSD1} - 20°C]

8.4.6 REF

A 100KΩ (1% or better recommended) resistor connected from this pin to ground sets the reference current required to bias internal circuitry of the device. The overload current limit tolerance depends upon the accuracy of this resistor, using a ±1% metal film resistor, or better, will yield best current limit accuracy and overall device performance.

8.4.7 Audio Accessory Detection

USB Type-C spec defines an Audio adapter decode state which allows implementation of an analog USB Type-C to 3.5 mm headset adapter. TPS25810 will detect an audio accessory device when both CC1 and CC2 pins sees vRa voltage (when pulled to ground by Ra resistor). The device will in response assert open drain AUDIOb pin low to indicate the detection of such a device.

CC1	CC2	AUDIOb	State
Ra	Ra	Asserted (pulled LO)	Audio Adapter Accessory Connected

Platforms supporting this extension can trigger off from AUDIOb pin to enable accessory mode circuits to support audio function. When Ra pull-down is removed from either CC1 or CC2, AUDIOb is de-asserted or pulled HI. When this function is not needed (for example in data-less port) AUDIOb can be tied to GND or left open.

8.4.8 Debug Accessory Detection

Type-C spec supports an optional Debug Accessory mode used for debug only and shall not be used for communicating with commercial products. When TPS25810 detects vRd voltage on both CC1 and CC2 pins (when pulled to ground by Rd resistor) it asserts DEBUGb pin low. With DEBUGb pin asserted, the system can enter debug mode for factory testing or similar functional mode. DEBUGb will de-assert or pull HI when either Rd pull down is removed from CC1 or CC2. If Debug accessory mode is not used tie DEBUGb to GND or leave it open.

CC1	CC2	DEBUGb	State
Rd	Rd	Asserted (pulled LO)	Debug Accessory Mode connected

8.4.9 Plug Polarity Detection

Reversible Type C plug orientation is resolved by the POLb pin when a UFP is connected. Below describes POLb state based on which device CC pin detects vRd from an attached UFP pull-down. When no UFP is connected POLb remains de-asserted. Since POLb is an open drain output, pull-high with 100KΩ to AUX when used; tie to GND or leave open when not used.

CC1	CC2	POLb	State
Rd	Open	Hi-Z	UFP connected
Open	Rd	Asserted (pulled LO)	UFP connected with reverse plug orientation

8.4.10 Device Enable Control

EN pin provides a convenient way to turn-on or turn-off the device while it is powered. Enable input threshold has hysteresis built-in, when this pin is pulled high, the device is turned-on or enabled. When device is disabled (EN pulled LO) the internal FETs tied to IN1 and IN2 are disconnected, all open drain outputs are left open (Hi-Z) and CC1, CC2 monitor block is turned off. EN terminal should not be left floating.

8.4.11 Load Detect

Load detect function in the device is enabled when it is set to broadcast high current charging (CHG = CHG_HI = V_{AUX}) on the CC pin. In this mode the device will monitor charging current to a valid UFP, if the charging current exceeds 1.67A (TYP) LD_DETb pin will assert. Since LD_DETb is an open drain output, pull-high with 100KΩ to AUX when used; tie to GND or leave open when not used.

8.4.12 Power Wake

Refer to below Figure. To enable power wake the UFPb from device #1 and #2 are tied together (each with its own 10KΩ pull-up) to the ENb pin of 5V/5A DC-DC. When no valid UFP is detected on *both* Type C ports, the ENb pin of DC-DC is pulled-hi thereby disabling it. Since both TPS25810 are powered by an always-on 3.3V LDO, turning off IN1 and/or IN2 supply does not affect its operation in detach state. Anytime a valid UFP is detected on either port, the corresponding TPS25810 UFPb pin is pulled low enabling the DC-DC to provide charging current to the attached UFP. Turning off the high power DC-DC when ports are unattached saves on system power.

8.4.13 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power made possible with the use of LD_DETb. It is for systems that have multiple charging ports but cannot power them all at their maximum charging current *simultaneously*.

Goals of PPM are:

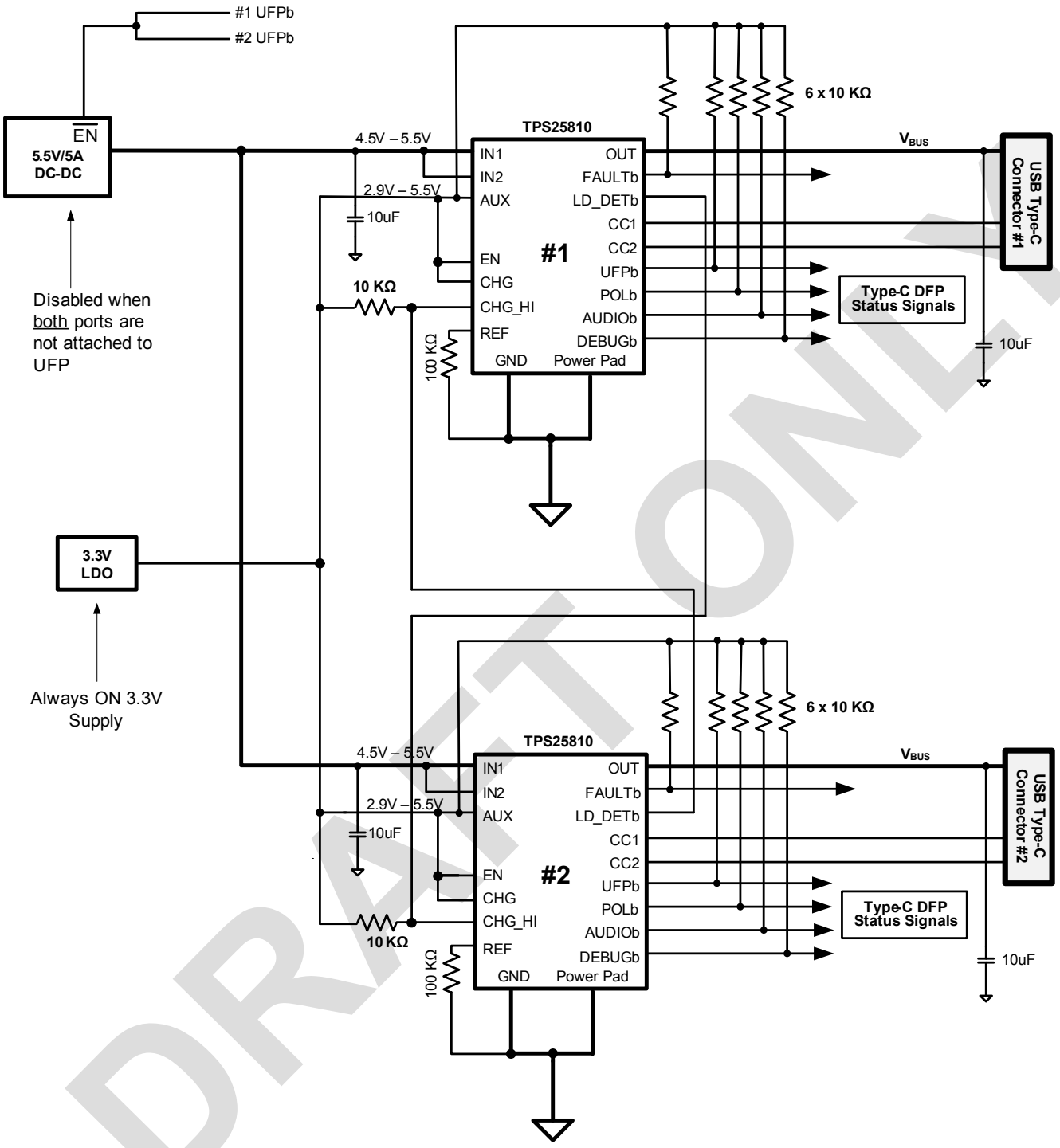
1. Enhances user experience since user does not have to search for high current charging port
2. Lowered cost and size of power supply needed for implementing high current charging in multiple Type C port in a system

Below Figure shows PPM and power wake implemented in a system with two Type C ports both initially set to broadcast high current charging (3A, CHG and CHG_HI pulled HI). Each device independently monitors charging current drawn by its attached UFP. Any device that provides a charging current that is higher than the LD_DETb threshold (1.77A) causes its LD_DETb to assert or pull-low. Since the LD-DETb of #1 and #2 device are connected back-two-back to the CHG_HI pin of the other device, a high current detection on one port forces the other port to broadcast 1.5A or medium charging current capability on its CC pin.

This simple scheme:

- Delivers better user experience as user does not have to worry about maximum charging current rating of the host ports, both ports initially advertise high current charging
- Enables smaller and lower cost power supply as the loading is controlled and never allowed to exceed 5A

8.4.14 Implementing Power Wake and Port Power Management in two port system



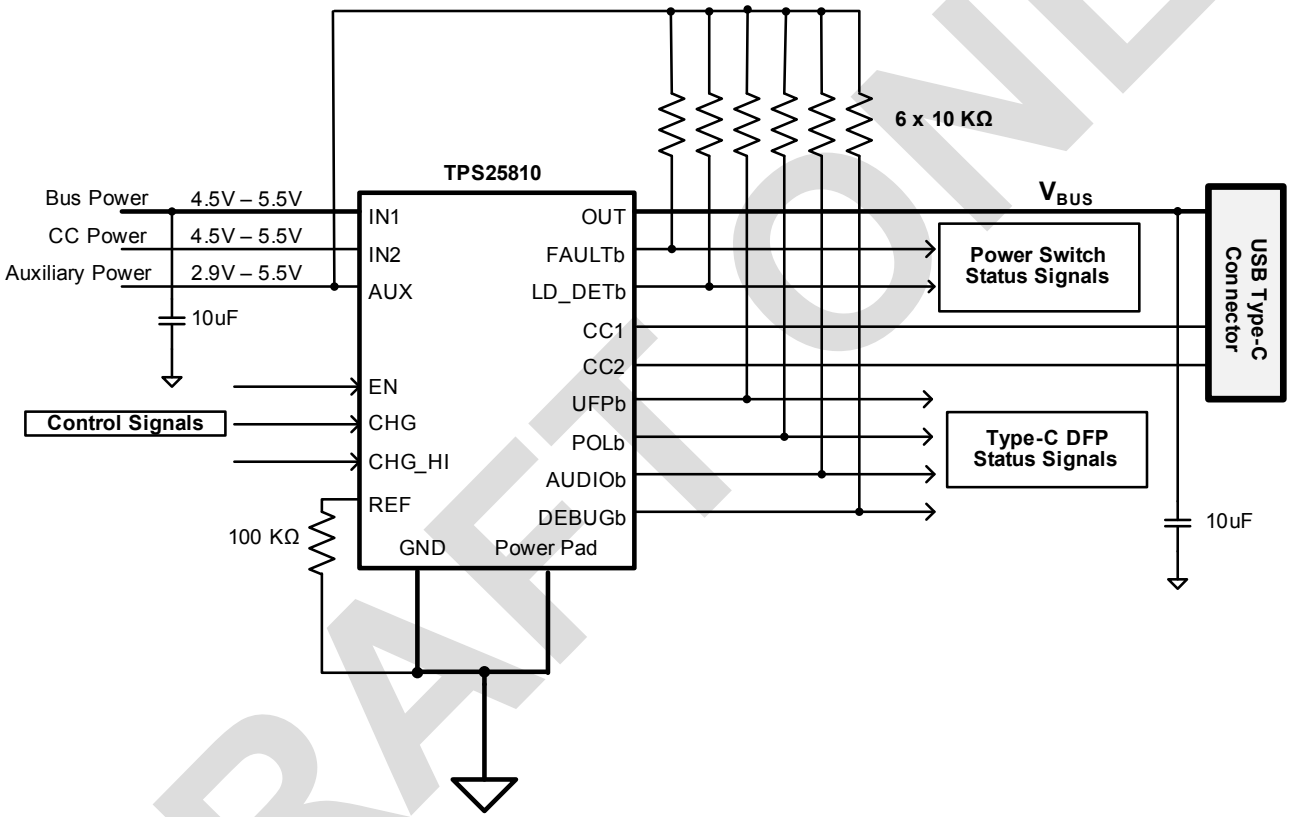
9 Application and Implementation

9.1 Application Information

The TPS25810 is a Type –C DFP power switch. It is typically used in a PCs/Tablets to implement Type-C USB host port without USB PD. It supports highly integrated features offered by latest Type C spec. and also adds to it to deliver lower system power design and enable port power management in multi-port systems. Additionally the CC1 and CC2 pins have built-in ESD protection tested to IEC61000-4-2 level on device evaluation board thereby lowering BOM cost in a typical implementation.

9.2 Typical Application

9.2.1 Type C Host Port in PC/Tablet

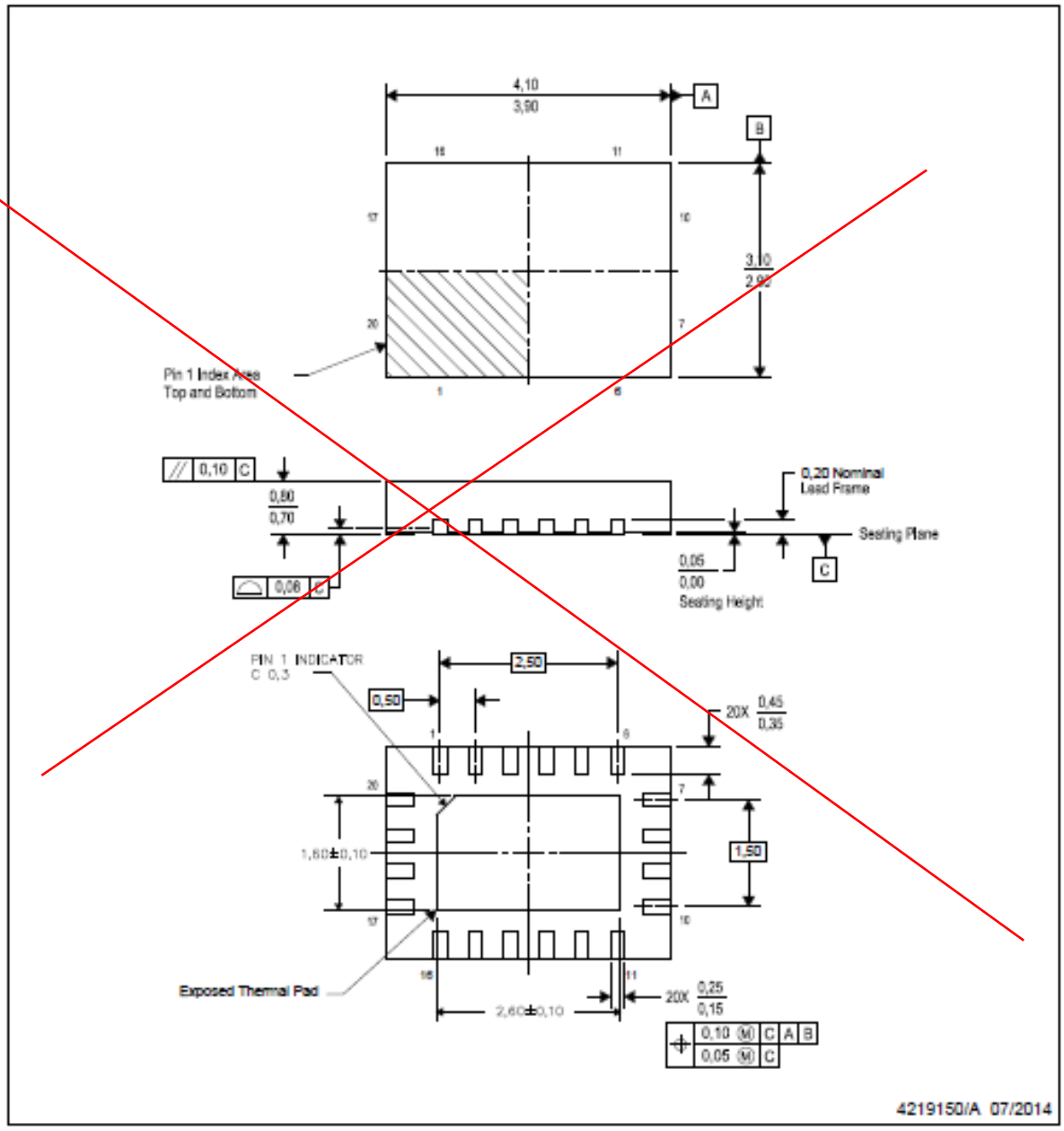


PACKAGE OUTLINE

RVC0020A

WQFN - 0.8 mm max height

WQFN



NOTES:

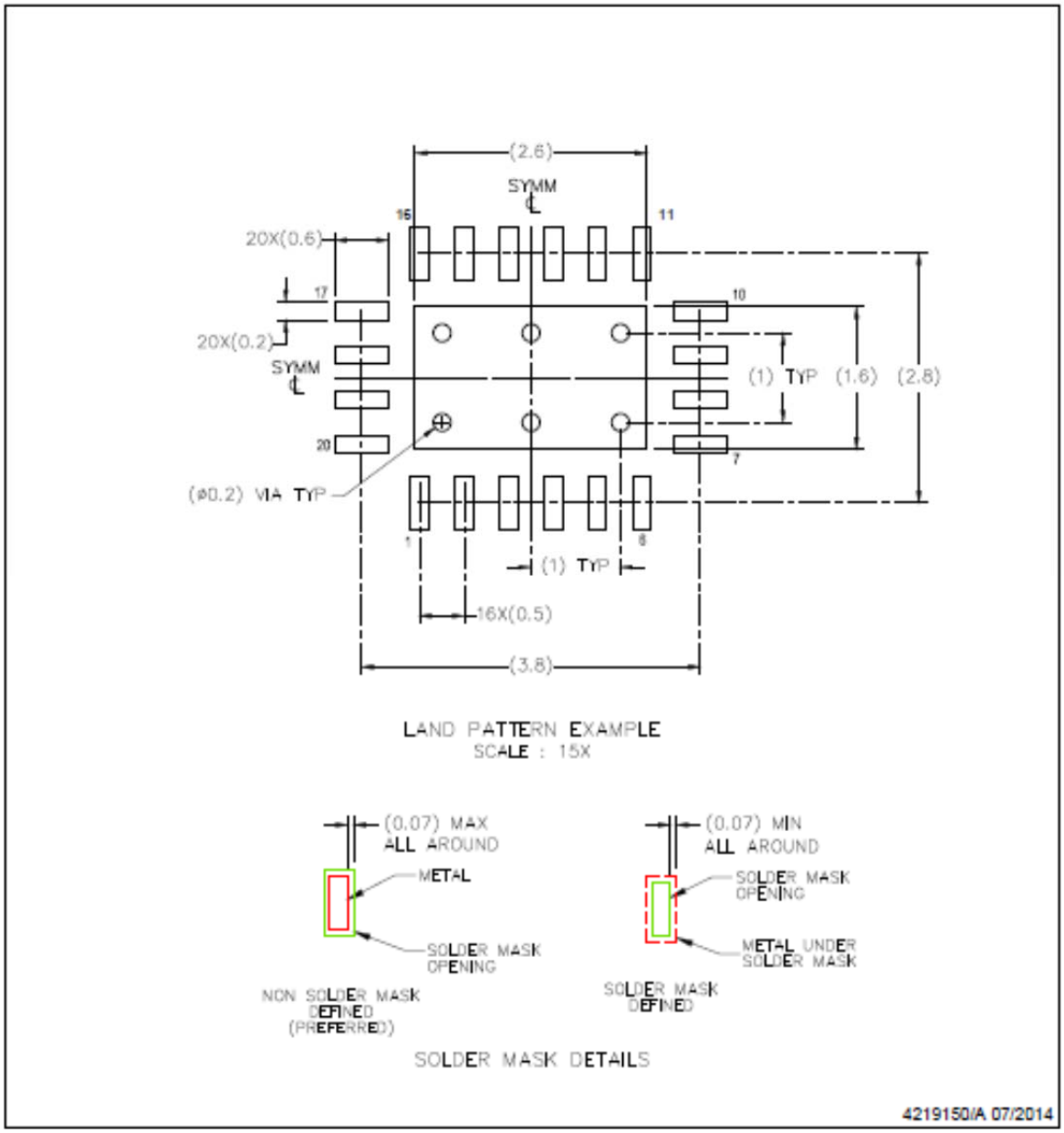
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RVC0020A

WQFN - 0.8 mm max height

WQFN



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271) .

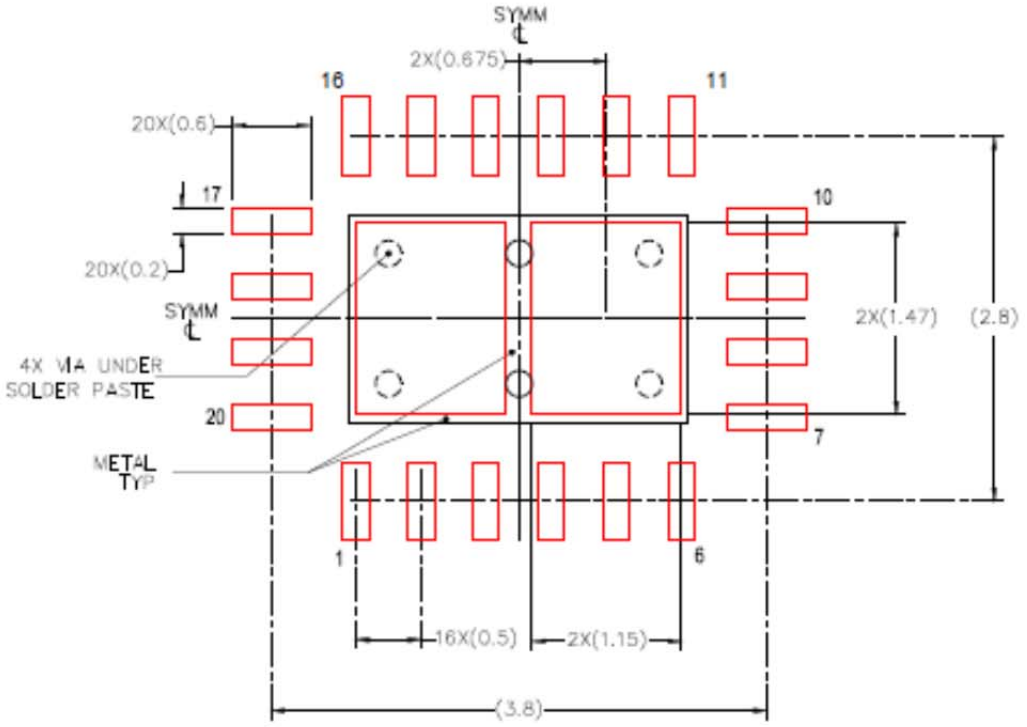
PRODUCT PREVIEW

PRODUCT PREVIEW

EXAMPLE STENCIL DESIGN

RVC0020A — **WQFN - 0.8 mm max height**

WQFN



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE : 20X

4219150/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.