

3 RGMII/SGMII to Copper

PIN	PIN_NAME	STRAP NAME	DEFAULT	ANEG_DIS	ANEGSEL_1	ANEGSEL_0	FUNCTIONAL
47	LED_0	ANEG_DIS	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 3000/100advertised, Auto MDI-X
				0	1	0	Auto-negotiation, 100/10 advertised,Auto-MDI-X
46	LED_1	ANEGSEL_0	0	0	1	1	M
				0	1	0	M
				1	0	1	M
45	LED_2	ANEGSEL_1	0	1	1	0	Forced 1000k, full duplex, MDI-X
				1	1	1	Forced 1000k, full duplex, MDI-X
38	RC_CTRL	MIRROR_EN	0	0			Port Mirroring Disabled
				1			Port Mirroring Enabled

1 PHY Address £ ° 0000

PIN	PIN_NAME	STRAP NAME	DEFAULT	PHY_ADD1		PHY_ADD0	
33	RX_D0	PHY_ADD[1:0]	00	W0IDE_0	0	W0IDE_0	0
				W0IDE_0	0	W0IDE_0	1
				W0IDE_0	1	W0IDE_0	0
				W0IDE_0	1	W0IDE_0	1
34	RX_D1	PHY_ADD[3:2]	00	W0IDE_0	0	W0IDE_0	0
				W0IDE_0	0	W0IDE_0	1
				W0IDE_0	1	W0IDE_0	0
				W0IDE_0	1	W0IDE_0	1

2 OP_MODE:000

PIN	PIN_NAME	STRAP NAME	DEFAULT	OPMODE[2]	OPMODE[1]	OPMODE[0]	FUNCTIONAL
22	JTAG_TDO /GPIO_1	OPMODE[0]	0	0	0	0	RGMII to Copper/1000Base-T /100Base-TX/10Base-Tx
				0	0	1	RGMII to 100Base-Tx
36	RX_D2	OPMODE[1]	0	0	1	0	RGMII-SCMII Bridge Mode
				0	1	1	RGMII to 100Base-FX
35	RX_D3	OPMODE[2]	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-Tx to 100Base-FX
				1	1	0	SGMII to Copper
				1	1	1	JTAG for boundary scan

4 Configurable clock skew

Configurable clock skew			
Aligned mode		Shift mode	
GT_X_CLK	Register :RGMIICTL	Address 32h	Register :RGMIICTL
RX_CLK			Address 86h

also ,when OP_mode[2.0]=000 LED Defaults: RGMII to Copper LED0 :10/100/1G LINK -UP LED1 : 1GLINK-UP LED2 :TX AND RX Activity

. LEDS_CFG2 Register : bit 2 bit6 bit10 are LED_0_POLARITYTS , NON STRAP Default active high

